# Fault-tolerant Open-Source CPU for Space

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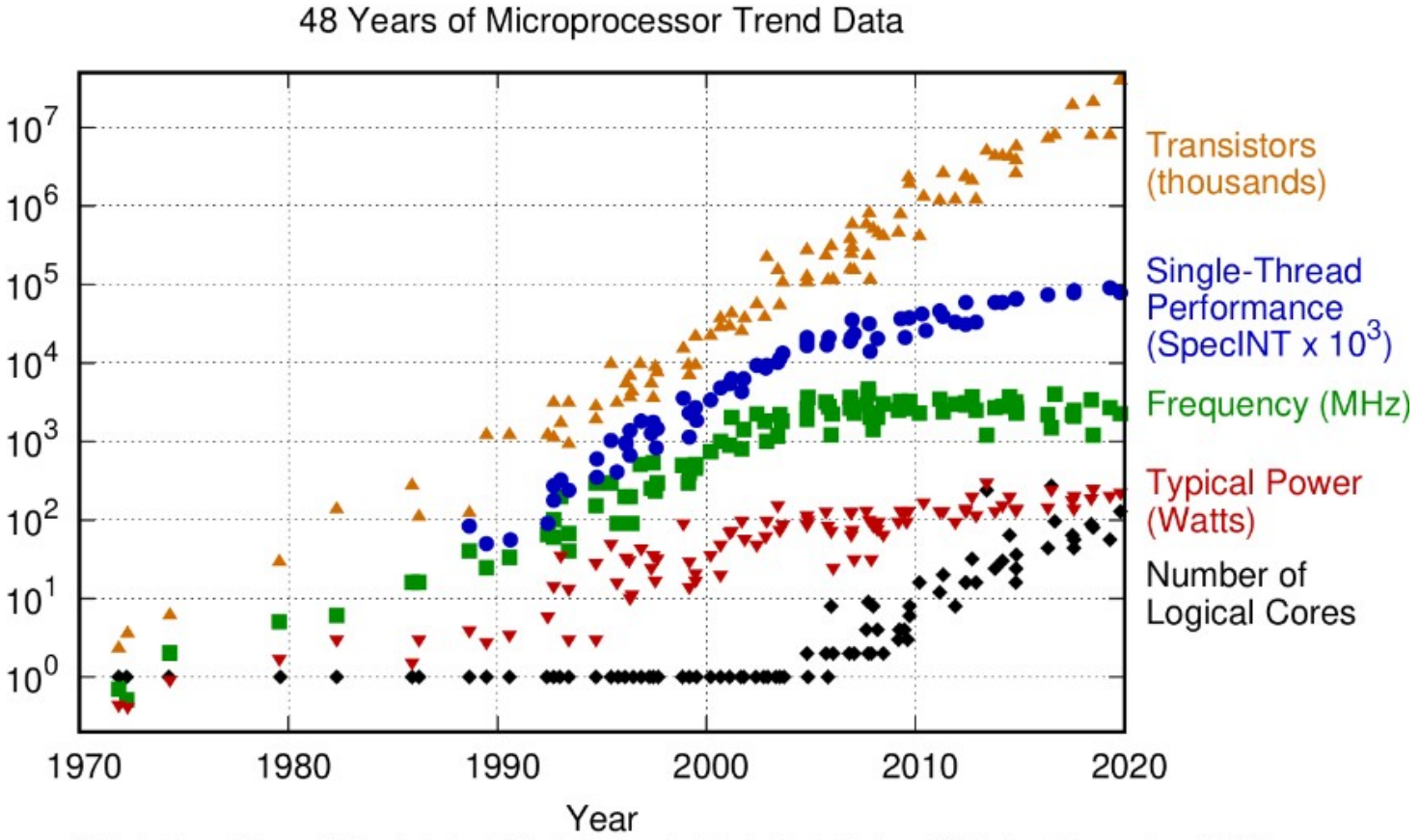
# Embedded systems were born as dependable

Embedded systems were born with Viking and Voyager missions, where also most of the current basic building blocks were developed (EPROMs, microcontrollers, ADC, DAC ... as well as specific ISAs and software languages)

Voyager-2 will turn 44 years old on 20th August!

# There is no alternative to progress, in space too.




However Rad-hard processors typically lag more than a decade behind

**Example: PowerPC-750 evolution from 1990s to 2005**

Commercial **2400x**
Space **300x**



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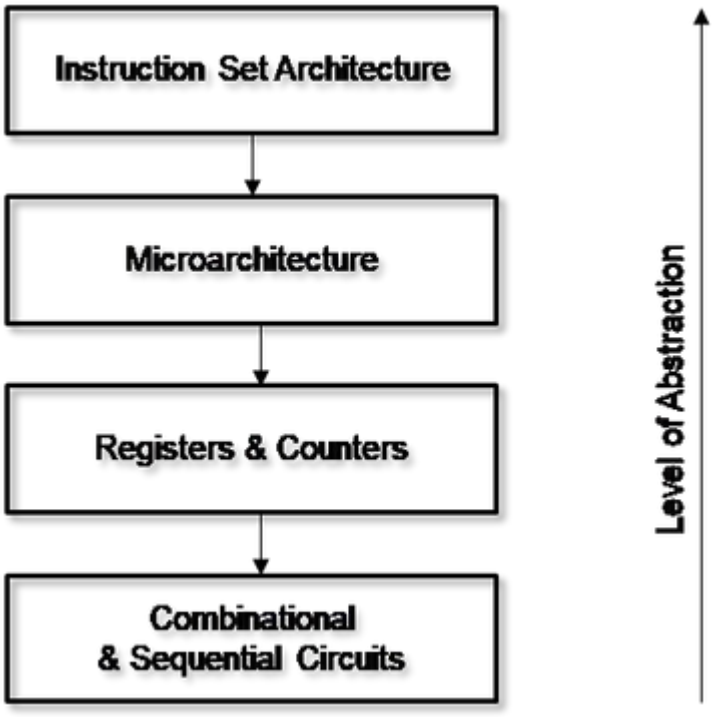
# Instruction Set Architecture (ISA)

An instruction set architecture is an abstract model of a computer which defines the **basic operations** it must support.

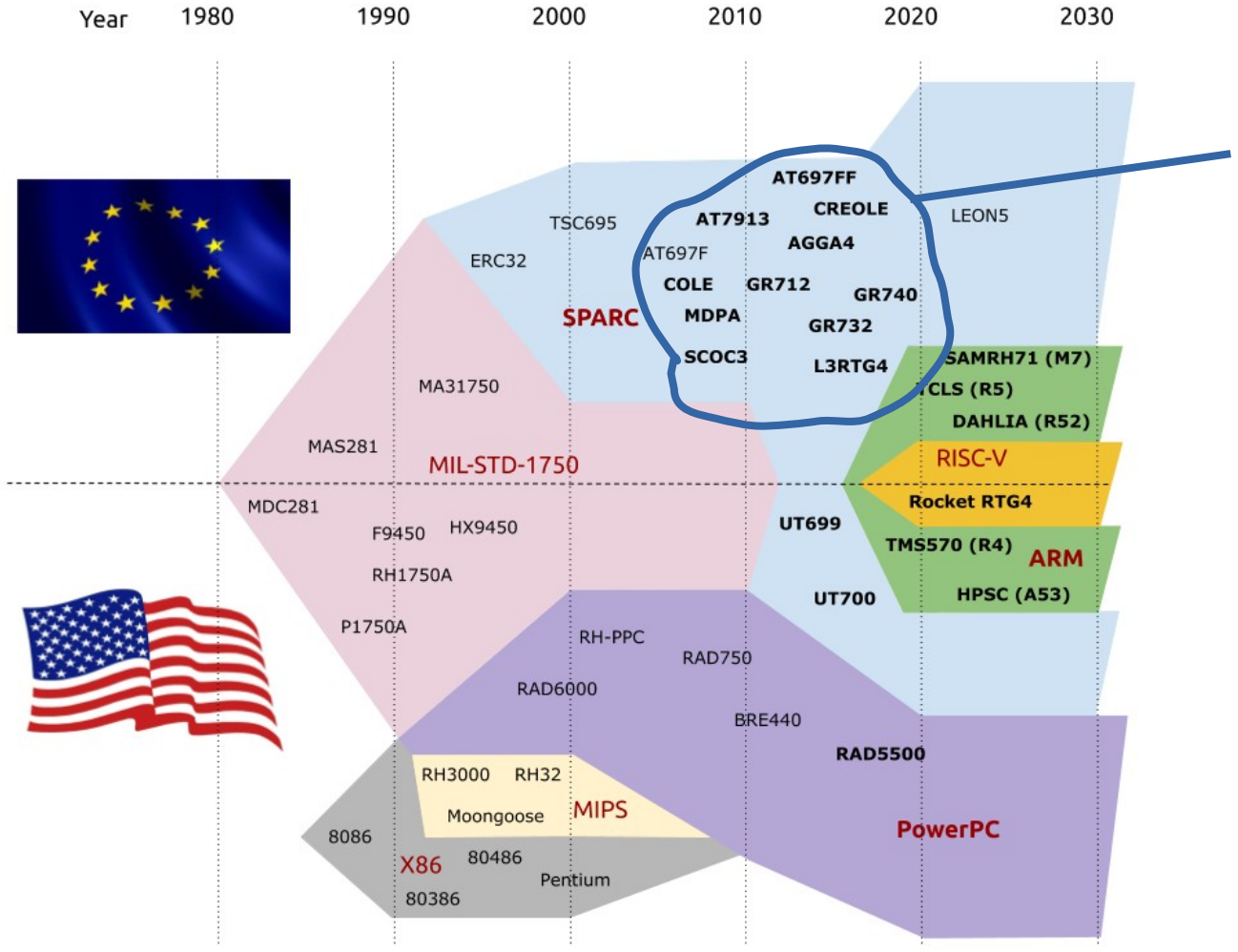
- Type of instruction (arithmetic/logic, data transfer, branch/jump)
- Maximum length of an instruction (i.e. 32 or 64 bits)
- Instruction format




An ISA can be seen as the **interface between software and hardware**.

Two big categories: Complex Instruction Set (CISC) and Reduced Instruction Set (RISC)

# CPU ISAs in Europe and US




ESA (and large part of the worldwide space community) is using LEON-based SoC for ongoing and planned missions

*From: Di Mascio et al. ApplePies 2018. Lecture Notes in Electrical Engineering, vol 550. Springer, Cham. doi: 10.1007/978-3-030-11973-7_37*



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# Challenges of space vs commercial.

Development of space grade processors is severely limited by:

1. **User space**
   - *Most successful processor ever (ESA's ERC32) sold only ~16000 pieces.*

2. **Access to IP and Foundries**:
   - *The limited market pushes for open ISAs.*
   - *Non-Recurring Engineering cost  of <28nm chip is huge (given the scale above)*
   - *e.g. no GPUs for space (too short market lifetime) !*

3. **Physics:**
   - *Radiation/ soft errors,*
   - *Memory (size, speed),*
   - *Thermal issues,*
   - *Packaging limitations,*
   - *Power supply stability.*

# Why an Open Source ISA?

The re-use of open ISAs gives the possibility to reuse an established **software ecosystem** (compilers, debuggers, development environment)

- The choice of SPARC by ESA in the 90s was based on this and proved to be very successful
- However SPARC has lost momentum in terrestrial applications, mainly because of the predominance of the proprietary x86.
- New markets with different requirements in terms of energy efficiency (e.g. mobile devices) have led to the success of proprietary ISAs from ARM.

# RISC-V

- RISC-V was originally developed in 2010 by UC Berkeley to support computer architecture research and education.
- The spread of an open and free ISA like RISC-V already enabled a broad range of research activities for terrestrial application (e.g. security, AI, etc.).
- RISC-V is backed also by big players of the commercial field: Google, Qualcomm, IBM, NVIDIA, Samsung and Western Digital are members of the RISC-V Foundation.




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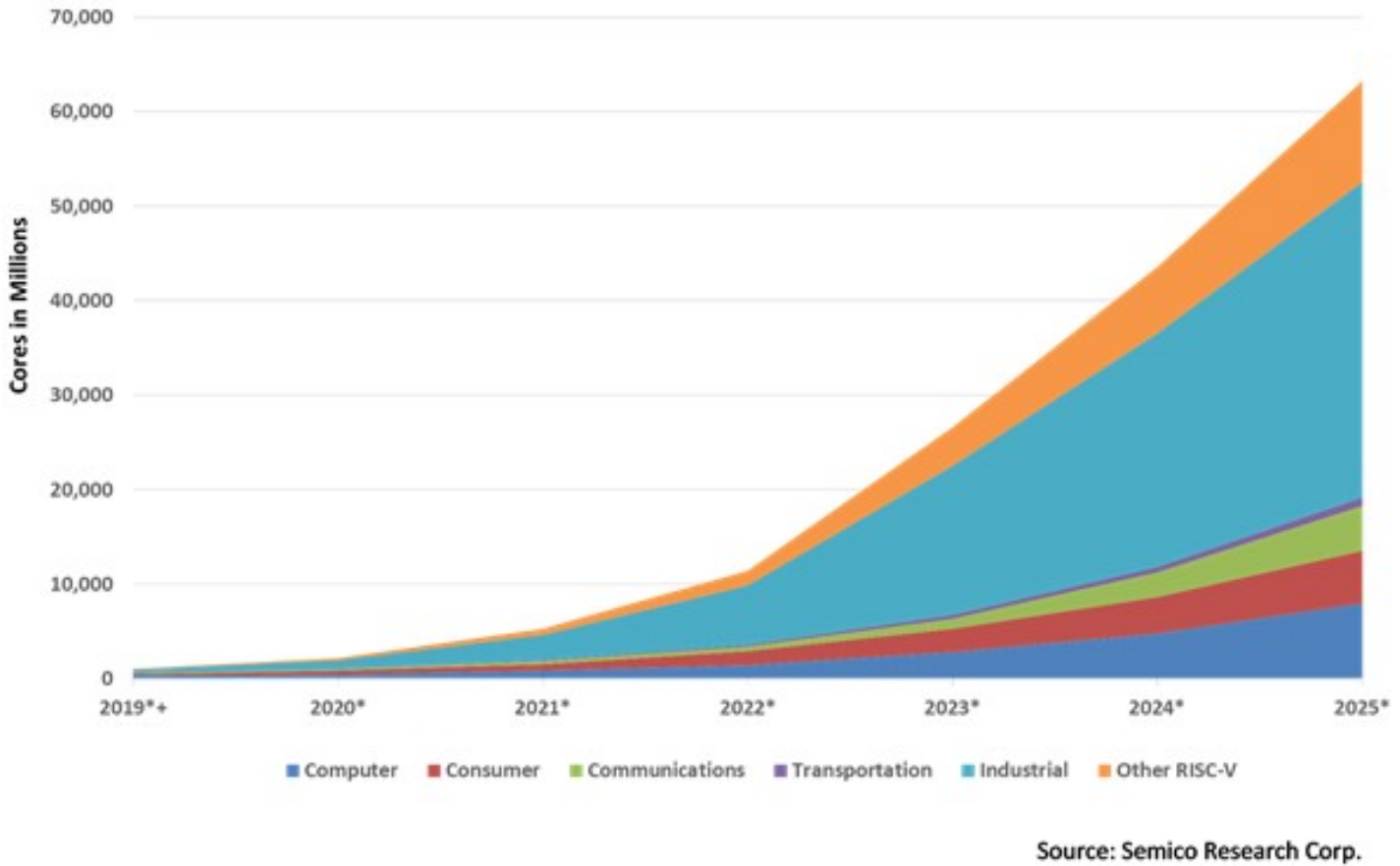
# RISC-V community is growing fast.




Semico forecasts strong growth for RISC-V, predicting the market will consume 62.4 billion RISC-V CPU cores by 2025



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# RISC-V in space.

Since a few years also ESA and the European space industry is investigating space application of RISC-V. Cobham Gaisler has released in 2020 Noel-V investigating FT adaptations to specific target technologies.

| Configuration | ISA* | Pipeline | Cache | MMU | PMP | FPU | Note | Availability |
|---|---|---|---|---|---|---|---|---|
| **TIN32** | RV32IM | single issue | no | no | no | no | Tiny configuration | 2020-Dec |
| **MIN32** | RV32IM AC | single issue | yes | no | yes | no | Minimal 32-bit configuration | 2020-Dec |
| **MIN64** | RV64IM AC | single issue | yes | no | yes | no | Minimal 64-bit configuration | 2020-Dec |
| **GPP32** | RV32GC HN | single issue | yes | yes | yes | GRFPU or NanoFPU | General purpose 32-bit configuration | 2020-Dec |
| **GPP64** | RV64GC HN | single issue | yes | yes | yes | GRFPU or NanoFPU | General purpose 64-bit configuration | 2020-Dec |
| **HPP32** | RV32GC HN | dual issue | yes | yes | yes | GRFPU or NanoFPU | High-performance 32-bit configuration | 2020-Dec |
| **HPP64**** | RV64GC HN | dual issue | yes | yes | yes | GRFPU or NanoFPU | High-performance 64-bit configuration | Available |


Available NOEL-V configurations from Gaisler

https://www.gaisler.com/index.php/products/processors/noel-v



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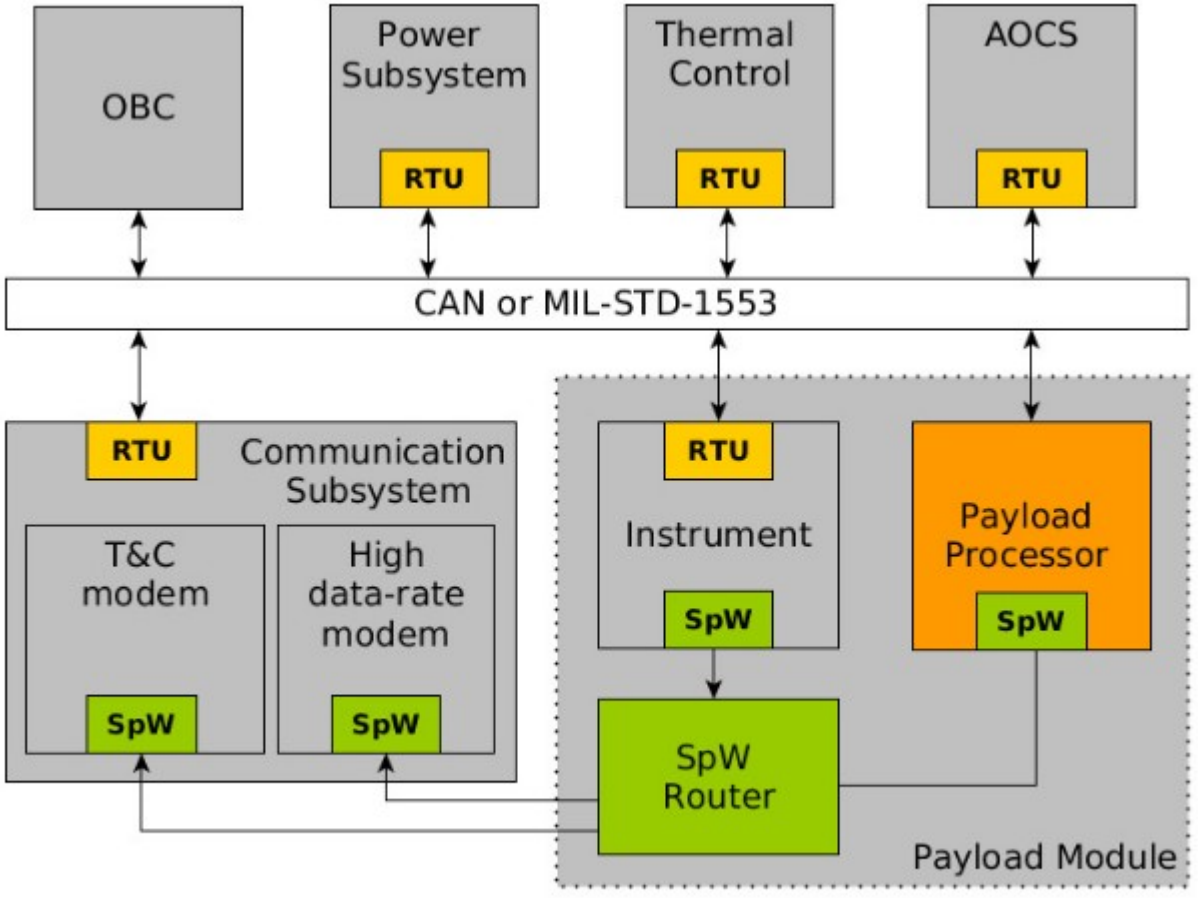
# Typical satellite data system architecture.



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# Evolution of space On-Board Computers.

| OBC | GOCE CDMU | GAIA CDMU | OSCAR (SCOC3) |
|---|---|---|---|
| Year | 2009 | 2013 | 2014 |
| Manufacturer | TAS-I | RUAG-S | AIRBUS |
| CPU (ISA) | ERC32 (SPARCV7) | LEON2FT (SPARCV8) | LEON3FT (SPARCV8) |
| Frequency [MHz] | 24 | 80 | 80 |
| Computational speed [MIPS] | 17 | 65 | 68 |
| Instructions per clock cycle | 0.71 | 0.81 | 0.85 |
| Pipeline stages | 4 | 5 | 7 |
| Power [W] | $\leq$ 90 (average) | $\leq$ 40 (average) | 15 (peak) |
| Mass [kg] | 21 | 16 | 5.2 |
| Dimensions [$mm^3$] | 470x272x332 | 420x270x276 | 250x150x216 |

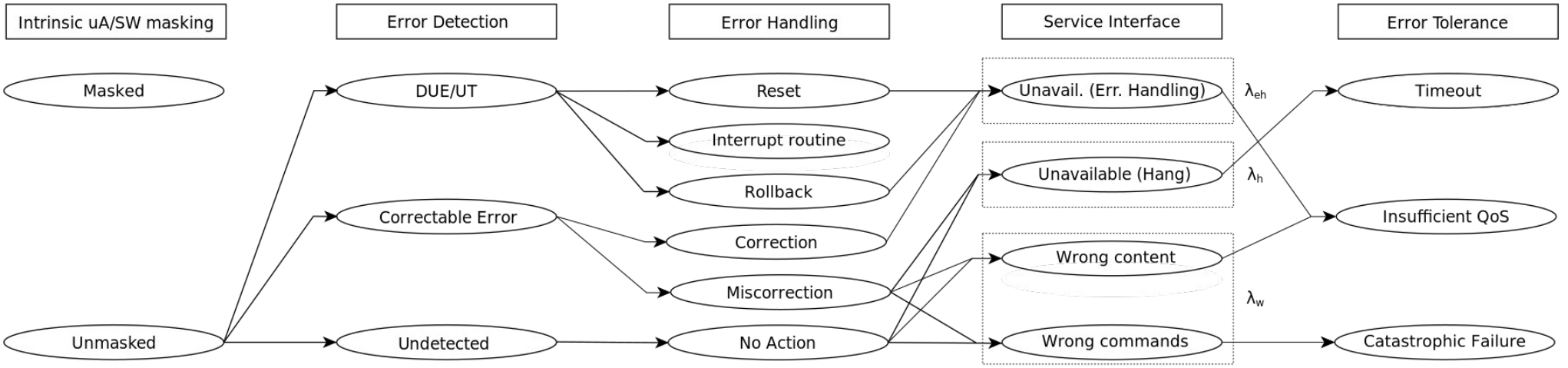
# Typical requirements for space grade processors.

Dependability

- A space grade OBC are typically required to have **less than one reboot in 15 years** due to all possible fault sources (soft errors, power faults, SW errors)
- A commercial 28nm (FDSOI) SRAM shows an in-orbit SEU rate of ~$5e^{-9}$ upsets/bit/day for solar minimum in GEO that may go up 3/4 order of magnitudes in case of solar events.
- As a comparison, for the processors in terrestrial environment, the upset rates at sea level is assumed to be ~$2e^{-11}$ upsets/bit/day

We cannot rely on process hardness only.

# Fault Tolerance relies on a multi layer design




✓You cannot rely on process hardness only.



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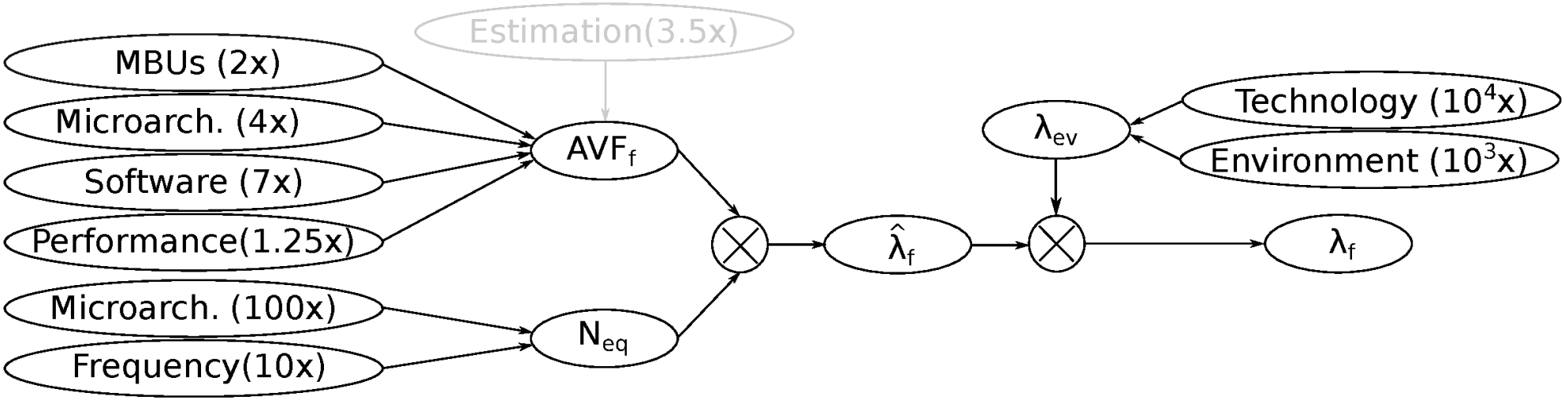
# Impact of each component




✓ You cannot rely on process hardness only.



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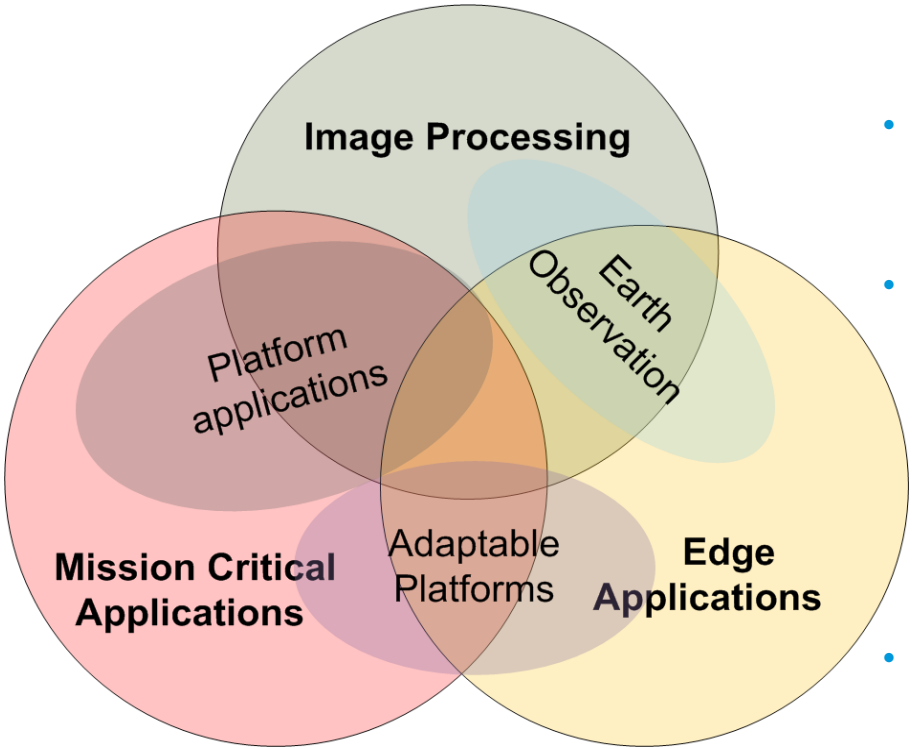
# Cache memories are critical in fault tolerance

- ✓Cache memories are shown to be the biggest contributors to the failure rate of processors due to soft errors, (e.g. the failure rate for the whole SET-sensitive processor is only less than doubled compared to a SET-immune layout).
- ✓ While the high Relative Soft Error Vulnerability of caches is largely insensitive to deviations in RSA and processor design, caches are so vulnerable in absolute terms that small deviations from reality of the models employed for errors (e.g. different fraction of MBUs) can cause an unacceptable behavior even when memory arrays are protected, given the demanding requirements of satellites in terms of dependability.

# AI/ML in space.




- **Debris removal, Docking, In orbit servicing**
  - Feature extraction
  - Identification against 3D mesh model
  - Obstacle avoidance
- **Landing, Robotic:**
  - Camera/LIDAR processing
  - Identification of craters, boulders
- **Payload processing**
  - Cloud identification to increase compression
  - Vessel detection/identification, integration with AIS receivers - identification of piracy
  - Open sea objects detection and monitoring
  - Identification of fast moving meteoroids
  - Fire/flares detection
- **Reconfigurable platforms**
  - Adapt platforms to change in requirements or new standards
  - Autonomous failure prognostic and detection
  - Autonomous Safe mode management



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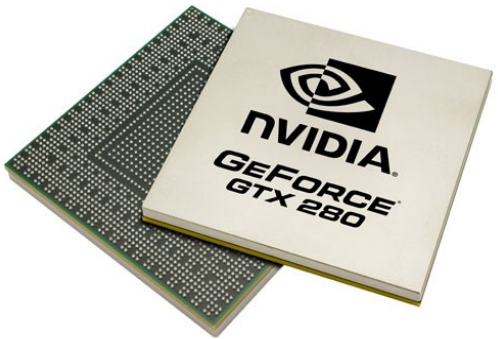
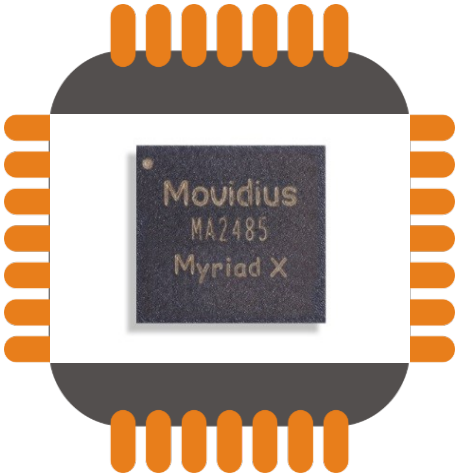
# HW for AI in space


**LEON - RISC-V**
**HPDP**
**PowerPC**




TEGRA
MALI
JETSON


**XILINX KU060**
XILINX
US/VERSAL
**BRAVE (future)**




**MYRIAD-2**
MYRIAD-X
KEEM BAY

**Agile, Flexible, 'easy'** ⟵ ⟶ **'Difficult', Efficient**



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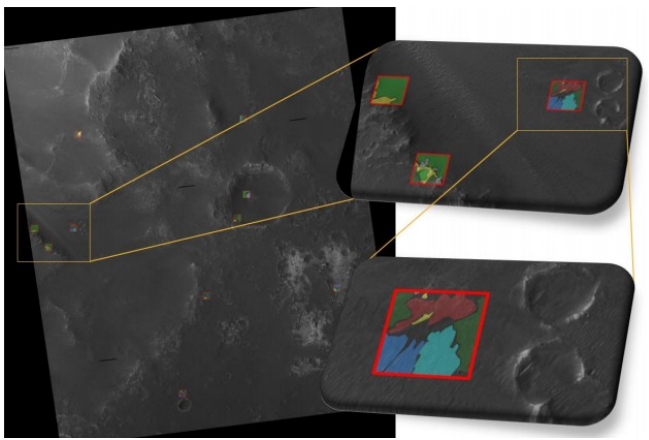
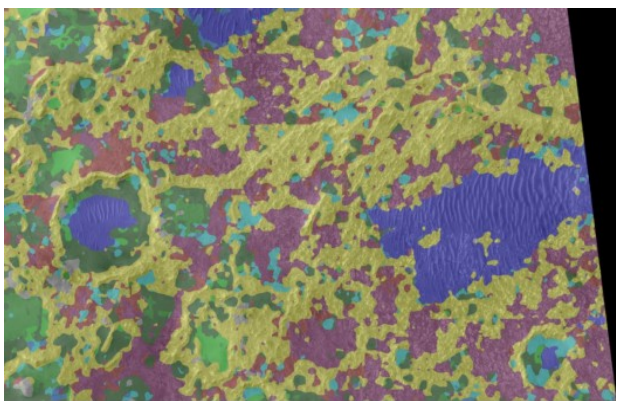
# AI for On-Board Autonomy – Payload data analytics

AI can be of great help to support on-board decisions to make possible for the spacecraft to autonomously select, among the science data it collects, which data is worth retaining of transmitting to ground.

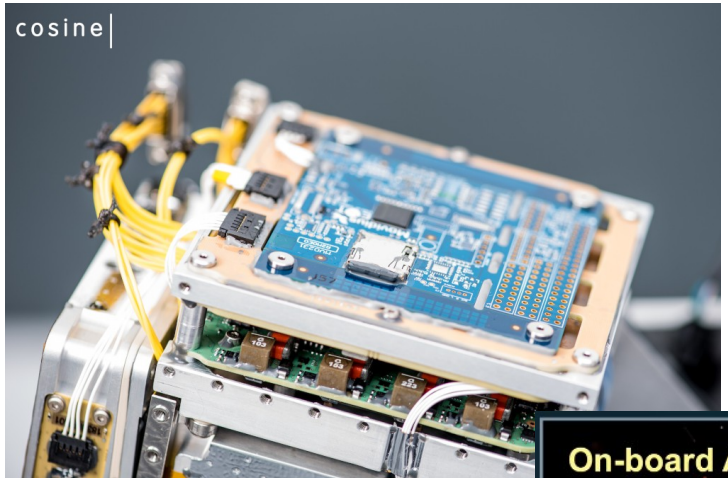


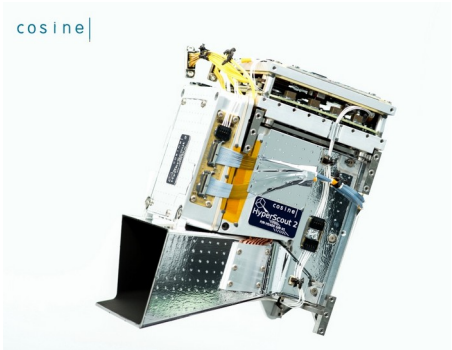
Small area annotated by geologist (teaching data)

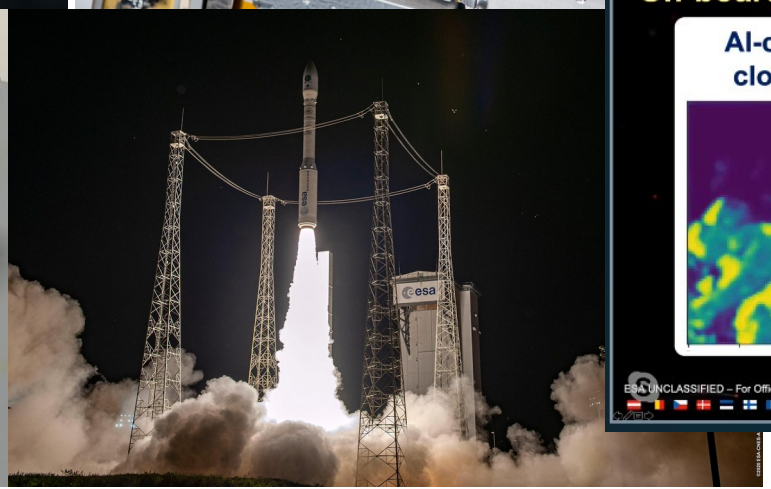


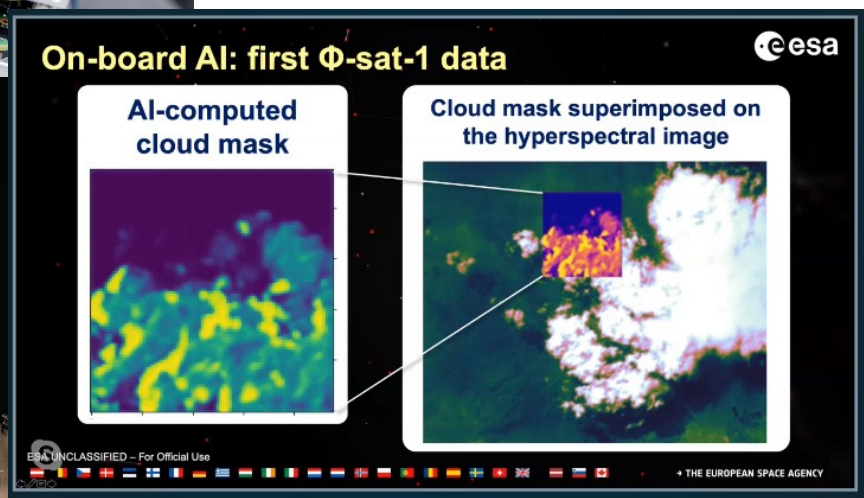
Much Larger area annotated by NOAH following Machine learning

# Phi-sat-1: first satellite with AI on-board.





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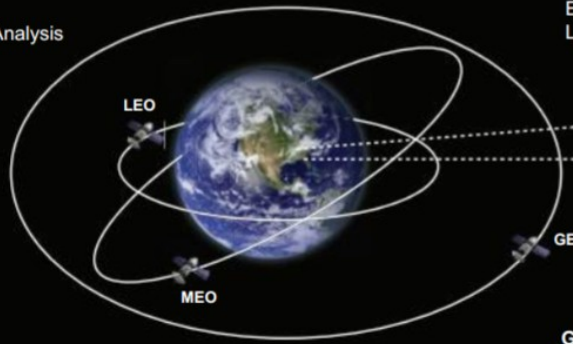
# Where do we go next?

**On Earth**
Data Processing
Planet/Comet/Asteroid Identification & Tracking
Constellation Management & Collision Avoidance
Weather Monitoring & Prediction
Natural Disaster Monitoring, Warning, & Impact Analysis
Autonomous Emergency First Response

**LEO**
EO/IR/SAR Data Processing & ATR
Astronaut Robotic Assistant & Health Management
Constellation Management & Collision Avoidance
Communication Network Reconfiguration/Optimization
Planet/Comet/Asteroid Identification & Tracking
Internet of Space Things
Weather Monitoring & Prediction
Natural Disaster Monitoring, Warning, & Impact Analysis
Autonomous Emergency First Response

**Moon**
Mineral/Mining Mapping & Site Identification
Swarm Drone Management & Optimization
Early Warning Threat Detection (Gateway)
Lunar Station/Base Power Optimization & Management

**Mars**
Autonomous Exploration & Weather Prediction
Mars Space Network Management & Optimizatio
Swarm Drone Management & Optimization
Mars Station/Base Power Optimization
& Management




**Route to Mars**
Solar/Cosmic Radiation Detection
Autonomous Navigation/Course Correction
Communication Network
Reconfiguration/Optimization

**Route to Deep Space**
Adaptive Propulsion
Extreme Data Compression
Deep Space Network Data Optimization

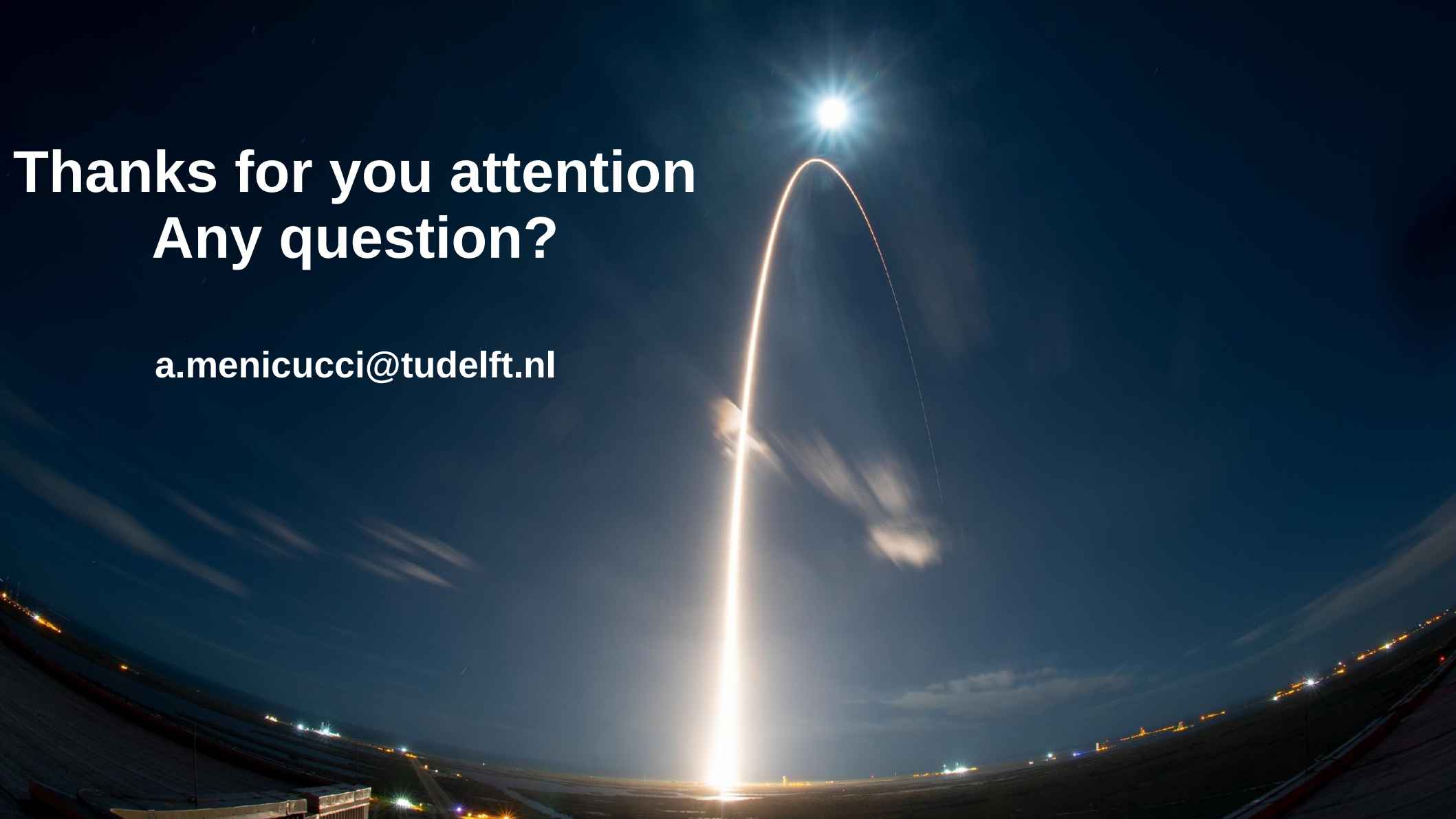
**Stratosphere**
EO/IR/SAR Data Processing
Communication Network Gap Enablement
Weather Monitoring & Prediction
Natural Disaster Monitoring, Warning, & Impact Analysis

**MEO**
Methane Super Emitter Tracking
Internet of Space Things
Collision Avoidance
Autonomous Emergency First Response

**GEO**
Smart Adaptive Comms
Solar Flare & GRB Monitoring & Notification
Weather Monitoring & Prediction
Natural Disaster Monitoring, Warning, & Impact Analysis
Autonomous Emergency First Response
Early Warning Threat Detection

# Conclusions

- Spin-in of Open Source ISAs has been and will continue to be a key for the success of space on-board computers
- RISC-V offers all the characteristics needed to become to new “standard” space processor which replaces the highly successful SPARC.
  - Openness
  - Modularity
  - Large growing community base with support of big players
  - Vector extension could enable on-board AI
    Fault-tolerance remains critical and must be addressed on multiple layers of the design



# Thanks for you attention
# Any question?

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# Some references:


- *The case for RISC-V in space* - International Conference on Applications in Electronics Pervading Industry, Environment and Society (2018)
- *Leveraging the Openness and Modularity of RISC-V in Space* - Journal of Aerospace Information Systems #11, 2019
- *A Fault-Tolerant MPSoC For CubeSats* - 2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)
- *On the Criticality of Caches in Fault-Tolerant Processors for Space*, 2019 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)
- *Single Event Effects Characterization of the Programmable Logic of Xilinx Zynq-7000 FPGA using Very/Ultra-High Energy Heavy Ions* - IEEE Transactions on Nuclear Science (2020)
- *Open-source IP cores for space: A processor-level perspective on soft errors in the RISC-V era* - Computer Science Review - Volume 39, February 2021, 100349