

Integrated Waveguides in Trapped Ion Quantum Computing Chips

A. Zesar^{1,2}, J. Wah^{2,3}, B. Lamprecht⁵, P. Hurdax⁵, M. Montagnese⁶, J. Pribošek⁶, M. Grüneberg⁶, C. Odaci⁶, K. Schüppert², C. Rössler², Y. Colombe², S. Auchter^{2,3}, S. Cano Castro^{2,7}, M. Glantschnig^{2,8}, F. Anmasser^{2,7}, M. Dietl^{2,7}, M. Schmauser³, M. Valentini³, P. Schindler³, T. Monz^{3,6}, J. Krenn¹

¹Institute for Experimental Physics, University of Graz, Graz, Austria

³Institute for Experimental Physics, University of Innsbruck, Innsbruck, Austria

⁵Joanneum Research Materials, Weiz, Austria

⁷Photonic Devices Group, Polytechnico di Milano, Italy

²Infineon Technologies Austria AG, Villach, Austria

⁴Alpine Quantum Technologies GmbH, Innsbruck, Austria

⁶Silicon Austria Labs, Villach, Austria

⁸Physikalisch-Technische Bundesanstalt, Braunschweig, Germany

Why Quantum Computing?

Optimization problems

Quantum simulations

Quantum Computing with Trapped Ions

life time ≈ 10 ns
 $P_{1/2}$
 blue laser readout 397 nm
 $S_{1/2} = |1\rangle$

life time ≈ 1 s
 $D_{5/2} = |0\rangle$
 red laser qubit 729 nm

motional states

Simplified electronic energy state scheme for Ca^{40+} ions.

Surface Ion Traps

Camera
Objective
100 μ m
Substrate

Sketch of a trapped ion setup with a surface ion trap on a chip.

Typical pseudopotential for a single trapping site on a surface ion trap.

Why Optical Integration in Ion Traps?

Useful QC requires 1000s of ions to talk to each other.

1000s of DC electrodes for ion control and shuttling

Wavelengths: 400 - 1800 nm

Laser access to 100s of ions @ ~ 10 nm beam accuracy

Standard Setup ion trap chip + free-space laser beams

Problems:

- Vibrations Typical. 1-10 nm
- Drifts Typical 100-1000 nm
- Scalability

Integrate Photonics in Chip!

Sketch of the Quantum CCD trap architecture for scaled up trapped ion processors. Ions are shuttled along lines in a grid. Laser access needs to be maintained at specific locations.

Optoquant Approach to Optical Integration

Waveguide
Metal Electrodes
Glass
Ion

9 mm
18 mm

Idea:

- Femto-second laser written waveguides in glass block
- Glass block bonded on chip via waferbond
- Butt-coupling via optical fiber
- Optional: Micro lens for beam focusing

Slab Waveguides and Thin Film Gratings

Al electrodes

SiO (upper cladding)
SiN/AlO/AIN
SiO (lower cladding)
Substrate

grating coupler

1000+ nm
50-200 nm
1000-4000 nm

Schematic cut through an ion trap chip with a slab waveguide and a focusing grating.

MIT Lincoln Labs, Illustration: Chet Beals

Integrated Optical Elements

b) Fiber end glued to incoupling facet of glass block

c) Femtosecond laser written waveguides in glass

e) Microlens placed on substrate

a) Fiber transports laser light to chip

d) Beam outcoupling at smooth sidewall

f) Beam waist at ion $\sim 30 \mu$ m

~ 1 mm

Waveguide Simulations

$\lambda = 730$ nm, $h = 150$ nm, sidewall angle = 90°

Sidewall taper 80°
h = 150 nm
w = 1000 nm

Profile of a slab waveguide with sidewall taper and denoted width and height. In the simulation the cladding extends 5 μ m to all directions.

Finite difference eigenmode simulation of the TE0 and TE1 modes. Here the effective index is plotted against the waveguide width at height 150 nm and wavelength 730 nm.

Field amplitude of a cut through the waveguide/cladding stack of modes TE0 and TE1 at a width of 600 nm. The waveguide is placed in the middle of the image. Here the TE1 is not guided in the waveguide. Instead we can see a mode that is guided at the boundaries of the cladding where a reflective metal boundary was placed.

Cutout of test chip design containing waveguide meanders of different lengths for cutback trials to obtain the waveguide losses.

Characterization of the Spot at the Ion

Spot at ion position

Stray light

intensity-distribution-vert

intensity-distribution-hor

4.63 μ m

5.11 μ m

Images by Mario Grüneberg (SAL)

ToDo: Fabrication and assembly of final design, trapping of ions
 Problems: stray light, small bending radii

ToDo: Fabrication of test chips, Characterization of materials and waveguides, Process development and optimization, Grating design and fabrication.