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Influence of grid configuration on grid-side inverters during faults

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Abstract

In order to achieve climate targets such as climate neutrality by 2050, the EU is relying primarily on wind and solar power in various scenario studies to make the energy supply as climate friendly as possible. In contrast to conventional hydroelectric and steam power plants, wind and solar power plants usually use power electronic interfaces, so-called inverters. These are used to convert the electrical energy into a grid-compliant form, characterized by voltage and frequency. However, modern connection guidelines and standards require inverter-based resources to have a variety of other grid-compliant characteristics that make the development and operation of such systems challenging. Compared to systems based purely on synchronous generators and transformers as the link between mechanical drive energy and delivered electrical energy, inverter-based systems are fundamentally different. One notable difference is the principle by which the plant synchronizes with the grid voltage. While in conventional power plants it is mainly physical laws that determine this behavior, in inverters this behavior is characterized by the implemented control method. This behavior is particularly interesting in grid-following inverters, which represent most of today's inverters. Such systems are always dependent on an externally controlled voltage and usually synchronize themselves with the help of a phase locked loop (PLL). In this work, an existing grid-following inverter model including PLL is analyzed, adapted to certain standard requirements and its stability behavior during grid faults is investigated. In addition, the model is to meet the requirements for use in the protection testing software *RelaySimTest* from *Omicron electronics*.

Kurzfassung

Um Klimaziele, wie Klimaneutralität bis 2050 zu erreichen, setzt die EU in verschiedenen Szenariostudien vor allem auf Wind- und Solarkraft, um die Energieversorgung möglichst klimafreundlich zu gestalten. Im Gegensatz zu konventionellen Wasser- und Dampfkraftwerken, werden in Wind- und Solarkraftwerken meist leistungselektronische Schnittstellen, sogenannte Umrichter eingesetzt. Diese werden verwendet, um die elektrische Energie in eine netzkonforme Form zu bringen, charakterisiert durch Spannung und Frequenz. Moderne Anschlussrichtlinien und Normen fordern von umrichterbasierten Erzeugern jedoch eine Vielzahl weiterer netzdienlicher Eigenschaften, welche die Entwicklung und den Betrieb solcher Anlagen zu einer Herausforderung machen. Verglichen mit Anlagen, welche rein auf Synchrongeneratoren und Transformatoren als Bindeglied zwischen mechanischer Antriebsenergie und abgegebener elektrischer Energie basieren, unterscheiden sich umrichterbasierte Anlagen grundsätzlich. Ein bemerkenswerter Unterschied ist das Prinzip, durch welches sich die Anlage mit der Netzspannung synchronisiert. Während in konventionellen Kraftwerken vor allem physikalische Gesetze dieses Verhalten bestimmen, wird in Umrichtern dieses Verhalten durch die implementierte Regelmethode charakterisiert. Besonders interessant ist dieses Verhalten bei netzgeführten Umrichtern, welche den Großteil heutiger Umrichter darstellen. Solche Anlagen sind immer auf eine extern geregelte Spannung angewiesen und synchronisieren sich meist mithilfe einer Phasenregelschleife (englisch: Phase Locked Loop, PLL). In dieser Arbeit wird ein bestehendes

netzgeführtes Umrichtermodell samt PLL analysiert, an bestimmte Normforderungen angepasst und dessen Stabilitätsverhalten während Netzfehler untersucht. Zudem, soll das Modell den Anforderungen entsprechen, um in der Schutztechnikprüfsoftware *RelaySimTest* von *Omicron electronics* eingesetzt zu werden.

List of indices and superscripts

x_s	sampling
x_{L12}	related to difference of phase L1 and L2 (respectively for other phases)
x_{pre}	pre-fault
x_1, x_2, x_0	positive, negative, zero sequence
x_{ref}	reference
x_d, x_q	direct, quadrature axis
$x_{PQ,DC}$	related to power and DC-link control
x_I	related to current
x_{PLL}	related to phase locked loop
x_α, x_β	Clarke components
x_{L1}	related to phase L1 (respectively for other phases)
x_c	center
x_D	delay
x_P, x_I	proportional, integral
$x_{cont.}$	artificially extended
x_{FFT}	fast fourier transform
x_{RMS}	root mean square
x_{temp}	temporary
x_{SC}	short circuit
x_{prim}, x_{sec}	primary, secondary
x_k, x_n	loop variable
x_{PCC}	point of common coupling
x_g	grid
x_f	fault
x_e	earth
x^T	orthogonal

List of abbreviations

UN	United Nations
GHG	Greenhouse gases
EU	European union
DC	Direct current
DFIG	Double fed induction generator
PLL	Phase locked loop
SRF	Synchronous reference frame
NERC	North American Electric Reliability Corporation
RMS	Root mean square
EMT	Electromagnetic transients
VDE	Verband der Elektrotechnik Elektronik Informationstechnik e. V.
FRT	Fault ride through
PCC	Point of common coupling
VSI	Voltage source inverter
PWM	Pulse width modulation
QSG	Quadrature signal generator
SOGI	Second order generalised integrator
FFT	Fast Fourier transform
PV	Photovoltaics
PI	Proportional-integral
LV	Low voltage
SM	Synchronous machine
MV	Medium voltage
DOA	Domain of attraction
HV	High voltage
HIL	Hardware in the loop

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1 Introduction

1.1 Motivation

Environmental changes and latest political tensions show that the transition from conventional energy resources towards renewable and environmentally friendly solutions is one of the most important topics in modern era. The year 2022 showed once again how far-reaching the strong dependency of European countries on the import of fossil fuels is. Prices for oil reached record levels of 2014 [1], while the European short-term gas price even reached an all-time record [2]. The associated budget problems for households, the risk of bankruptcy for companies and even whole economical regions, in addition to further increasing greenhouse gas emissions [3] highlight the need for a drastic change in modern energy politics.

Concerning this topic, already back in 2015, at the UN Climate Change Conference in Paris, a legally binding international contract was decided and accepted by 194 parties worldwide, the so-called *Paris Agreement*. The adopted goals contain a reduction of greenhouse gas emissions to reach a limited temperature rise of 2° for the current century. In addition, it was agreed to review participating countries commitment every five years and to enable financial help for developing countries [4].

Europe has in this climate transition a worldwide lead role [5, 6] and reached the own intermediate goal, of reducing the greenhouse gas (GHG) emissions until 2020 by 20 % compared to 1990 clearly already in 2019. By 2020 the GHG-emissions were reduced by 34.3 %, which corresponds to a CO_2-equivalent of 1939 million tonnes. Alone between 2019 and 2020 the emissions dropped by a CO_2-equivalent of 346 million tonnes [7], also due to the COVID-19 caused lockdowns [8]. In 2021 the EU updated its own climate targets with the *European Climate Law* of 2021. The main goal is to reach climate neutrality for Europe in 2050. The target for GHG-emission reduction by 2030 was set to 55 % compared to 1990 [9]. To find legislative ways to reach the targets by 2030 and 2050 the European Commission is working on documents containing legislative proposals, called *Fit for 55* [10, 11]. The documents contain proposals about topics such as: GHG-emissions, GHG-removals by carbon sinks, fair/just transition, renewable energy, energy efficiency, more alternative fuels and charging station for electric vehicles, energy taxation and carbon border adjustments [10].

To achieve climate neutrality means to reduce the GHG-emission as much as possible and at the same time to compensate remaining emission by means of carbon sinks, such as forests for example [12].

Since 1990 38 % of the decreased European GHG-emissions are attributed to the sector of *Public Electricity and Heat Production*, which is the biggest portion assigned to one single sector [7]. Also, in future this sector, besides the *transport* sector, will give opportunity for the biggest reduction of emission. Considering emissions caused by cars, the target is to only sell zero-emission cars by 2035 and to reduce the GHG-emission caused by cars by 55 % until 2030 compared to 2021 [13].

The share of renewable energies instead should be increased from 22 % in 2021 [14], to 45 % by 2030 following the document *REPowerEU* published on 18 May 2022 to rapidly reduce EU's dependency on

Russian fossil fuels. In this document the expansion of solar power plants is requested from 165 GW (2022) to the doubled power in 2025 and 600 GW by 2030 [15].

According to the EU reference scenario 2020 [16], the share of generated electricity in Europe should change from 2020 to 2050 in the following way: solar energy from 6 % to 18 %; wind energy from 16 % to 40 %; while hydro power and biomass should stay rather constant. While, modern hydro power projects are often connected to complex permitting procedures, limited environmental and social acceptance, long construction periods and therefore higher investment risks [17], the European energy transition clearly relies on solar and wind power the most.

In wind power plants the kinetic energy of moving air is converted into rotational energy via wind turbines. The rotational energy can then be transformed into electrical energy by using a generator, similar as in hydro power. In photovoltaic power plants the solar energy is converted into electrical energy via solar panels. Besides the high volatility and weather-dependency, both methods have another impactful characteristic. Both methods need a special interface, namely an inverter, to be connected to a modern three-phase electric grid efficiently. While wind power plants theoretically could also work without, in solar power plants, the inverter is unavoidable, since the principle, the photovoltaic effect, used in solar panels only delivers DC current. Nowadays also wind power plants rely on power electronics-based inverters [18], combined with either doubly fed induction generators (DFIG) or permanently excited synchronous generators. The wind turbine can then rotate efficiently independently on the grid frequency. The basic task of the inverter is to convert the DC or variable frequency power into a grid-compliant form, such as 50 Hz (e.g. Europe), 60 Hz (e.q. USA) or 16.7 Hz (for some railway applications).

Conventional synchronous generators, as they were used for more than a century, control the terminal voltage directly via their generator excitation and control the output power dependent on the frequency [19]. This generation methodology is well-known and due to its underlying control principle called of type *grid-forming*. Nearly all of today installed inverters in wind or solar power plants although are of the *grid-following* type [19]. In contrast to grid-forming generation sources, the grid-following type always needs an externally controlled grid voltage and can therefore not work stably when not connected to a conventional controlled synchronous generator or modern grid-forming inverter. Grid-following inverters use phase-locked-loops (PLL's) to track the terminal's voltage angle to be able to inject current with a specific phase angle. This way of synchronization not only impedes the operation in island mode, the involvement in restoration processes after blackouts [19], but also leads to an increased risk of loss of synchronism during strong voltage deviation caused by grid faults [20] compared to grids with higher share of conventional synchronous generators.

Although a more sophisticated grid-forming inverter type is subject of many academic publications [21], it is interesting to analyse the currently widespread grid-following inverter and challenges related to its PLL in more detail, since the ongoing energy transition relies to a great extent on this technology.

1.2 Comparable studies

With increasing share of power electronic interfaced renewable energy sources connected to electric grids, the characteristics of those power system change continuously, compared to traditional, synchronous generator-dominated grids. Especially in dynamic behaviour modern grids differ from traditional power grids. Since dynamic behaviour of modern renewable energy sources strongly depends on implemented inverter control strategies, more detailed simulations are necessary to analyse and distinguish probable stability issues [22]. Especially grid-following inverters, with PLL's for synchronization show stability issues under specific circumstances, which can cause severe power and voltage deviations or lead to the tripping of a power plant [22]. Under weak grid situations such issues are generally more probable [23], where the weakness of the grid, in the easiest definition, is inversely proportional to the short circuit power at a specific position. The weaker the grid is, the more sensitive the voltage and phase angle at the inverter's terminal reacts to the injected current [23, 24], which thereupon again increases risk of instability.

In the NERC Reliability Guideline [23], the main stability issues with grid-following inverters in weak grids are explained, examples are shown, and hints are provided for members of the electric utility industry to recognize typical problems and to bypass them via appropriate planning. In this rather practical guideline, although no further details, mathematical relations or clear thresholds about PLL-stability are given.

In more technical publications specific analytical and numerical methods to access stability for inverter's PLL are discussed. To examine stability of the highly non-linear PLL, in multiple publications classical methods are used, that stem from linear control theory, and can therefore only be used for small-signal-analysis after linearization of the model [25].

The most basic approach is to analyse the eigenvalues of the state space model's system matrix after linearization [26, 27]. For simple systems, this is very convenient, although for more complex systems, with a large number of state variables, the setting up of the analytical model can get impractical [28]. Compared to other linear stability assessment methods there is also the disadvantage of the necessity of knowing the whole dynamic model in deep detail, which can be an obstacle, when coming to internal inverter settings, which often are not published by the manufacturer [25].

Another approach is the impedance-based stability method [25, 28, 29]. There by analytical means or by the help of measurements, the input impedance at the interface between grid and inverter or at the interface between different stages of the inverter, e.g. interface to DC-link, is determined for variable frequency. This input impedance can be used to represent the system behaviour in a small-signal model and allows to determine the open-loop transfer function of a closed-loop system. According to the Nyquist criterion, the locus of the open loop transfer function, as well as the information about its potential unstable poles, can be used beneficially in a graphical method to determine the stability of the closed-loop function. This has the very big advantage, that the model must not be known in detail, but measurements can be used instead and can therefore even be used in real-time [30]. By using the Nyquist criterion, not only between stable and unstable models can be distinguished, but the method

can also be used to rate the possible stability, by means of amplitude and phase margins, which can indicate the system's tendency to oscillate [30].

In [31] a method, based on the non-linear PLL-characteristic, is presented, which allows to evaluate if a stable operating point exists during a steady state symmetrical grid-fault for a PLL-synchronized system. It shows that the result is independent of the PLL-settings itself. In [32] this method is extended to unsymmetrical faults, considering coupling of positive and negative sequence.

According to [33] and [34] the previously mentioned linear stability assessment methods are not suited to evaluate severe transient PLL instabilities during and after grid faults, since they cannot represent large signal disturbances. In [33] methods are mentioned that are suited for large-signal modelling, such as time-domain simulations, pseudo trajectory analysis methods and non-linear analytical methods.

The time domain simulation method is the state-of-the-art method to validate simplified or analytical models. In most modern commercial power system analysis and simulation software packages, basic blocks to simulate inverters and its control are available [35, 36, 37]. Depending on the aim of the analysis, the simulation method can be differentiated into phasor domain (RMS-simulation for example for power flow analysis) and transient (EMT-simulation) [38]. Using transient simulation methods, it is even possible to decide if modelling the power electronic-based system as a switched (simulation of switching elements) or a simplified averaged (averaged signals over one switching cycle) model [39]. Due to the accurate modelling of each relevant element, time-domain simulation delivers the most accurate results. The disadvantages although are high computational effort and also the difficulty to isolate specific phenomena related to a single element, when using prebuilt models.

In [24] a pseudo-trajectory method is presented to analyse large-signal disturbances. The relation between injected current, terminal voltage, fault impedance, grid impedance and the PLL system are described by a non-linear differential equation system, which can be solved numerically, while there is typically no possibility to find an analytical solution [40]. The resulting trajectories describe the dynamic behaviour in a graphical intuitive way. Numerical simulations to analyse PLL synchronization issues compared to the nature of synchronous machine synchronization are also covered in [41]. The advantage of such simulations is the possibility to isolate a specific part of the model and to investigate only specific influences. In [42] for example, depending on the equations used, once the non-linearity of the power control loop and once the non-linearity of the PLL is investigated, while considering the opposite loop as constant.

In analytical approaches often the Lyapunov method [33, 43] is used, which enables to analyse the stability of non-linear systems in an analytical way. In this method (often referred as *Lyapunov stability criterion* or the *Direct Method*) a Lyapunov function is searched, which applied to the dynamical problem has to fulfil several conditions to indicate different types of stability. The Lyapunov function has similarities to the potential function in classical dynamics [44] and when found in an appropriate form can be used to determine a domain of attraction [45], which is used to distinguish stable and unstable trajectories of the system. Analytical methods can have clear computational benefits [33], but are on the other hand requesting higher mathematical knowledge and are therefore restricted to more academic environments, in contrast to other methods.

1.3 Prescribed behaviour

As a representative standard in this document, the German VDE-4110 [46] is taken. The standard describes *technical requirements for the connection and operation of customer installations to the medium voltage network*. Besides information about organizational procedures, construction rules and steady state behaviour, it also contains a description of the prescribed behaviour for faulty situations. For feeding power plants, this standard subdivides into type 1 generators (synchronous) and type 2 generators (not synchronous to grid), while in this work focus lies clearly on type 2 plants.

1.3.1 Fault start and end detection

To determine the fault start timing, one of the following criteria is taken:

- **Voltage jump**
  A voltage jump can be understood as a deviation of one of the instantaneous voltage waveforms from a 50-cycle-average waveform by more than 5 % of the nominal peak voltage.
- **RMS-voltage-deviation**
  This criterion is fulfilled when at least one of the phase-to-phase voltages as RMS-value differs by more than 10 % from the nominal voltage.

For the end of fault, the earliest of the following criteria is observed:

- **RMS-voltages again in 10 %-band**
  This criterion is fulfilled when each of the phase-to-phase voltages as RMS-value is back in the ±10 % band around the nominal voltage.
- **Fault time > 5 s**
  This criterion is fulfilled when the fault time exceeds 5 seconds. This does not allow the inverter to trip, but rather stops the reactive current injection demand.

In the following flow chart this logic should be explained graphically.

Thereby the block including z^{-1} indicates a discrete unit-delay, while T_s indicates the sampling time step.

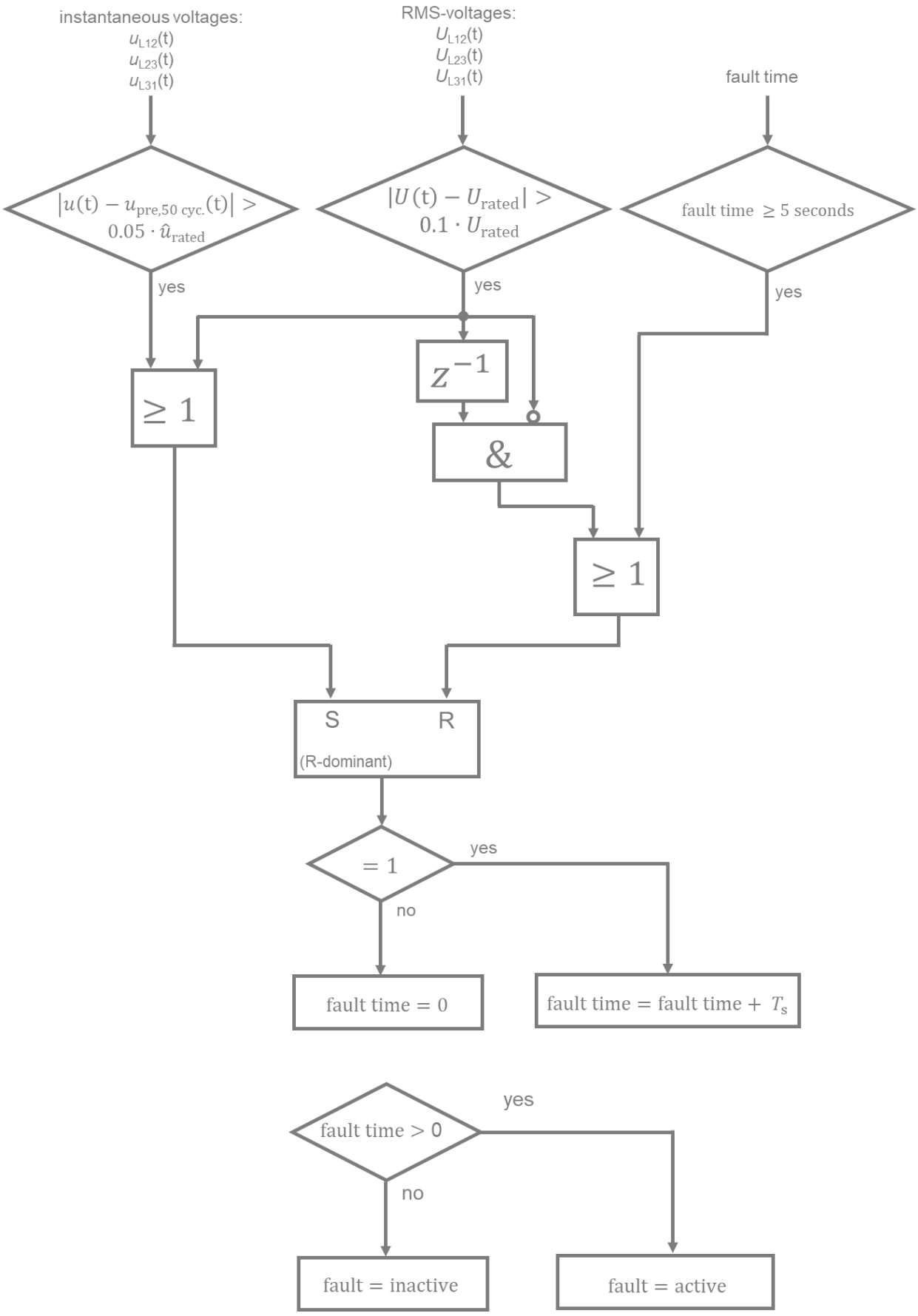

Fig. 1 Fault start and end detection logic (VDE-4110)

1.3.2 Fault ride through logic

To avoid the tripping of multiple power plants during faults and the associated risk of a major grid instability, fault ride through ('FRT') curves are introduced. The FRT-curves are time-voltage curves, which define when an inverter is allowed to trip during a fault.

In the relevant curves form VDE-4110 are shown in Fig. 2

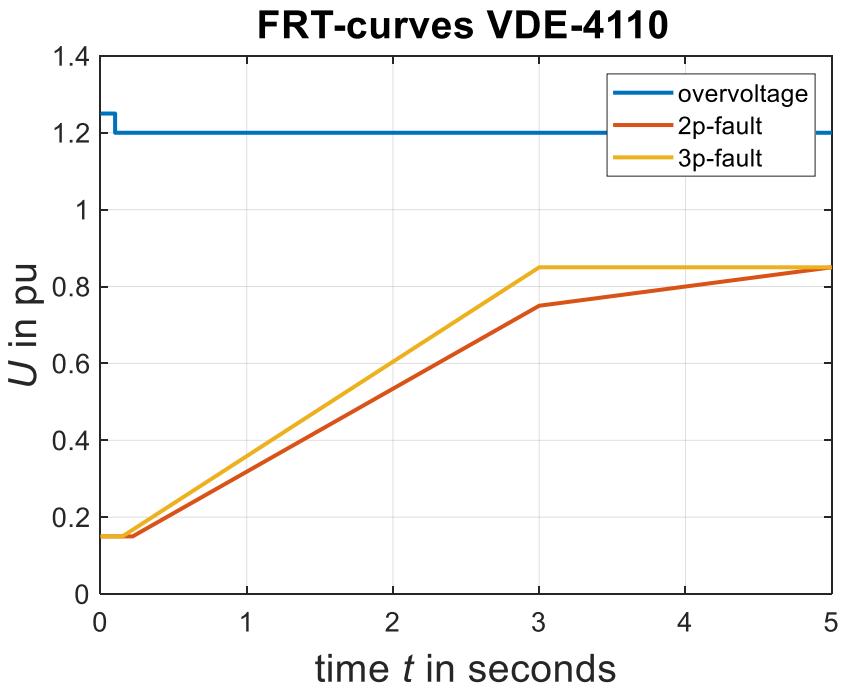

Fig. 2 FRT curves (VDE-4110)

If all RMS-phase-to-phase voltages lie between the upper overvoltage line and one of the lower voltage lines (depending on fault type) no trip is allowed.

As an example, two situations should be shown, where only one of those would allow a trip after a specific time.

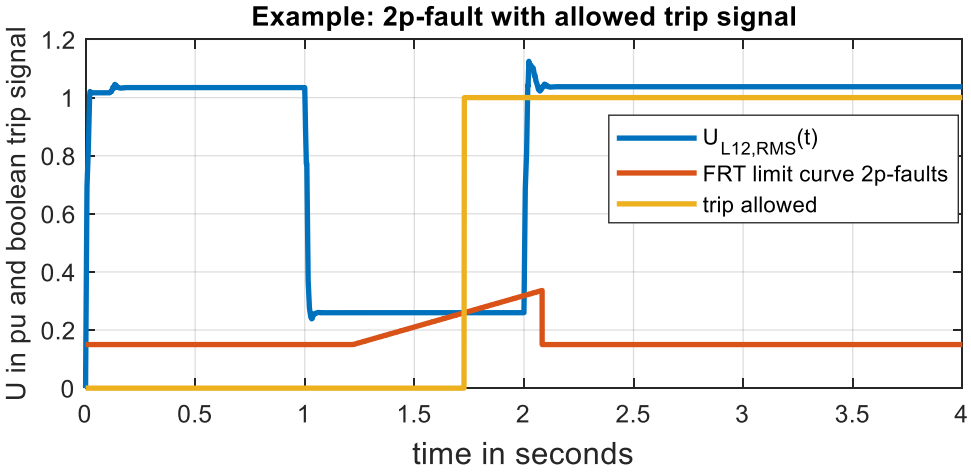

Fig. 3 FRT example: trip allowed

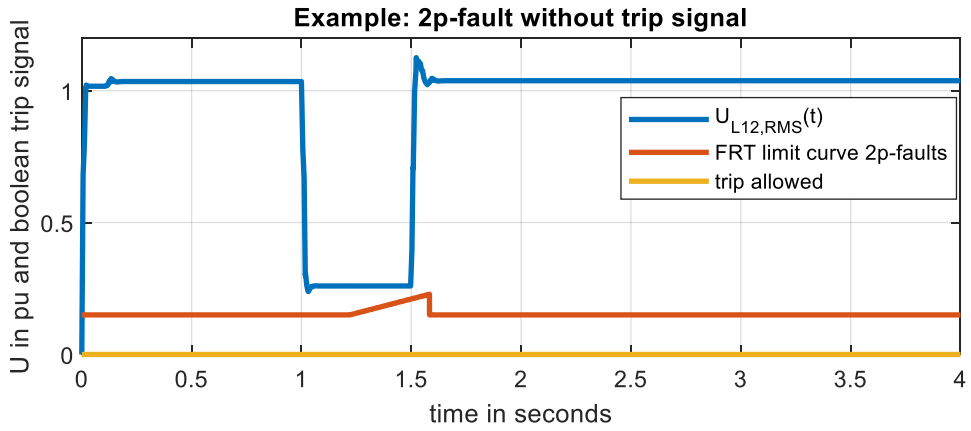

Fig. 4 FRT example: no trip allowed

In both cases the same phase-to-phase fault between L1 and L2 is simulated. In the first example, the fault duration is long enough, to cause the minimum RMS-voltage to cut the lower FRT-limit, which ends in an allowed trip. In the second example, the fault duration is shorter and therefore the FRT situation ends without trip.

1.3.3 Additional reactive current injection

During faults additional reactive current injection in positive and negative sequence is mandatory. The amount of additional current is depending on the difference between the sequence voltages during and before the fault. The injected reactive current components should act against the voltage deviation caused by the fault.

In VDE-4110 the following characteristic is shown: (the same is valid for negative sequence)

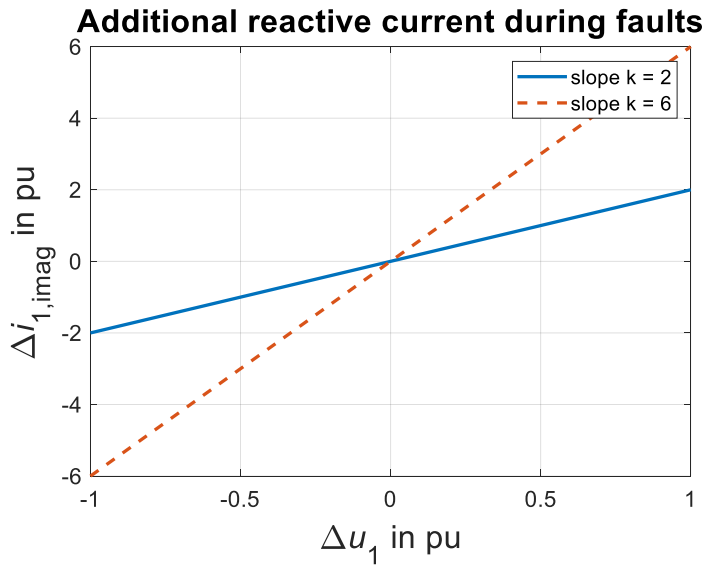

Fig. 5 Characteristic of additional reactive current and voltage deviation

The ratio *k* describes the relation between voltage deviation and additional current and can be varied between 2 and 6. To assure the maximum reactive current possible, during faults the injected active current can be reduced if otherwise the total injected current exceeds the maximum possible current.

In 2.3 a detailed description of the implementation of this request can be found.

1.4 Overview of the research in this work

In this work an existing averaged three-phase inverter model, created by Dr. Zhang at IEAN of TU Graz in Simulink, should be analysed. In addition, the model should be adapted to specific requirements of the German standard (VDE-4110, detailed in chapter 1.3), which is the standard defining technical connection rules to the medium-voltage grid. Since the final result of the model should be used as a basis for an inverter model in a commercial system-based protection testing software, especially fault relevant requests from the standards are of interest. Those include:

- Fault start and end detection
- Fault ride through mode
- Additional reactive current injection during faults

The research focus of this work includes the analysis of the phase locked loop (PLL) implemented in the model and its behaviour in dependency of different grid configurations.

Therefore, this work has the following structure:

In chapter 2 an overview about the implemented model should be given. Special attention should be paid to control logics, such as the PLL, sequence-decoupling, current-limiting, current reference determination and fault detection.

Chapter 3 should provide a mathematical comparison between classical symmetrical components (used in definitions of standard) and the signals in dq-domain used in the control block of the model.

Chapter 4 should supply detailed observations about the behaviour of the PLL under different situations, such as: start-up, fault-situations, and after-fault-situations. The stability in those situations should be investigated and the main influence factors distinguished. To analyse the stability during symmetrical faults the method explained in [31, 47] is applied and validated by simulations and its practicability tested. Furthermore, to investigate transient/dynamic PLL-stability a similar method as in [34] is used, to describe the dynamic behaviour for symmetrical faults and domain of attraction plots are generated, to achieve similar results as in [33], although with a much simpler mathematical approach.

In chapter 5 a concluding simulation example should be shown, in which to describe the specific behaviour, the in previously chapters explained phenomena, are recovered. The model used in the example, represents a typical wind park connected to the resonant grounded 110 kV-grid.

2 Inverter model description

2.1 Conventional grid-following inverter structure

The hardware of a conventional two-level three-phase inverter consists typically of a DC-circuit part, containing a DC-link capacitor, and a bridge consisting of three half-bridges, made up of six switching elements. A control logic determines the signals to operate the switches in such a way to achieve the demanded voltage at the bridge output. For a two-level voltage source inverter this circuitry should be shown schematically.

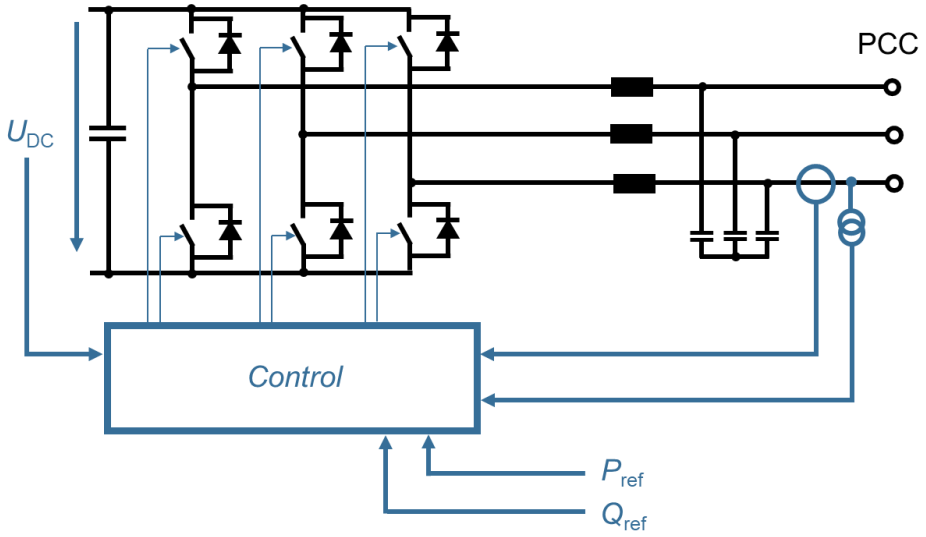

Fig. 6 Typical structure of a grid-following inverter

In real life, a variety of three-phase inverter circuitries are available with specific advantages and drawbacks. Also, in contrast to voltage source inverters (VSI), DC-current-stiff systems (current source inverters) are available [48], but are not considered in this work.

By measuring PCC-voltages and -currents, as well as the DC-link voltage, the inverter control determines the requested current to achieve the requested reference power flow into the grid. The basic inner control structure can be seen in Fig. 7. In this representation only a positive sequence control is shown, based on dq-domain, which is explained later. For completeness it must be mentioned that there exist also control types, which work without dq-transformation, but instead with Clarke-components in connection with resonant or hysteresis controllers for example [49].

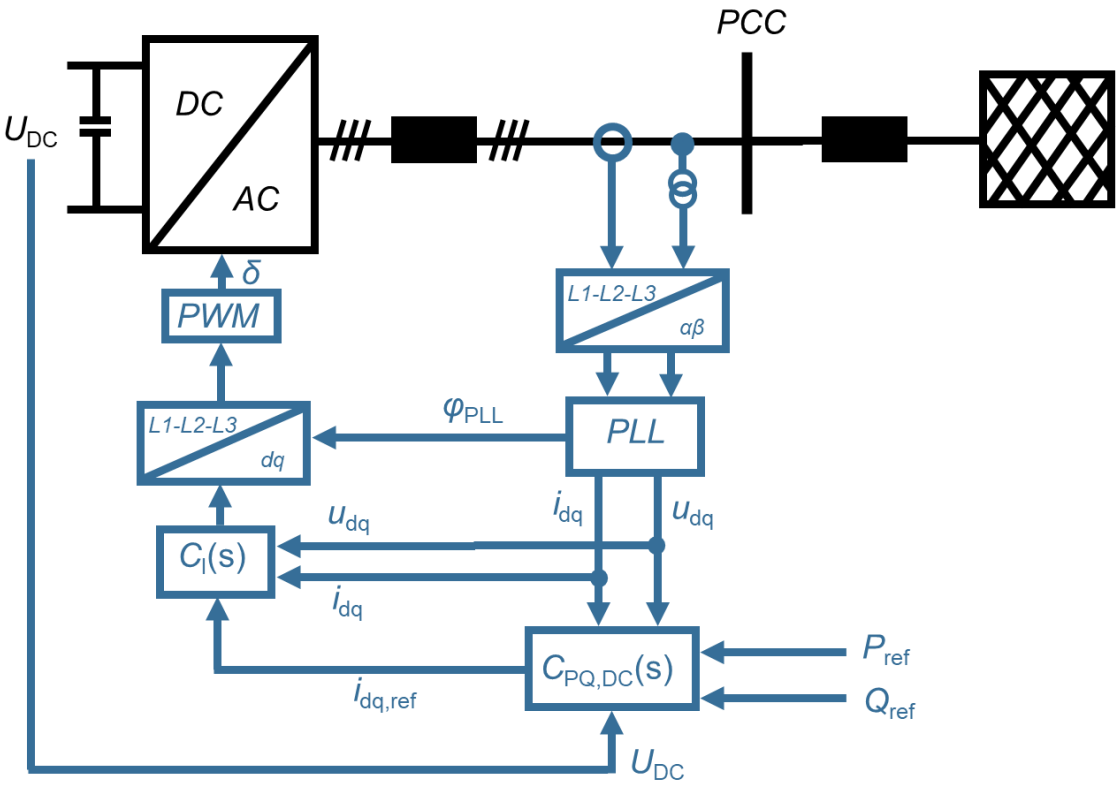

Fig. 7 Typical control structure of grid-following inverter (positive sequence)

In this basic control structure, the measured terminal voltages and currents are transferred into dq-domain, by extracting the voltage phase angle through a PLL. In a power and DC-link voltage control loop ($C_{PQ,DC}$), a reference dq-current is calculated depending on the current output power, the reference power and the DC-link voltage, which can be understood as an indicator of the balance between DC input power (from the energy source) and the output power. In a current control loop (C_I) depending on the measured current and voltage and the reference current a voltage is calculated, which if generated by the bridge, leads to a current flow with the value of the reference current. The generation of the requested voltage by the bridge can be realized through a pulse width modulated (PWM) high frequency signal driving the bridge elements. Also here, different realization topologies exist, but are not discussed in this work.

2.2 Simplified model

When observing Fig. 7 it is clear, that both, the current and the power control in dq-domain, strongly depend on a stable dq-transformation, hence a stable PLL-behaviour, which makes the PLL to a crucial element in this type of control. When focusing just on PLL-behaviour, the model can further be simplified, due to the following reasons. The current-control is normally tuned to have much smaller time-constants, compared to the PLL [33, 34] and can therefore be assumed to work properly when discussing relative slow synchronization problems. This assumed ideal current controller, in combination with an ideal bridge and ideal filtering can be replaced by a controlled current source. In addition, the outer power and DC-link control loop can be assumed to remain constant during the interesting critical stability situations, due to the large time constants of the feeding energy source [33]. With these simplifications two control loops are eliminated and the structure for a positive sequence control can be reduced clearly.

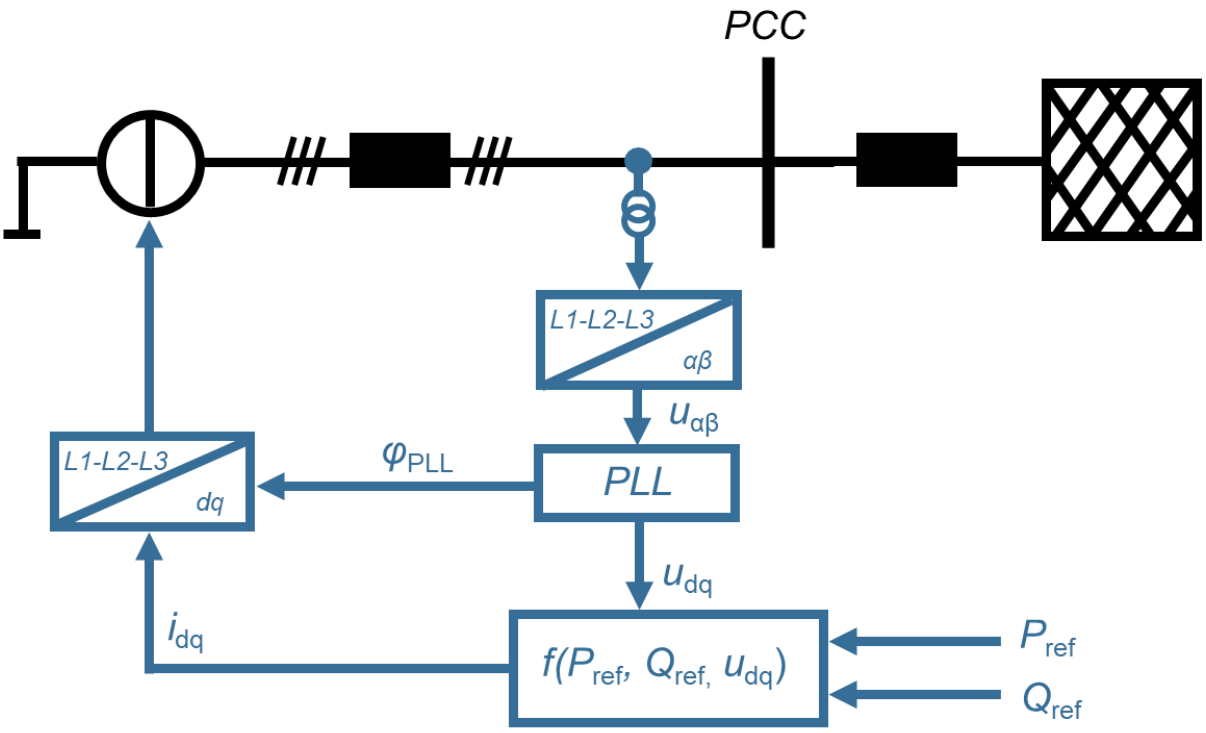

Fig. 8 Simplified control structure (positive sequence)

Although, to meet specific requirements (standard compliance, hardware-limits, etc.) some additional elements, such as fault detection, current limiting and a negative sequence control must be added, which leads to the final structure, used in this work.

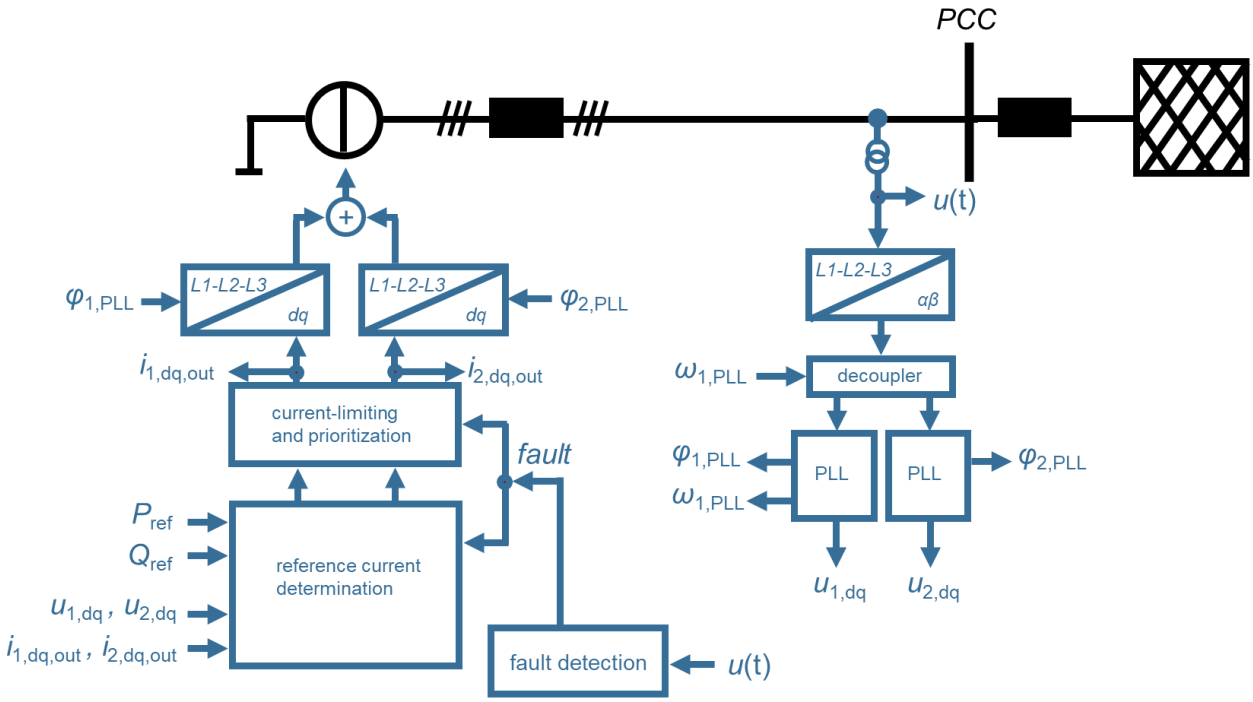

Fig. 9 Complete control structure

The decoupler is used to split the measured voltages into positive and negative sequence components, which is necessary since modern standards (e.g. VDE-4110) requests also negative sequence control during faults. In addition, without the decoupling the PLL could not work properly, when fed with a negative sequence containing voltage, which to a certain extent is normal especially for distribution grids [50].

The fault detection block, determines if the inverter, must switch into fault operating mode, which changes the method to calculate the reference current, as well as the current prioritization.

As, explained later in detail, the current limiting is necessary to prevent currents in ranges harmful for the switching elements.

In chapter 2.3 the blocks of Fig. 9 Complete control structure are explained in more detail.

2.3 Control

In the control block itself the first action, is a transformation of the measured voltages into per unit (p.u.) values, where rated peak values are taken as reference values. This simplifies scaling the model to other power and voltage levels. Due to the normally high zero-sequence impedance path between inverters and the grid, due to delta transformers, the zero-sequence voltage can be neglected in the PCC voltage. For this reason, the three-phase voltage system is fully described by two values, for example by one complex space vector $\underline{u}$ or its real and imaginary part u_α *and* u_β, which can be achieved when applying the Clarke-transformation onto the three time-dependent voltage signals.

For a first explanation, a symmetrical voltage system is assumed.

After transformation into the orthogonal αβ-frame, the signals are fed to a phase locked loop (PLL) containing block, which transforms the measurement data to a rotating frame, which leads to constant values in steady state operation. For a purely symmetrical voltage set, this would work like depicted in the following illustrations.

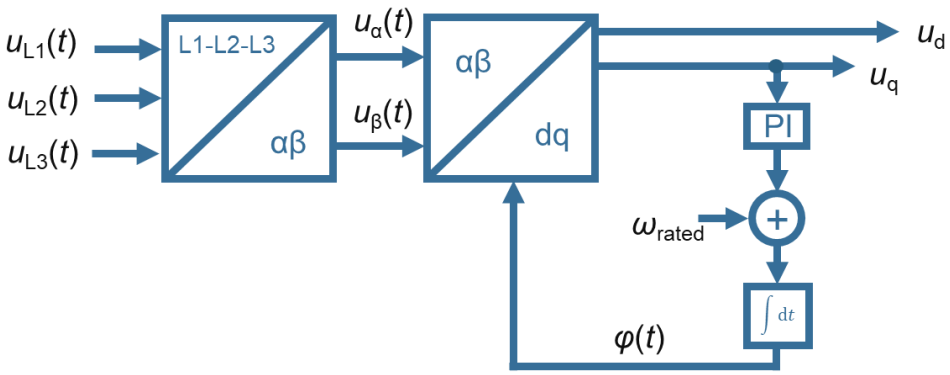

Fig. 10 Clarke transformation and synchronous reference frame PLL (SRF-PLL)

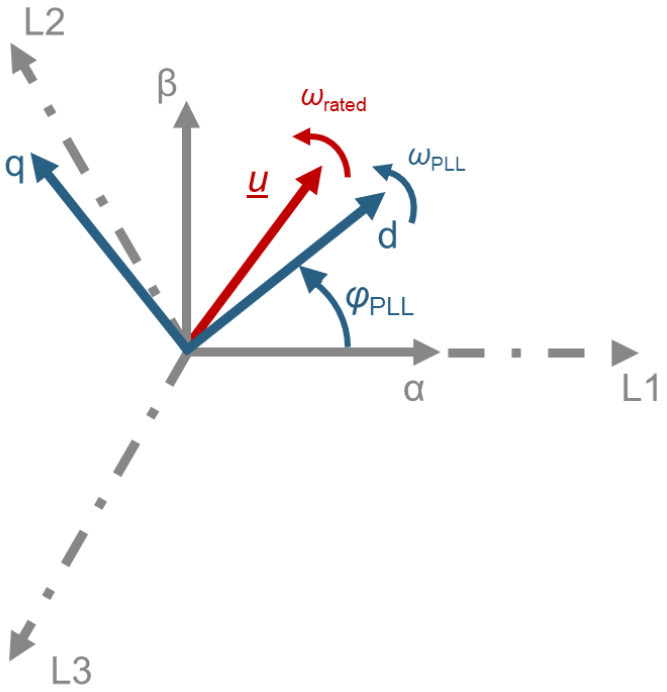

Fig. 11 Relevant stationary and rotating reference frames

The complex space vector $\underline{u}$ rotates with rated frequency and its angle in the stationary αβ-frame changes therefore over time. Via the dq-transformation the complex vector is transferred into the rotating dq-frame, which in steady state also rotates with rated frequency and the vector can therefore be represented through two constant values in dq-domain, which simplifies control.

In steady state the dq-frame should not only rotate as fast as the space vector $\underline{u}$, but the d-axis (dependent on definition also q-axis is possible) should be locked with the space vector, causing the q-component to be zero. This is for a symmetrical voltage set theoretically always possible, since the voltage set is uniquely defined by two values ($u_d(t)$ and $\varphi_{PLL}(t)$), using the degree of freedom to set u_q to zero. To achieve the locking of the d-axis with the space vector, the PLL is used, which controller varies the frequency $\omega_{PLL}(t)$ and hence it's integral $\varphi_{PLL}(t)$ until u_q is zero. The current value of $u_q(t)$ can be interpreted as an indicator, of how much the instantaneous angle is off the optimum one. The controller tuning of the PLL is explained in 2.4.

But since the inverter model should be designed to operate even in unbalanced situations, such as asymmetrical grid faults, before feeding the voltage to the PLL, it must be split into positive and negative sequence. Otherwise, the trajectory of the computed space vector does not rotate in form of a circle, which makes tracking hard.

It can be assumed the phase voltages have the following structure:

$$\begin{bmatrix} u_{L1}(t) \\ u_{L2}(t) \\ u_{L3}(t) \end{bmatrix} = \hat{u}_1 \cdot \begin{bmatrix} \cos(\omega t + \varphi_1) \\ \cos(\omega t + \varphi_1 - {}^{2\pi}/_{3}) \\ \cos(\omega t + \varphi_1 + {}^{2\pi}/_{3}) \end{bmatrix} + \hat{u}_2 \cdot \begin{bmatrix} \cos(\omega t - \varphi_2) \\ \cos(\omega t - \varphi_2 + {}^{2\pi}/_{3}) \\ \cos(\omega t - \varphi_2 - {}^{2\pi}/_{3}) \end{bmatrix} \quad (1)$$

$\hat{u}_1$ and $\hat{u}_2$ denote the amplitude in positive and negative sequence respectively, while φ_1 and φ_2 are the respective phase angles.

The first step is to transform the three time-varying signals into a space vector, whose components are the αβ-components.

$$\begin{bmatrix} u_\alpha(t) \\ u_\beta(t) \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} u_{L1}(t) \\ u_{L2}(t) \\ u_{L3}(t) \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} u_\alpha(t) \\ u_\beta(t) \end{bmatrix} = \hat{u}_1 \cdot \begin{bmatrix} \cos(\omega t + \varphi_1) \\ \sin(\omega t + \varphi_1) \end{bmatrix} + \hat{u}_2 \cdot \begin{bmatrix} \cos(-\omega t + \varphi_2) \\ \sin(-\omega t + \varphi_2) \end{bmatrix} \tag{3}$$

Since positive and negative sequence differ in the sign of the frequency defining variable, different mathematical methods are possible to split the Clarke components into a set for positive and one for negative sequence. In this case the use of a quadrature signal generator (QSG, delays signals by 90°) was chosen, to achieve this. More accurately this block is based on a block known under the name of *second order generalised integrator (SOGI)* [48] and is shown in Fig. 12.

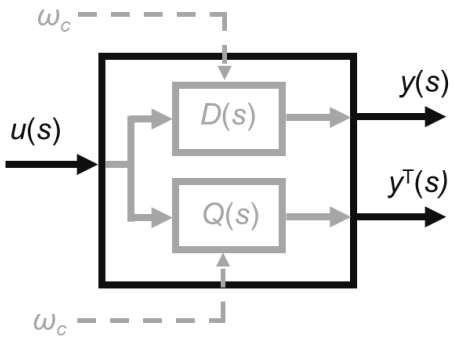

Fig. 12 Quadrature signal generator based on SOGI

The two (direct and quadrature) signal paths can be described by the following transfer functions, which are based on typical resonant controller structure:

$$D(s) = \frac{k\omega_c s}{s^2 + k\omega_c s + \omega_c^2} \tag{4}$$

$$Q(s) = \frac{k\omega_c^2}{s^2 + k\omega_c s + \omega_c^2} \tag{5}$$

A very common structure [51, 48] to achieve this behaviour is shown in Fig. 13.

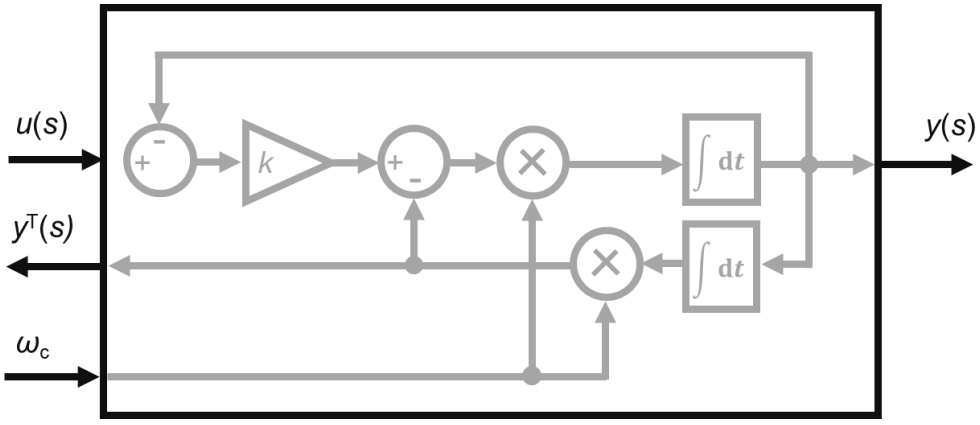

Fig. 13 realization of quadrature signal generator

The factor k is normally chosen to be $\sqrt{2}$. By changing k, the transient behaviour (bandwidth) can be varied.

The two transfer functions have the following frequency dependent behaviour:

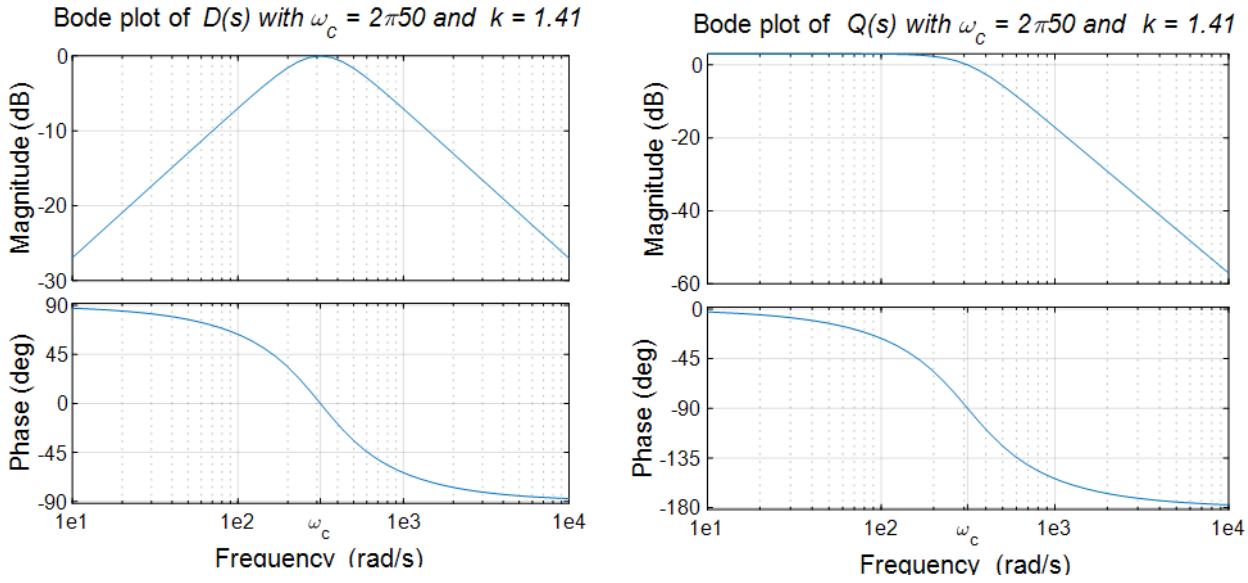

Fig. 14 Bode plots of DSOGI transfer functions

As it can be deduced from the bode plots, for ω_c, $D(s)$ conducts the input signal with no attenuation and no phase shift, while $Q(s)$ causes a phase shift of -90° at ω_c. When ω_c equals the frequency of the input signal $u(t)$, then $y(t)$ equals $u(t)$ and $y(t)^T$ is the 90°-delayed version of $u(t)$.

In discrete implementation it must be assured that both signal paths cause equal delays, to achieve accurate orthogonality.

The phase-shifted signals have then the following structure:

$$\begin{bmatrix} u_\alpha^T(t) \\ u_\beta^T(t) \end{bmatrix} = \hat{u}_1 \cdot \begin{bmatrix} \sin(\omega t + \varphi_1) \\ -\cos(\omega t + \varphi_1) \end{bmatrix} + \hat{u}_2 \cdot \begin{bmatrix} -\sin(-\omega t + \varphi_2) \\ \cos(-\omega t + \varphi_2) \end{bmatrix} \quad (6)$$

By adding the two sets of alpha-beta components in an appropriate matter, splitting into positive and negative sequence is achieved.

$$\begin{bmatrix} u_{1\alpha}(t) \\ u_{2\alpha}(t) \\ u_{1\beta}(t) \\ u_{2\beta}(t) \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} u_{\alpha}(t) - u_{\beta}^{\mathrm{T}}(t) \\ u_{\alpha}(t) + u_{\beta}^{\mathrm{T}}(t) \\ u_{\alpha}^{\mathrm{T}}(t) + u_{\beta}(t) \\ -u_{\alpha}^{\mathrm{T}}(t) + u_{\beta}(t) \end{bmatrix} = \begin{bmatrix} \hat{u}_1 \cdot \cos(\omega t + \varphi_1) \\ \hat{u}_2 \cdot \cos(-\omega t + \varphi_2) \\ \hat{u}_1 \cdot \sin(\omega t + \varphi_1) \\ \hat{u}_2 \cdot \sin(-\omega t + \varphi_2) \end{bmatrix} \tag{7}$$

By adding an SRF-PLL for each of the αβ-voltage sets, the following complete structure can be created.

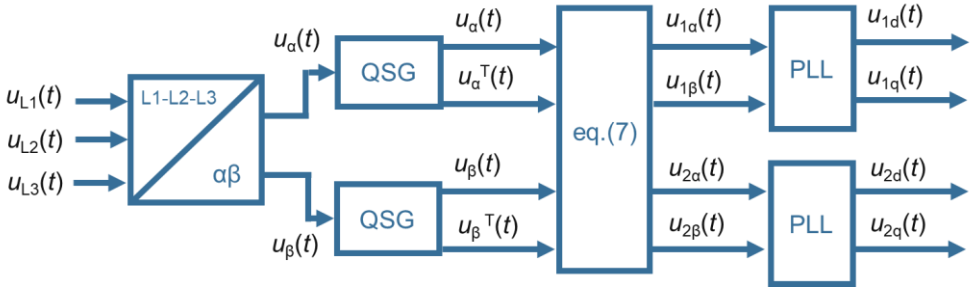

Fig. 15 Complete transformation structure

When having computed the dq-components for grid voltage, as a next step the calculation for the reference current can be carried out. Since, according to VDE-4110, power control is only necessary during mostly symmetrical healthy grid situations, for the computation of the reference for healthy grid situations current negative sequence system can be neglected.

Instantaneous power calculation in per unit system works as follows: (it is assumed that voltage and current base values are the nominal peak values)

$$p(t) = \frac{2}{3} \cdot [u_{\mathrm{L1}}(t) \cdot i_{\mathrm{L1}}(t) + u_{\mathrm{L2}}(t) \cdot i_{\mathrm{L2}}(t) + u_{\mathrm{L3}}(t) \cdot i_{\mathrm{L3}}(t)] \tag{8}$$

$$q(t) = \frac{2}{3} \cdot \frac{1}{\sqrt{3}} \cdot [(u_{\mathrm{L2}}(t) - u_{\mathrm{L3}}(t)) \cdot i_{\mathrm{L1}}(t) + (u_{\mathrm{L3}}(t) - u_{\mathrm{L1}}(t)) \cdot i_{\mathrm{L2}}(t) + (u_{\mathrm{L1}}(t) - u_{\mathrm{L2}}(t)) \cdot i_{\mathrm{L3}}(t)] \tag{9}$$

For healthy grid situations the instantaneous voltages and currents in (8) and (9) can be replaced by its positive sequence dq-domain representants, as shown in (10) and explained in more detail in later chapters. By applying (10) to (8) and (9), (11) can be obtained.

$$\begin{bmatrix} u_{1\mathrm{d}}(t) \\ u_{1\mathrm{q}}(t) \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} \cos(\varphi_{1,\mathrm{PLL}}) & \cos(\varphi_{1,\mathrm{PLL}} - {}^{2\pi}/_{3}) & \cos(\varphi_{1,\mathrm{PLL}} - {}^{4\pi}/_{3}) \\ -\sin(\varphi_{1,\mathrm{PLL}}) & -\sin(\varphi_{1,\mathrm{PLL}} - {}^{2\pi}/_{3}) & -\sin(\varphi_{1,\mathrm{PLL}} - {}^{4\pi}/_{3}) \end{bmatrix} \cdot \begin{bmatrix} u_{\mathrm{L1}}(t) \\ u_{\mathrm{L2}}(t) \\ u_{\mathrm{L3}}(t) \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} p(t) \\ q(t) \end{bmatrix} = \begin{bmatrix} u_{1\mathrm{d}}(t) & u_{1\mathrm{q}}(t) \\ u_{1\mathrm{q}}(t) & -u_{1\mathrm{d}}(t) \end{bmatrix} \cdot \begin{bmatrix} i_{1\mathrm{d}}(t) \\ i_{1\mathrm{q}}(t) \end{bmatrix} \tag{11}$$

To obtain the reference currents, dependent on given reference power and measured and transformed voltages, the relation of (11) is used. The voltage matrix from (11) is inverted and multiplied with the reference power values, as shown in (12).

$$\begin{bmatrix} i_{1\mathrm{d,ref}}(t) \\ i_{1\mathrm{q,ref}}(t) \end{bmatrix} = \frac{1}{u_{1\mathrm{d}}^2(t) + u_{1\mathrm{q}}^2(t)} \cdot \begin{bmatrix} u_{1\mathrm{d}}(t) & u_{1\mathrm{q}}(t) \\ u_{1\mathrm{q}}(t) & -u_{1\mathrm{d}}(t) \end{bmatrix} \cdot \begin{bmatrix} P_{\mathrm{ref}} \\ Q_{\mathrm{ref}} \end{bmatrix} \tag{12}$$

The reference current calculation works like this in healthy grid situations. During faults, as already mentioned, a specific amount of reactive current (in positive and negative sequence) must be injected in addition to the pre fault reactive injection current. The additional reactive current is dependent on the deviation of the actual sequence voltage from the pre fault voltage. Therefore, pre fault values must be saved and held constant during faults. Since in this simulation model faults happen at user defined times, this can be used beneficially, by saving the pre fault values at a fixed time step before the fault start. The additional reactive currents in positive and negative sequence are then determined as follows:

$$\begin{bmatrix} \Delta i_{1\mathrm{q,ref}}(t) \\ \Delta i_{2\mathrm{q,ref}}(t) \end{bmatrix} = k \cdot \begin{bmatrix} |u_1| - |u_{1,\mathrm{pre}}| \\ |u_2| - |u_{2,\mathrm{pre}}| \end{bmatrix} \tag{13}$$

The relation between dq-values and active and reactive parts of symmetrical component currents, is explained in 0.

The magnitudes of the positive and negative sequence voltages used in (13) are calculated, as shown in (14).

$$\begin{bmatrix} |u_1| \\ |u_2| \end{bmatrix} = \begin{bmatrix} \sqrt{{u_{1\mathrm{d}}}^2 + {u_{1\mathrm{q}}}^2} \\ \sqrt{{u_{2\mathrm{d}}}^2 + {u_{2\mathrm{q}}}^2} \end{bmatrix} \tag{14}$$

In contrast to traditional synchronous generators, power electronics-based infeeds have a much smaller over-current capability. Therefore, the exceeding of the maximum current must strictly be avoided. In this model, the current limitation is implemented in the following way:

The maximum current is set to 1.2 pu. In healthy grid situations, the whole available current can be used for positive sequence current. In a faulty situation, where some standards (e.g. VDE-4110) demand reactive current injection in positive and negative sequence system, the current limitation must be adapted. In this model, the maximum available current i_{max} is split into a positive and into a negative sequence part. The ratio between the maximum available current in positive and negative sequence is set proportional to the associated sequence voltage deviation.

$$i_{1,\mathrm{max}} = i_{\mathrm{max}} \cdot \frac{|\Delta u_1|}{|\Delta u_1| + |\Delta u_2|} \tag{15}$$

$$i_{2,\mathrm{max}} = i_{\mathrm{max}} \cdot \frac{|\Delta u_2|}{|\Delta u_1| + |\Delta u_2|} \tag{16}$$

Since positive and negative sequence currents may have different phase angles, although are added in this logic algebraically, this logic may not lead to the best utilisation of the available current. Although it is a safe method to assure the current not getting too high.

In addition, in the current limiting logic also a prioritization logic between active and reactive current is implemented. During healthy grid situations active current is prioritized, while during faults reactive

current has priority. This means, during faults when the reference current exceeds the maximum current, active current is reduced first.

At the output of the block, which computes the reference current in dq-domain a low-pass filter of second order with a default cut-off frequency of 25 Hz is used. This is necessary, when dealing with current sources. The possibly high rates of change in the output current would cause overvoltages due to inductive elements in the grid, which must be avoided.

2.4 PLL controller tuning [51]

As already mentioned, to transform the two αβ-component sets into dq-components, a phase locked loop is used. In this chapter some further details should be supplied.

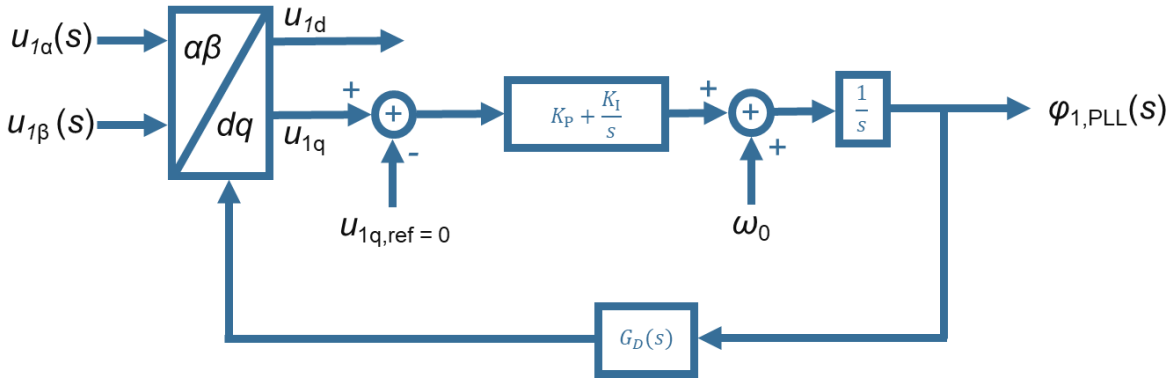

Fig. 16 Three-phase PLL structure (only positive sequence demonstrated)

The instantaneous q-component of the voltage is compared against its reference value of zero. The error is fed to a PI-controller, which's output indicates if the d-frame has to "accelerate" or "deaccelerate" to lock with the space vector. After adding the nominal frequency, and integrating, the output is the current PLL-angle. The computed angle is fed back to the αβ-dq-transformation block. In the feedback path a delay block is inserted, which in digital domain avoids an algebraic loop and can be approximated by the transfer function in (17).

$$G_D(s) = \frac{1}{s \cdot T_s + 1} \tag{17}$$

With T_s as the simulation step width of 0.1 ms at 10 kHz simulation frequency.

To get u_{1q} from *αβ*-components a multiplication with a rotation matrix is necessary:

$$\begin{bmatrix} u_{1d} \\ u_{1q} \end{bmatrix} = \begin{bmatrix} \cos(\varphi_{1,PLL}) & \sin(\varphi_{1,PLL}) \\ -\sin(\varphi_{1,PLL}) & \cos(\varphi_{1,PLL}) \end{bmatrix} \cdot \begin{bmatrix} u_{1\alpha} \\ u_{1\beta} \end{bmatrix} \tag{18}$$

For the q-component therefore (19) is valid.

$$u_{1q} = -\sin(\varphi_{1,PLL}) \cdot u_{1\alpha} + \cos(\varphi_{1,PLL}) \cdot u_{1\beta} \tag{19}$$

From a previous chapter, the following is known:

$$\begin{bmatrix} u_{1\alpha} \\ u_{1\beta} \end{bmatrix} = \hat{u}_1 \begin{bmatrix} \cos(\omega t + \varphi_1) \\ \sin(\omega t + \varphi_1) \end{bmatrix} \tag{20}$$

This then leads to:

$$u_{1q} = \hat{u}_1 \cdot \sin(-\varphi_{1,PLL}) \cdot \cos(\omega t + \varphi_1) + \hat{u}_1 \cdot \cos(\varphi_{1,PLL}) \cdot \sin(\omega t + \varphi_1) \tag{21}$$

Which equals:

$$u_{1q} = \hat{u}_1 \cdot \sin(\omega t + \varphi_1 - \varphi_{1,PLL}) \tag{22}$$

Since during healthy operation $\omega t+\varphi_1$ is close to $\varphi_{1,\mathrm{PLL}}$, for control purposes, a linearisation around this stable operating point is permitted. To derive the small-signal model, the argument in the sin-function of (22) is substituted.

$$x = \omega t + \varphi_1 - \varphi_{1,\mathrm{PLL}} \tag{23}$$

$$u_{1\mathrm{q}}(x) = \hat{u}_1 \cdot \sin(x) \tag{24}$$

The linearisation should be done around the operating point x_0.

$$x_0 = 0 \tag{25}$$

$$u_{1\mathrm{q}}(x) \sim \underbrace{u_{1\mathrm{q}}(x_0)}_{=0} + \underbrace{\frac{\mathrm{d}u_{1\mathrm{q}}(x)}{\mathrm{d}x}}_{at\ x_0} \cdot x \tag{26}$$

$$\underbrace{\frac{\mathrm{d}u_{1\mathrm{q}}(x)}{\mathrm{d}x}}_{at\ x_0} = \hat{u}_1 \cdot \underbrace{\cos(\underbrace{x_0}_{=0})}_{=1} = \hat{u}_1 \tag{27}$$

$$u_{1\mathrm{q}}(x) \sim \hat{u}_1 \cdot x \tag{28}$$

Inserting the original argument:

$$u_{1\mathrm{q}} = \hat{u}_1 \cdot (\omega t + \varphi_1 - \varphi_{1,\mathrm{PLL}}) \tag{29}$$

To denote the small-signal characteristic around the operating point with value 0, the Δ-prefix is used, and another substitution is done:

$$\varphi_{\mathrm{G}} = \omega t + \varphi_1 \tag{30}$$

$$\Delta u_{1\mathrm{q}} = \hat{u}_1 \cdot (\Delta\varphi_{\mathrm{G}} - \Delta\varphi_{1,\mathrm{PLL}}) \tag{31}$$

From this simplification, the small signal model can be obtained:

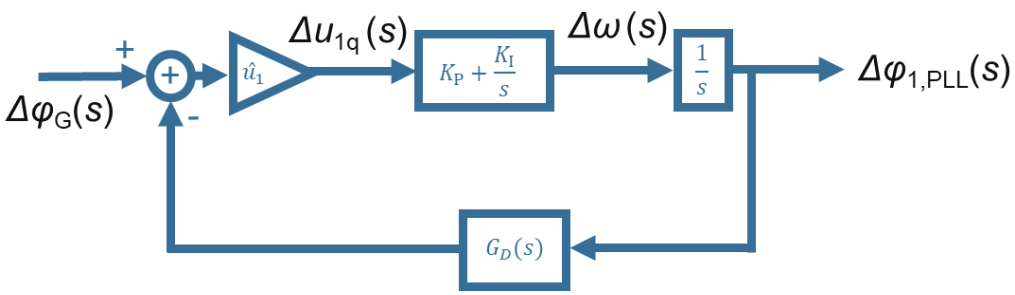

Fig. 17 Small signal model of PLL

The open loop transfer function, which is necessary for the controller parameter tuning method, is:

$$G_{\mathrm{ol}}(s) = \hat{u}_1 \cdot \left(K_{\mathrm{P}} + \frac{K_{\mathrm{I}}}{s}\right) \cdot \frac{1}{s} \cdot \frac{1}{(s \cdot T_{\mathrm{s}} + 1)} \tag{32}$$

In general, this is a transfer function of the following structure:

$$T(s) = \frac{\omega_{\mathrm{c}}}{s} \cdot \frac{\omega_1 + s}{s} \cdot \frac{\omega_2}{\omega_2 + s} \tag{33}$$

According to the common 'symmetrical optimum' tuning method, the following relations between the frequencies should apply:

$$h = \frac{\omega_2}{\omega_1} \tag{34}$$

$$\omega_c = \sqrt{h} \cdot \omega_1 \tag{35}$$

If these demands are met, the bode diagram of the transfer function has the following look:

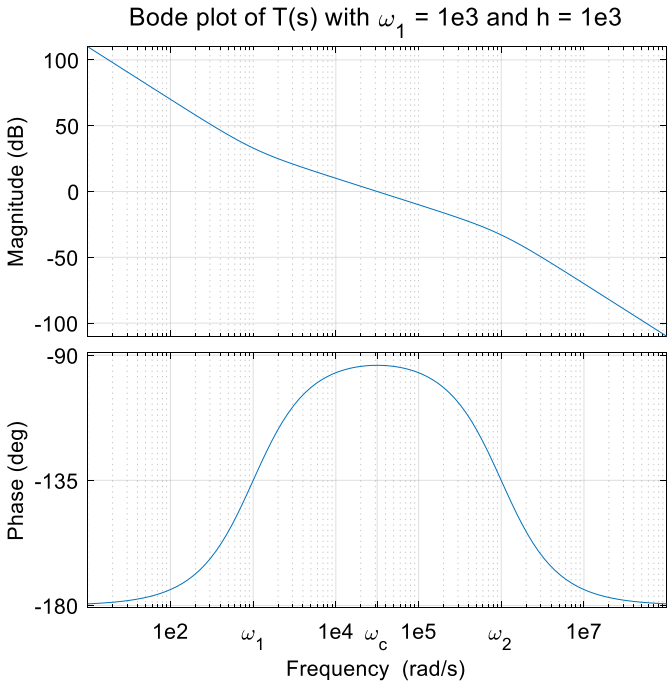

Fig. 18 Bode diagram of transfer function (symmetrical optimum method)

The use of the symmetrical optimum method assures a symmetrical phase behaviour around the center-frequency ω_c, as well as a maximum phase margin at ω_c, which is an indication for stability at the corresponding frequency.

With the use of and (34) and (35), *T(s)* can be rearranged:

$$T(s) = \frac{\omega_{\mathrm{c}}}{s} \cdot \frac{\frac{\omega_c}{\sqrt{h}} + s}{s} \cdot \frac{\omega_c \cdot \sqrt{h}}{\omega_c \cdot \sqrt{h} + s} = \frac{{\omega_{\mathrm{c}}}^2 \cdot \sqrt{h} \cdot \left(\frac{\omega_c}{\sqrt{h}} + s\right)}{s^2 \cdot \left(\sqrt{h} \cdot \omega_{\mathrm{c}} + s\right)} \tag{36}$$

Equation (32) can be brought into a similar form as (36):

$$G_{\mathrm{ol}}(s) = (K_{\mathrm{P}} \cdot s + K_{\mathrm{I}}) \cdot \frac{\hat{u}_1}{s^2} \cdot \frac{1}{(s \cdot T_{\mathrm{s}} + 1)} = \frac{\hat{u}_1 \cdot K_{\mathrm{P}}}{s^2} \cdot \frac{s + \frac{K_{\mathrm{I}}}{K_{\mathrm{P}}}}{T_{\mathrm{s}} \cdot \left(s + \frac{1}{T_{\mathrm{s}}}\right)} \tag{37}$$

Comparing (37) with (36), leads to:

$$\frac{\hat{u}_1 \cdot K_{\mathrm{P}}}{T_{\mathrm{s}}} = {\omega_{\mathrm{c}}}^2 \cdot \sqrt{h} \tag{38}$$

$$\frac{\omega_c}{\sqrt{h}} = \frac{K_{\mathrm{I}}}{K_{\mathrm{P}}} \tag{39}$$

$$\sqrt{h} \cdot \omega_{\mathrm{c}} = \frac{1}{T_{\mathrm{s}}} \tag{40}$$

Solving the equation system consisting of (38)-(40), leads to the setting rules for K_{P} and K_{I}.

$$K_{\mathrm{P}} = \frac{\omega_c}{\hat{u}_1} \tag{41}$$

$$K_{\mathrm{I}} = T_{\mathrm{s}} \cdot \frac{{\omega_c}^3}{\hat{u}_1} \tag{42}$$

Since in healthy grid situations $\hat{u}_1$ in per unit will be close to 1, the default setting for $\hat{u}_1$ will also be 1.

For the negative sequence PLL-controller the same rules apply, with $\hat{u}_2$ instead of $\hat{u}_1$. Since negative sequence voltage is close to zero in healthy grid situations and between zero and about 0.5 p.u. in faulty situations, the default $\hat{u}_2$ setting is set to 0.5. This typical value can be explained with the following example.

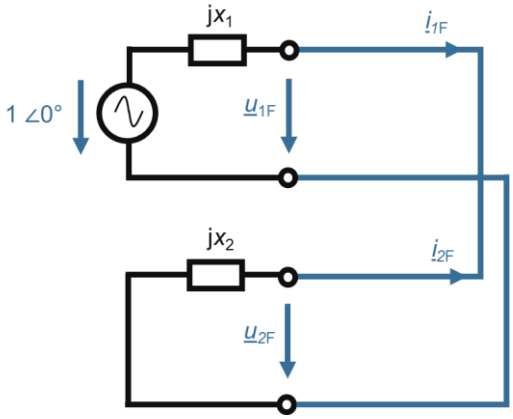

Fig. 19 Phase to phase fault without earth connection in symmetrical components

With the often valid assumption of $x_1 = x_2$, the above-mentioned value can be verified easily.

$$\underline{i}_{1F} = \frac{1}{\mathrm{j}x_1 + \mathrm{j}x_2} = \frac{1}{\mathrm{j}x_1 \cdot 2} \tag{43}$$

$$\underline{i}_{2F} = -\underline{i}_{1F} = \frac{-1}{\mathrm{j}x_1 \cdot 2} \tag{44}$$

$$\underline{u}_{2F} = -\underline{i}_{2F} \cdot \mathrm{j}x_2 = -\underline{i}_{2F} \cdot \mathrm{j}x_1 = \frac{\mathrm{j}x_1}{\mathrm{j}x_1 \cdot 2} = 0.5 \tag{45}$$

The default center frequencies are set empirically to 10 Hz for positive sequence and 30 Hz for negative sequence. In the following table the default settings are listed:

Table 1: Default PLL settings

	Positive sequence	Negative sequence
Voltage magnitude in pu	1	0.5
PI-controller center frequency f_c in Hz	10	30
T_s in seconds	10^{-4}	10^{-4}

2.5 Fault detection

As shown in the flowchart in Fig. 1, to detect a fault start, the standard VDE-4110 mentions two approaches. One of them just uses RMS-computed values of the sampled voltage measurements to detect faulty grid situations. This method can easily be implemented by inserting an RMS-block and simple logic to detect exceeding of the 10 % band around the nominal voltage.

The second approach consists in directly detecting the voltage phase jump by measuring the voltage waveforms and comparing them with a tolerance band around the voltage waveform of the continued pre-fault voltage. In theory this has the advantage, of detecting faults faster, then the RMS-method, since it is not dependent on a rather slow integration- or summation process.

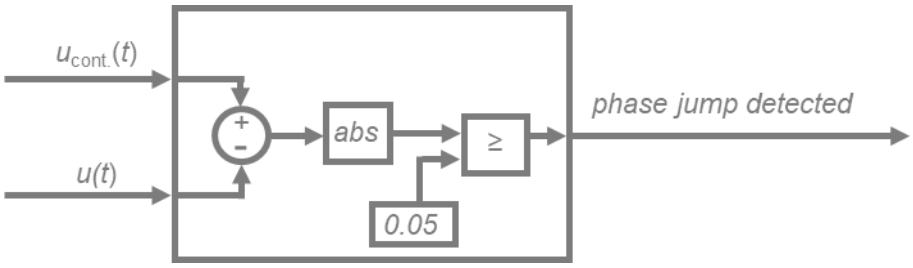

Fig. 20 Phase jump detection - basic logic

Although to find an appropriate time-domain solution to generate the continued signal is not trivial. In this work, two methods were developed and tested.

The first method, uses the dq-voltage components, computed by the PLL for current reference calculation, and transforms them back into time-dependent phase signals. Since during a phase-jump, the PLL itself cannot track the new phase angle immediately, also the signals transformed back into phase values will show a delayed angle change compared with the directly measured voltages.

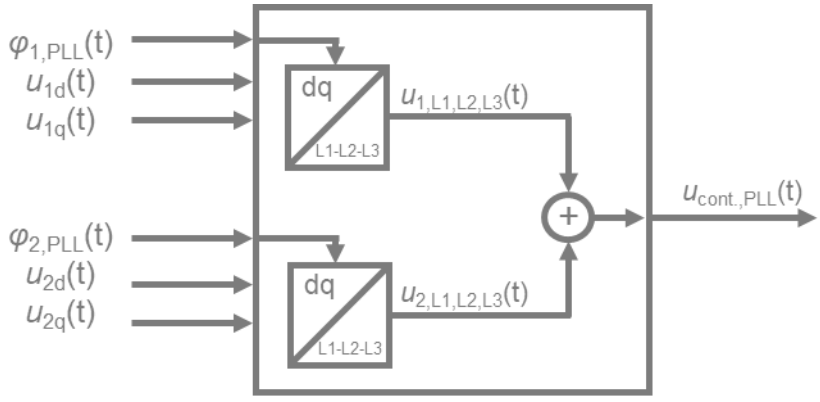

Fig. 21 PLL method to achieve continued signal

As a second method, an FFT-algorithm is used, to extract information about magnitude, phase angle and frequency of the three voltage signals. After a low-pass filter, this information is used to generate the continued signal, as shown in Fig. 22.

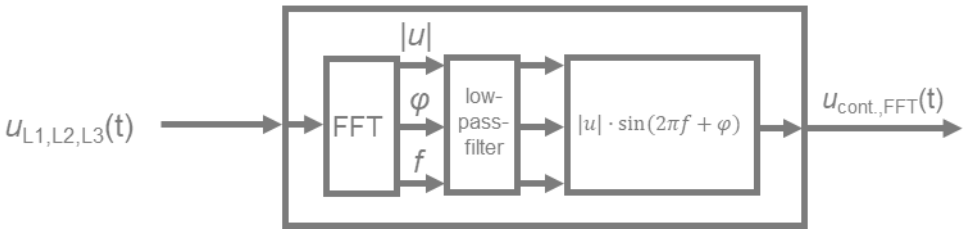

Fig. 22 FFT method to achieve continued signal

As an example, those two methods, and the conventional RMS-methods are compared for a situation with a three-phase fault.

At fault start the measured phase voltages change in the following manner:

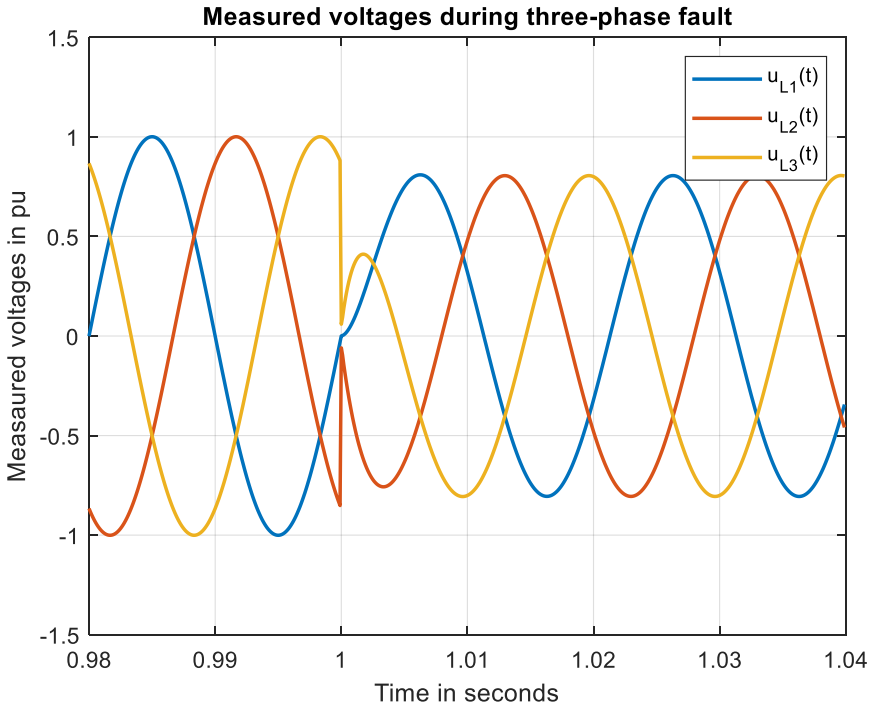

Fig. 23 Voltage phase jump during fault

Applied to phase L2, this method is capable of detecting the phase jump in less than $1 \cdot 10^{-5}$ seconds, which in a discrete time simulation leads to a total detecting time of only one discrete time step ($1 \cdot 10^{-4}$ seconds) at 10 kHz sampling frequency.

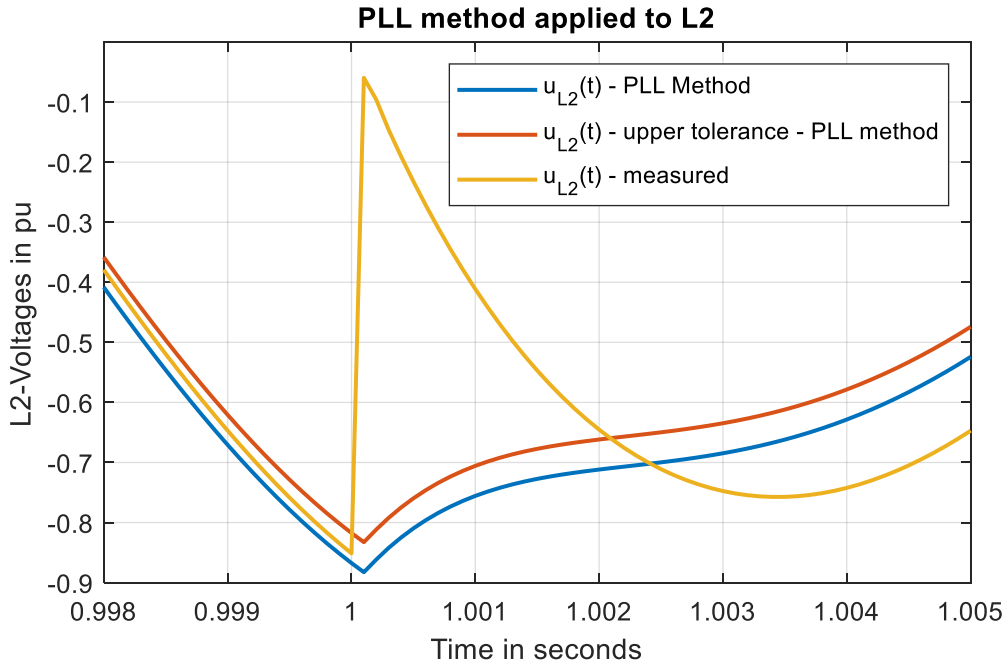

Fig. 24 PLL method applied to L2

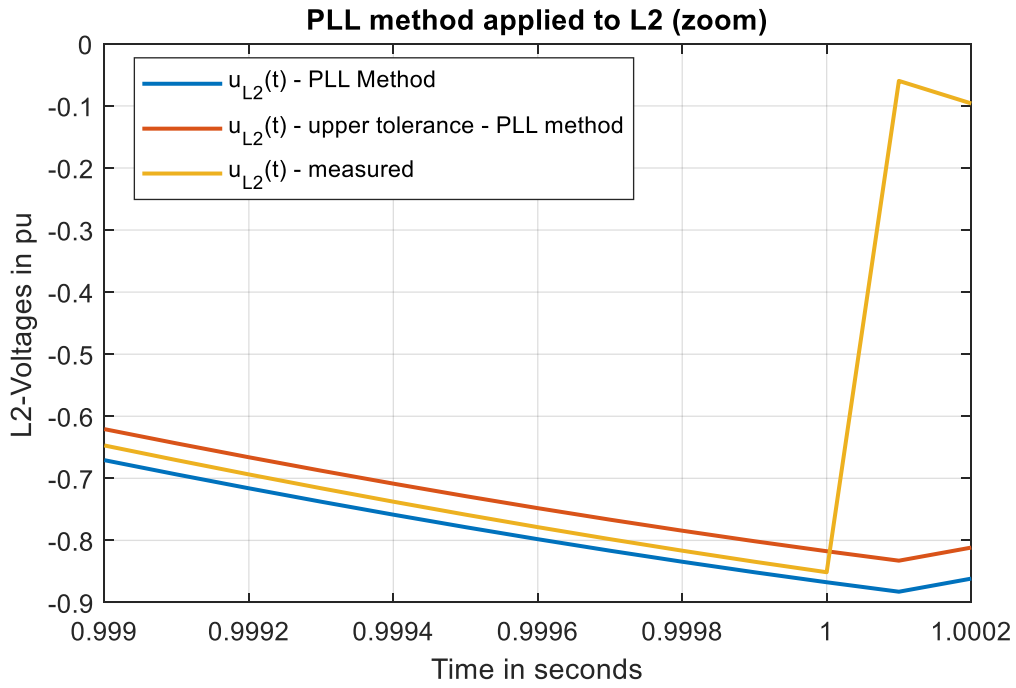

Fig. 25 PLL method applied to L2 (zoom)

Also, the FFT method leads to similar results, namely a detecting time of only one time step (at 10 kHz sampling frequency). Compared to the PLL-method, visible in Fig. 24, it can be seen, how the phase jump of the measured voltage, can be filtered out and is therefore not clearly visible in the continued signal.

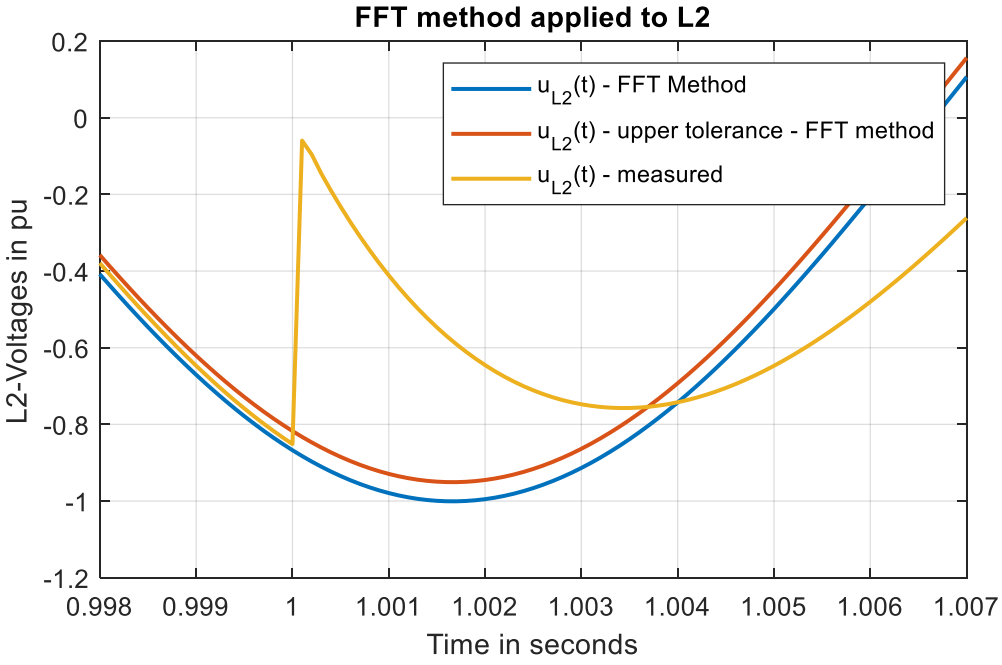

Fig. 26 FFT method applied to L2

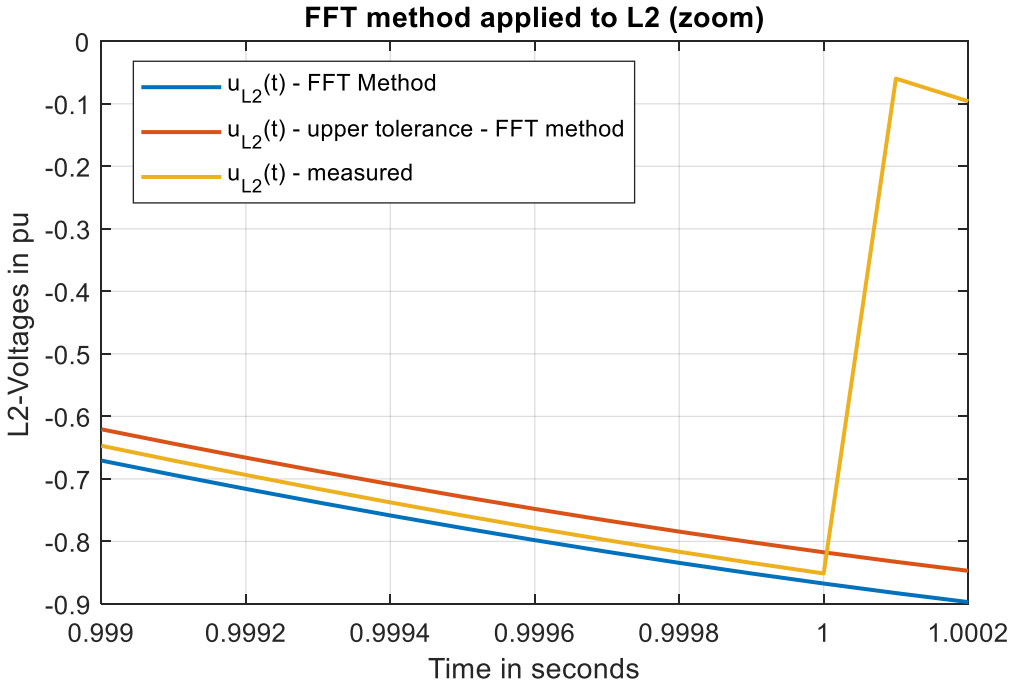

Fig. 27 FFT method applied to L2 (zoom)

The simple RMS-method detects the fault after about $4.2 \cdot 10^{-3}$ seconds, which is higher, compared to the previously mentioned methods, but is still way below one power system cycle.

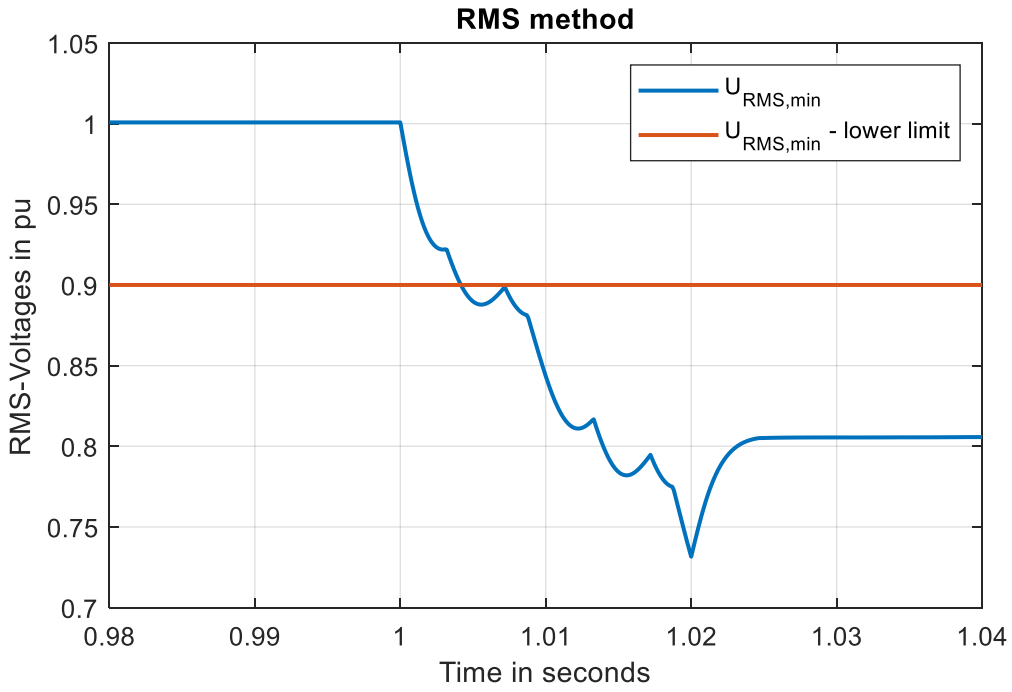

Fig. 28 RMS method to detect faults

In Fig. 28 it can be seen, how the minimum of the three computed RMS-voltages crosses the threshold of 0.9 p.u. nearly a second time shortly after the first crossing. According to the flowchart in Fig. 1 this could potentially lead to a wrongly detected end of fault, which would immediately stop reactive current injection and reset the fault time. Since this non monotonous behaviour is typical for the transient response of the RMS-computation to a phase jump, some countermeasures must be taken, as shown in Fig. 31, to avoid signal-bouncing in the boolean *fault*-signal.

Another issue can also be deduced from Fig. 1. Namely, according to the flowchart, the phase jump detection method is not used to detect the end of the fault. This means, that the start of a fault, which causes an RMS-voltage drop to a value higher than 0.9 p.u., may be detected by the phase jump detection, but not by the RMS-method, which then leads to a missed detection of the fault end.

In addition, another minor issue occurs with the PLL and FFT-methods. The standard VDE-4110 requests a continued signal computed by the average of magnitude, phase angle, and frequency over the last 50 cycles (1 seconds at 50 Hz). Although to achieve this accurately, with the FFT, a very long data set would be necessary, which efforts rather high computational effort. In contrast to this, the PLL-method, as implemented in this work, cannot be tuned at all.

This issues, combined with the fast fault detection by the RMS-method (less than half a cycle), lead to the following selected solution for this work.

Namely, the fault starts, and ends are only detected by the RMS-method, the time of start to measure the fault time although is taken, by the user-inserted fault starting time.

The used fault detection logic, namely the RMS-method, works in the following manner.

The three instantaneous phase-to-phase voltages are used to determine RMS voltages, using a discrete block containing basic mathematical methods, such as square-root, unit-delays etc. The maximum and minimum RMS-values are then compared against the thresholds defined by standard (VDE-4110). This comparison already indicates if a faulty situation is active. To avoid maloperation during transient PLL-start-up, another logical activation-signal is used to start this logic's operation. In this case the fault detection logic activation is triggered, as soon as the PLL-computed voltage u_{1d}. stays above 0.9 p.u. for 0.1 seconds, as shown in Fig. 29.

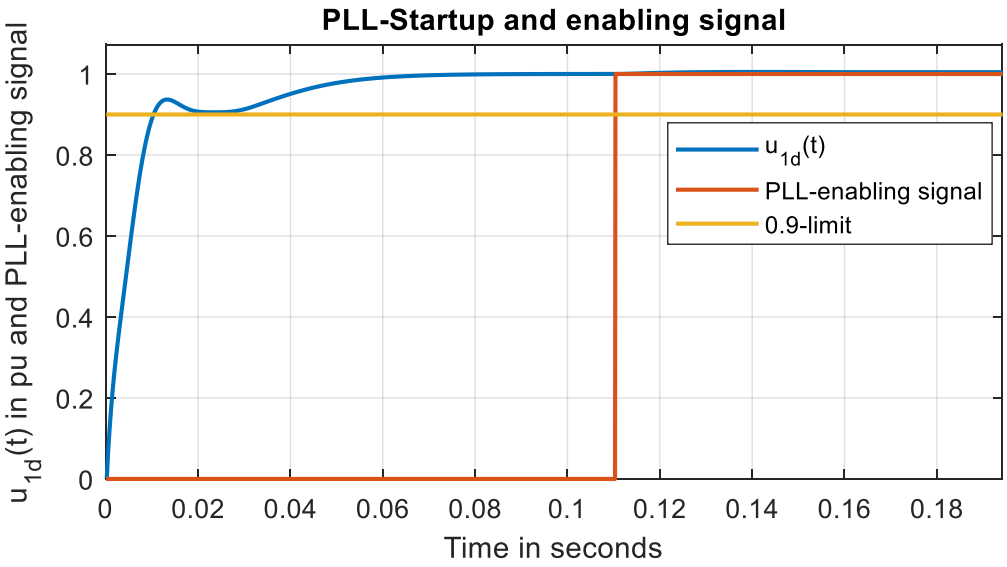

Fig. 29 PLL start-up and enabling signal

In addition to blocking the fault detection algorithm for PLL start-up, the explained enabling-signal is also used to enable current injection, only after finished PLL start-up, to avoid the risk of instability during start.

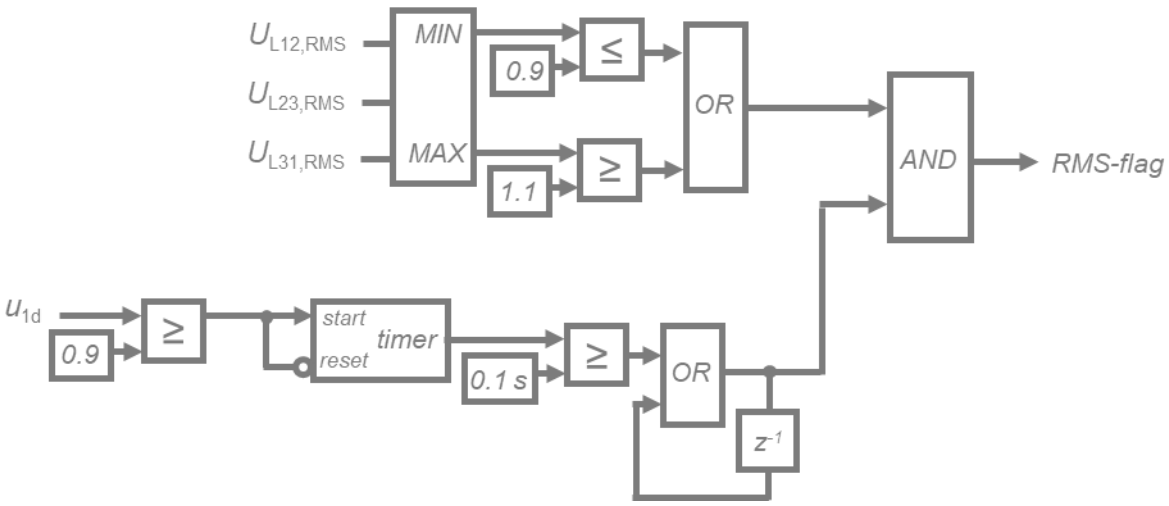

Fig. 30 RMS-fault detection logic

Since the RMS computation of the transient voltages does not always lead to monotone signals (see for example Fig. 28) and the computed signals may cross the threshold level several times during a transition. To avoid high frequency changes in the signal *RMS-flag* at fault end, a further *delaying falling edge*-block is used.

Then the fault time is computed, using the user-defined fault start as stated before. In addition, the fault time must be limited to a maximum value of 5 seconds, as stated in VDE-4110.

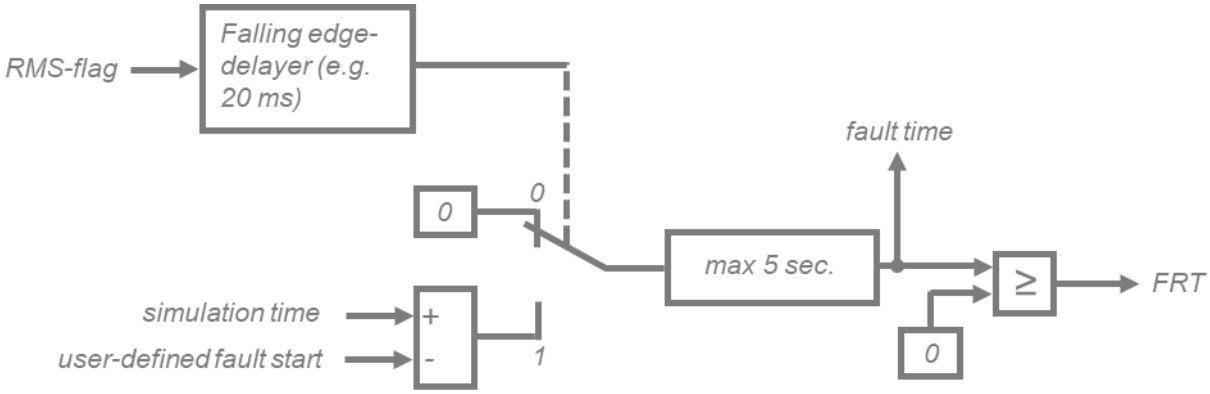

Fig. 31 Determination of fault time and FRT flag

The *Fault-Ride-Through* mode (*FRT*) is only activated if the fault time is positive.

To compare the voltage with the requested FRT-voltage-curve, a distinction between unsymmetrical and symmetrical faults is necessary. This is done through the use of negative-sequence voltage, which should only be zero under symmetrical conditions.

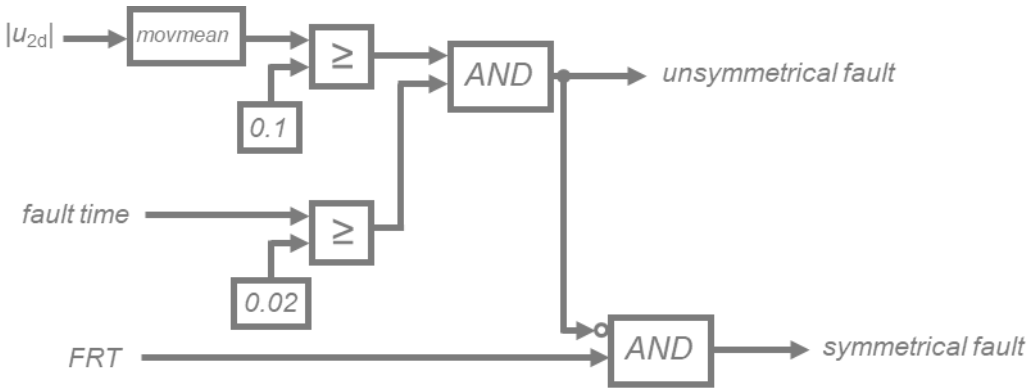

Fig. 32 Fault type distinction

The distinction between fault types is only done when the fault time is already above a threshold, since also negative sequence voltage may oscillate slightly after a symmetrical fault start due to PLL dynamics. This delayed distinction is compliant with VDE-4110, since according to Fig. 2, for the first 20 ms of fault, the fault type is not relevant.

Do determine, if in a specific situation the inverter would be allowed to trip, the voltage must be compared to FRT-curves, which can be done using look-up-tables, as shown schematically in Fig. 33.

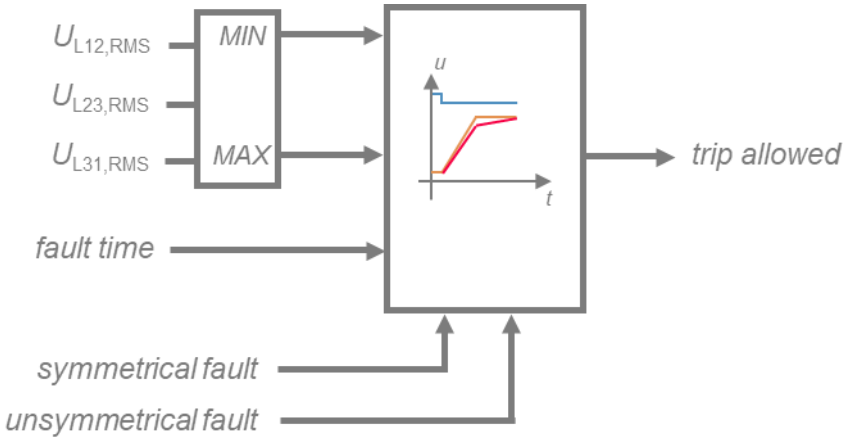

Fig. 33 FRT curve comparison

2.6 Compliance with technical guideline for generation plants (TR3)

The German FGW-Guideline *Technische Richtlinie Teil 3* (TR3) [52] specifies methods to determine the electrical characteristics of generation plants connected to the medium or high voltage grid. Those methods are the basis for tests and measurements carried out by certification authority to check the conformity of the relevant devices or systems. If all measurements result to be compliant with the corresponding standard, a unit certificate can be issued, necessary for the manufacturer to sell the product.

In this work the requirements for dynamic behaviour, especially reactive current injection during faults should be considered. According to VDE-4110, the additional reactive current injection must reach 90% of its reference step within 30 ms after fault start, while after 60 ms the additional reactive current must lay in a standard-defined tolerance band. To determine the relevant signals, from the measured terminal voltage and current signals, in the appendix of TR3, Fourier-series based formulas are provided.

TR3 requires for these verifications, measurements at different levels of voltage sags, caused by a voltage divider, included in a test facility acting as an interface between the inverter and the grid infeed. The guideline also defines a minimum X/R-ratio of the used impedances in the voltage divider, as well as a specific short circuit level of the infeed.

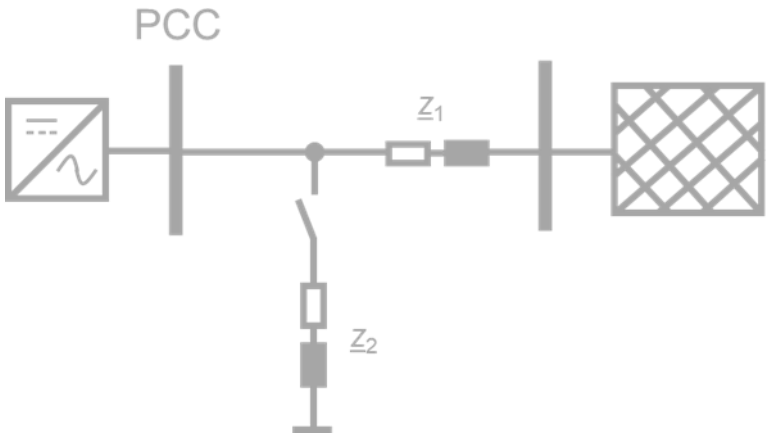

Fig. 34 TR3 verification set-up

For a three-phase voltage sag to a remaining voltage of just 0.23 pu, which is the lowest voltage range, where VDE-4110 requires reactive current injection, the following results were achieved.

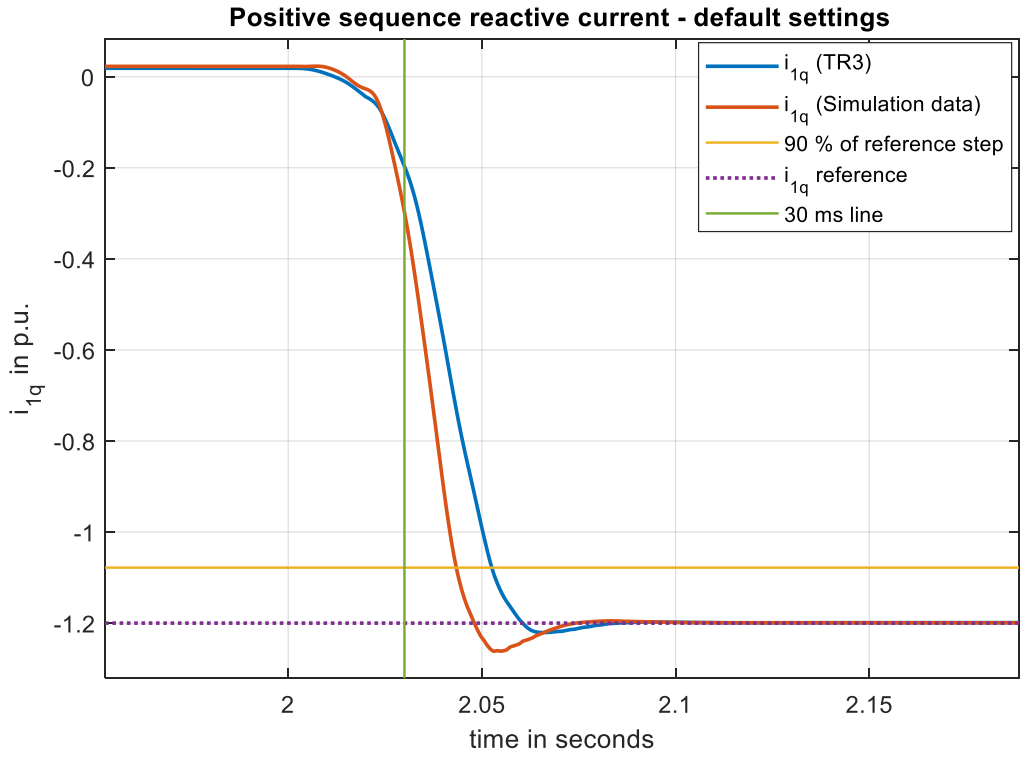

Fig. 35 TR3 verification with default settings

With the default PLL and filter settings, both, the internal i_{1q}, as wells as the calculated i_{1q} take too long to reach the reference value, to be compliant with VDE-4110. Namely both signals cross the yellow (90%) line after they crossed the green (30 ms) line.

By changing the default negative sequence PLL center frequency from 30 to 45 Hz, as well as by changing the cut-off frequency of low-pass filter located at the output of the i_{dq}-reference-block from 25 to 100 Hz, better results could be achieved. Why the negative sequence PLL influences the inverter behaviour during purely symmetrical situations is explained in chapter 5

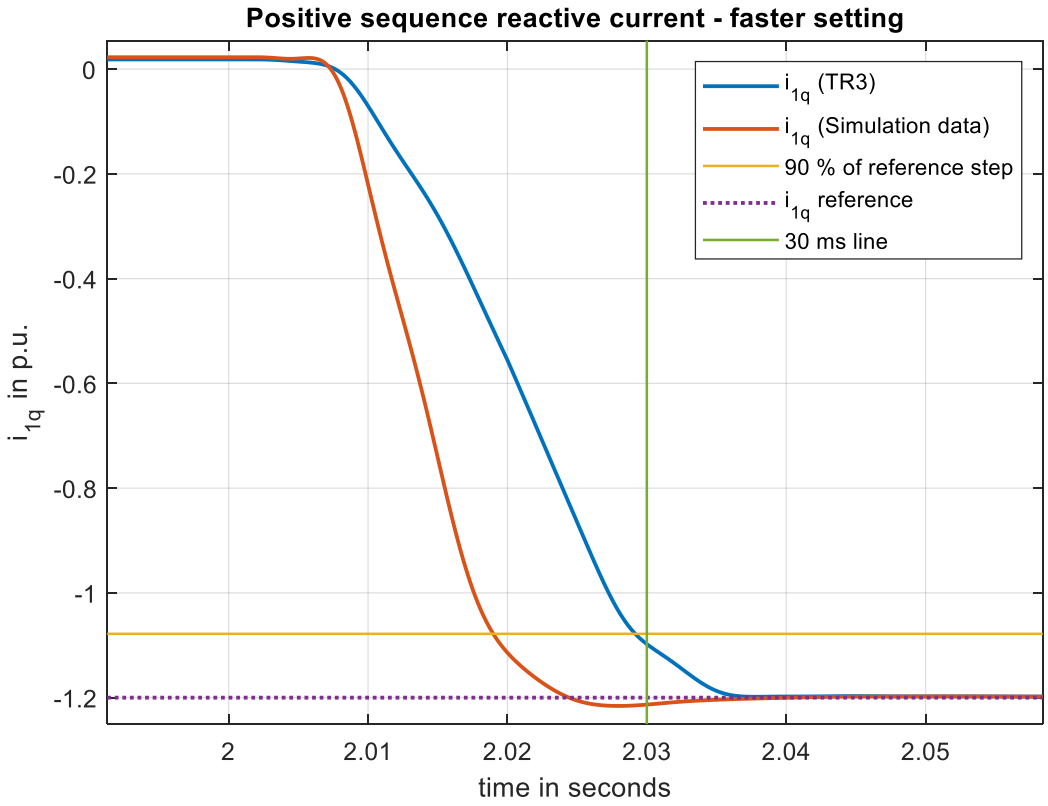

Fig. 36 Faster setting for better results

Fig. 36 shows, that it is possible to tune the model in such a way to reach standard-compliant dynamic behaviour. Although, since this generic model should be used to investigate the influence of different settings on the model's stability, standard-compliant behaviour is not necessary at all cost. To avoid having to test the model's standard compliancy after every setting change, for the rest of this work just the default settings ($f_{c,1}$ = 10 Hz, $f_{c,2}$ = 30 Hz, $f_{low\text{-}pass}$ = 25 Hz) are used.

In Fig. 35 and Fig. 36 it can be seen that the TR3-method to compute the relevant current signals leads to a delay compared to the internal simulation signals, due to its Fourier-series based approach. This means that the internal control signals of a real inverter must even be faster, than the standard requirements, to obtain standard-compliant results with the TR3-method.

3 Relation between symmetrical components and dq-values

For adapting the control to the requested standard characteristic, which is defined in classical symmetrical components, it is important to highlight the relation between symmetrical components and dq-quantities used in control.

3.1 Symmetrical Components

Again, it is assumed, the three-phase voltages consist of a positive and a negative sequence part, as visible in (46). The three-phase voltage set can therefore be described by two symmetrical three-phase sets, with opposed frequency sign and different magnitude and phase angle. The sign of the argument of the cos-function can be changed in (47), without further impact on the equation.

$$\begin{bmatrix} u_{\mathrm{L1}}(t) \\ u_{\mathrm{L2}}(t) \\ u_{\mathrm{L3}}(t) \end{bmatrix} = \hat{u}_1 \cdot \begin{bmatrix} \cos\left(\omega t + \varphi_1\right) \\ \cos\left(\omega t + \varphi_1 - {}^{2\pi}/_{3}\right) \\ \cos\left(\omega t + \varphi_1 + {}^{2\pi}/_{3}\right) \end{bmatrix} + \hat{u}_2 \cdot \begin{bmatrix} \cos\left(-\omega t + \varphi_2\right) \\ \cos\left(-\omega t + \varphi_2 - {}^{2\pi}/_{3}\right) \\ \cos\left(-\omega t + \varphi_2 + {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{46}$$

$$= \hat{u}_1 \cdot \begin{bmatrix} \cos\left(\omega t + \varphi_1\right) \\ \cos\left(\omega t + \varphi_1 - {}^{2\pi}/_{3}\right) \\ \cos\left(\omega t + \varphi_1 + {}^{2\pi}/_{3}\right) \end{bmatrix} + \hat{u}_2 \cdot \begin{bmatrix} \cos\left(\omega t - \varphi_2\right) \\ \cos\left(\omega t - \varphi_2 + {}^{2\pi}/_{3}\right) \\ \cos\left(\omega t - \varphi_2 - {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{47}$$

From the time-dependent voltages, trivial peak phasors can be computed, visible in (48). (the index ‘temp’ denotes a further future change in phasor representation)

$$\begin{bmatrix} \underline{\hat{u}}_{\mathrm{L1,temp}} \\ \underline{\hat{u}}_{\mathrm{L2,temp}} \\ \underline{\hat{u}}_{\mathrm{L3,temp}} \end{bmatrix} = \hat{u}_1 \cdot \begin{bmatrix} e^{\mathrm{j}\varphi_1} \\ e^{\mathrm{j}\left(\varphi_1 - {}^{2\pi}/_{3}\right)} \\ e^{\mathrm{j}\left(\varphi_1 + {}^{2\pi}/_{3}\right)} \end{bmatrix} + \hat{u}_2 \cdot \begin{bmatrix} e^{-\mathrm{j}\varphi_2} \\ e^{\mathrm{j}\left(-\varphi_2 + {}^{2\pi}/_{3}\right)} \\ e^{\mathrm{j}\left(-\varphi_2 - {}^{2\pi}/_{3}\right)} \end{bmatrix} = \begin{bmatrix} \hat{u}_1 \cdot e^{\mathrm{j}\varphi_1} + \hat{u}_2 \cdot e^{-\mathrm{j}\varphi_2} \\ \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 - {}^{2\pi}/_{3}\right)} + \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 + {}^{2\pi}/_{3}\right)} \\ \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + {}^{2\pi}/_{3}\right)} + \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - {}^{2\pi}/_{3}\right)} \end{bmatrix} \tag{48}$$

In practice when defining phasors, always phase L1 is taken as reference.

With $\angle\underline{\hat{u}}_{\mathrm{L1,temp}} = \varphi_{\mathrm{L1}}$ the voltage phasors can be written as shown in (49) and (50).

$$\begin{bmatrix} \underline{\hat{u}}_{\mathrm{L1}} \\ \underline{\hat{u}}_{\mathrm{L2}} \\ \underline{\hat{u}}_{\mathrm{L3}} \end{bmatrix} = \begin{bmatrix} \underline{\hat{u}}_{\mathrm{L1,temp}} \\ \underline{\hat{u}}_{\mathrm{L2,temp}} \\ \underline{\hat{u}}_{\mathrm{L3,temp}} \end{bmatrix} \cdot e^{-\mathrm{j}\varphi_{\mathrm{L1}}} \tag{49}$$

$$\begin{bmatrix} \underline{\hat{u}}_{\mathrm{L1}} \\ \underline{\hat{u}}_{\mathrm{L2}} \\ \underline{\hat{u}}_{\mathrm{L3}} \end{bmatrix} = \begin{bmatrix} \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 - \varphi_{\mathrm{L1}}\right)} + \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{\mathrm{L1}}\right)} \\ \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 - \varphi_{\mathrm{L1}} - {}^{2\pi}/_{3}\right)} + \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{\mathrm{L1}} + {}^{2\pi}/_{3}\right)} \\ \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 - \varphi_{\mathrm{L1}} + {}^{2\pi}/_{3}\right)} + \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{\mathrm{L1}} - {}^{2\pi}/_{3}\right)} \end{bmatrix} \tag{50}$$

The general methodology to calculate the positive sequence component from complex phasors is shown in (51).

Relation between symmetrical components and dq-values

$$\underline{\hat{u}}_1 = {}^1\!/_3 \cdot \left(\underline{\hat{u}}_{\mathrm{L1}} + \underline{\hat{u}}_{\mathrm{L2}} \cdot e^{\mathrm{j}\left({}^{2\pi}/_3\right)} + \underline{\hat{u}}_{\mathrm{L3}} \cdot e^{-\mathrm{j}\left({}^{2\pi}/_3\right)}\right) \tag{51}$$

By applying (51) to (50), (52) can be deduced.

$$\underline{\hat{u}}_1 = \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 - \varphi_{\mathrm{L1}}\right)} \tag{52}$$

The general equation for the negative sequence component (53), applied to (50), brings to (54).

$$\underline{\hat{u}}_2 = {}^1\!/_3 \cdot \left(\underline{\hat{u}}_{\mathrm{L1}} + \underline{\hat{u}}_{\mathrm{L2}} \cdot e^{-\mathrm{j}\left({}^{2\pi}/_3\right)} + \underline{\hat{u}}_{\mathrm{L3}} \cdot e^{\mathrm{j}\left({}^{2\pi}/_3\right)}\right) \tag{53}$$

$$\underline{\hat{u}}_2 = \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{\mathrm{L1}}\right)} \tag{54}$$

As already mentioned in 2.3, the treatment of zero-sequence quantities in inverter models, is normally not necessary and is therefore set to be zero in this derivation. The non-existence of zero-sequence in the voltage set defined by (46), gets even more obvious when applying (55) to (50).

$$\underline{\hat{u}}_0 = {}^1\!/_3 \cdot \left(\underline{\hat{u}}_{\mathrm{L1}} + \underline{\hat{u}}_{\mathrm{L2}} + \underline{\hat{u}}_{\mathrm{L3}}\right) \tag{55}$$

$$\underline{\hat{u}}_0 = 0 \cdot e^{\mathrm{j}(0)} \tag{56}$$

Summarized, the symmetrical voltage components are shown in (57):

$$\begin{bmatrix} \underline{\hat{u}}_1 \\ \underline{\hat{u}}_2 \\ \underline{\hat{u}}_0 \end{bmatrix} = \begin{bmatrix} \hat{u}_1 \cdot e^{\mathrm{j}\left(\varphi_1 - \varphi_{\mathrm{L1}}\right)} \\ \hat{u}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{\mathrm{L1}}\right)} \\ 0 \cdot e^{\mathrm{j}(0)} \end{bmatrix} \tag{57}$$

Similar as for voltages, also the phase currents consist of a positive and negative sequence component. Respectively to the voltages the two sequence currents have an angle of $\varphi_{1\mathrm{I}}$ and $\varphi_{2\mathrm{I}}$ and can be written as (58) and (59).

$$\begin{bmatrix} i_{\mathrm{L1}}(t) \\ i_{\mathrm{L2}}(t) \\ i_{\mathrm{L3}}(t) \end{bmatrix} = \hat{\imath}_1 \cdot \begin{bmatrix} \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}}\right) \\ \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}} - {}^{2\pi}/_{3}\right) \\ \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}} + {}^{2\pi}/_{3}\right) \end{bmatrix} + \hat{\imath}_2 \cdot \begin{bmatrix} \cos\left(-\omega t + \varphi_2 + \varphi_{2\mathrm{I}}\right) \\ \cos\left(-\omega t + \varphi_2 + \varphi_{2\mathrm{I}} - {}^{2\pi}/_{3}\right) \\ \cos\left(-\omega t + \varphi_2 + \varphi_{2\mathrm{I}} + {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{58}$$

$$= \hat{\imath}_1 \cdot \begin{bmatrix} \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}}\right) \\ \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}} - {}^{2\pi}/_{3}\right) \\ \cos\left(\omega \mathrm{t} + \varphi_1 + \varphi_{1\mathrm{I}} + {}^{2\pi}/_{3}\right) \end{bmatrix} + \hat{\imath}_2 \cdot \begin{bmatrix} \cos\left(\omega t - \varphi_2 - \varphi_{2\mathrm{I}}\right) \\ \cos\left(\omega t - \varphi_2 - \varphi_{2\mathrm{I}} + {}^{2\pi}/_{3}\right) \\ \cos\left(\omega t - \varphi_2 - \varphi_{2\mathrm{I}} - {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{59}$$

In (60) phasor notation is used again.

$$\begin{aligned} \begin{bmatrix} \underline{\hat{\imath}}_{\mathrm{L1,temp}} \\ \underline{\hat{\imath}}_{\mathrm{L2,temp}} \\ \underline{\hat{\imath}}_{\mathrm{L3,temp}} \end{bmatrix} &= \hat{\imath}_1 \cdot \begin{bmatrix} e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}}\right)} \\ e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} - {}^{2\pi}/_{3}\right)} \\ e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} + {}^{2\pi}/_{3}\right)} \end{bmatrix} + \hat{\imath}_2 \cdot \begin{bmatrix} e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}}\right)} \\ e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} + {}^{2\pi}/_{3}\right)} \\ e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} - {}^{2\pi}/_{3}\right)} \end{bmatrix} \\ &= \begin{bmatrix} \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}}\right)} + \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}}\right)} \\ \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} - {}^{2\pi}/_{3}\right)} + \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} + {}^{2\pi}/_{3}\right)} \\ \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} + {}^{2\pi}/_{3}\right)} + \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} - {}^{2\pi}/_{3}\right)} \end{bmatrix} \end{aligned} \tag{60}$$

Referencing the phasors to L1-voltage is shown in (61).

$$\begin{aligned} \begin{bmatrix} \underline{\hat{\imath}}_{\mathrm{L1}} \\ \underline{\hat{\imath}}_{\mathrm{L2}} \\ \underline{\hat{\imath}}_{\mathrm{L3}} \end{bmatrix} &= \begin{bmatrix} \underline{\hat{\imath}}_{\mathrm{L1,temp}} \\ \underline{\hat{\imath}}_{\mathrm{L2,temp}} \\ \underline{\hat{\imath}}_{\mathrm{L3,temp}} \end{bmatrix} \cdot e^{-\mathrm{j}\varphi_{\mathrm{L1}}} \\ &= \begin{bmatrix} \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} - \varphi_{\mathrm{L1}}\right)} + \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} - \varphi_{\mathrm{L1}}\right)} \\ \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} - \varphi_{\mathrm{L1}} - {}^{2\pi}/_{3}\right)} + \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} - \varphi_{\mathrm{L1}} + {}^{2\pi}/_{3}\right)} \\ \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} - \varphi_{\mathrm{L1}} + {}^{2\pi}/_{3}\right)} + \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} - \varphi_{\mathrm{L1}} - {}^{2\pi}/_{3}\right)} \end{bmatrix} \end{aligned} \tag{61}$$

Computing the symmetrical components leads to the result, shown in (62).

$$\begin{bmatrix} \underline{\hat{\imath}}_1 \\ \underline{\hat{\imath}}_2 \\ \underline{\hat{\imath}}_0 \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & e^{\mathrm{j}\,{}^{2\pi}/_{3}} & e^{-\mathrm{j}\,{}^{2\pi}/_{3}} \\ 1 & e^{-\mathrm{j}\,{}^{2\pi}/_{3}} & e^{\mathrm{j}\,{}^{2\pi}/_{3}} \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \underline{\hat{\imath}}_{\mathrm{L1}} \\ \underline{\hat{\imath}}_{\mathrm{L2}} \\ \underline{\hat{\imath}}_{\mathrm{L3}} \end{bmatrix} = \begin{bmatrix} \hat{\imath}_1 \cdot e^{\mathrm{j}\left(\varphi_1 + \varphi_{1\mathrm{I}} - \varphi_{\mathrm{L1}}\right)} \\ \hat{\imath}_2 \cdot e^{\mathrm{j}\left(-\varphi_2 - \varphi_{2\mathrm{I}} - \varphi_{\mathrm{L1}}\right)} \\ 0 \end{bmatrix} \tag{62}$$

With respect to the associated sequence voltage angles, the current components can be split into an active and reactive part, as shown in (63) and (64).

$$\begin{gathered}\hat{\imath}_{1,\mathrm{active}} + \mathrm{j}\cdot\hat{\imath}_{1,\mathrm{reactive}} = \\ \left|\underline{\hat{\imath}}_1\right|\cdot\left(\cos\left(\varphi_1+\varphi_{1\mathrm{I}}-\varphi_{\mathrm{L}1}-\varphi_1+\varphi_{\mathrm{L}1}\right)+\mathrm{j}\cdot\sin\left(\varphi_1+\varphi_{1\mathrm{I}}-\varphi_{\mathrm{L}1}-\varphi_1+\varphi_{\mathrm{L}1}\right)\right) \\ = \hat{\imath}_1\cdot\cos\left(\varphi_{1\mathrm{I}}\right)+\mathrm{j}\cdot\hat{\imath}_1\cdot\sin\left(\varphi_{1\mathrm{I}}\right)\end{gathered} \tag{63}$$

Similar for the negative sequence current:

$$\begin{gathered}\hat{\imath}_{2,\mathrm{active}} + \mathrm{j}\cdot\hat{\imath}_{2,\mathrm{reactive}} = \\ \left|\underline{\hat{\imath}}_2\right|\cdot\left(\cos\left(-\varphi_2-\varphi_{2\mathrm{I}}-\varphi_{\mathrm{L}1}+\varphi_2+\varphi_{\mathrm{L}1}\right)+\mathrm{j}\cdot\sin\left(-\varphi_2-\varphi_{2\mathrm{I}}-\varphi_{\mathrm{L}1}+\varphi_2+\varphi_{\mathrm{L}1}\right)\right) \\ = \hat{\imath}_2\cdot\cos\left(-\varphi_{2\mathrm{I}}\right)+\mathrm{j}\cdot\hat{\imath}_2\cdot\sin\left(-\varphi_{2\mathrm{I}}\right)\end{gathered} \tag{64}$$

3.2 dq-transformation method (used in digital control)

As already explained in 2.3, the three-phase voltages can be represented in an orthogonal coordinate system using the Clarke-transformation, shown in (65).

$$\begin{bmatrix}u_\alpha(t)\\ u_\beta(t)\end{bmatrix} = \frac{2}{3}\cdot\begin{bmatrix}1 & -\frac{1}{2} & -\frac{1}{2}\\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2}\end{bmatrix}\cdot\begin{bmatrix}u_{\mathrm{L}1}(t)\\ u_{\mathrm{L}2}(t)\\ u_{\mathrm{L}3}(t)\end{bmatrix} \tag{65}$$

By Applying (65) to (46) and the use of some trigonometric identities, (66) can be deduced.

$$\begin{bmatrix}u_\alpha(t)\\ u_\beta(t)\end{bmatrix} = \hat{u}_1\cdot\begin{bmatrix}\cos(\omega t+\varphi_1)\\ \sin(\omega t+\varphi_1)\end{bmatrix}+\hat{u}_2\cdot\begin{bmatrix}\cos(-\omega t+\varphi_2)\\ \sin(-\omega t+\varphi_2)\end{bmatrix} \tag{66}$$

By delaying the components of (66) by a quarter cycle, (67), can be received.

$$\begin{bmatrix}u_\alpha^{\mathrm{T}}(t)\\ u_\beta^{\mathrm{T}}(t)\end{bmatrix} = \hat{u}_1\cdot\begin{bmatrix}\sin(\omega t+\varphi_1)\\ -\cos(\omega t+\varphi_1)\end{bmatrix}+\hat{u}_2\cdot\begin{bmatrix}-\sin(-\omega t+\varphi_2)\\ \cos(-\omega t+\varphi_2)\end{bmatrix} \tag{67}$$

By adding the original and orthogonal signals in an appropriate matter, Clarke-components can be split into positive and negative sequence, as shown in (68).

$$\begin{bmatrix}u_{1\alpha}(t)\\ u_{2\alpha}(t)\\ u_{1\beta}(t)\\ u_{2\beta}(t)\end{bmatrix} = \frac{1}{2}\cdot\begin{bmatrix}u_\alpha(t)-u_\beta^{\mathrm{T}}(t)\\ u_\alpha(t)+u_\beta^{\mathrm{T}}(t)\\ u_\alpha^{\mathrm{T}}(t)+u_\beta(t)\\ -u_\alpha^{\mathrm{T}}(t)+u_\beta(t)\end{bmatrix} = \begin{bmatrix}\hat{u}_1\cdot\cos(\omega t+\varphi_1)\\ \hat{u}_2\cdot\cos(-\omega t+\varphi_2)\\ \hat{u}_1\cdot\sin(\omega t+\varphi_1)\\ \hat{u}_2\cdot\sin(-\omega t+\varphi_2)\end{bmatrix} \tag{68}$$

For computing the dq-components for positive and negative sequence the following park-transformation is applied. The needed angles φ_1 and φ_2 are not known but in reality, can be computed using a controller to control the q-component to zero (PLL). For positive sequence (69) is used.

$$\begin{bmatrix} u_{1\mathrm{d}}(t) \\ u_{1\mathrm{q}}(t) \end{bmatrix} = \begin{bmatrix} \cos(\omega t + \varphi_1) & \sin(\omega t + \varphi_1) \\ -\sin(\omega t + \varphi_1) & \cos(\omega t + \varphi_1) \end{bmatrix} \cdot \begin{bmatrix} u_{1\alpha}(t) \\ u_{1\beta}(t) \end{bmatrix} \tag{69}$$

For negative sequence very similar to (69), (70) is used.

$$\begin{bmatrix} u_{2\mathrm{d}}(t) \\ u_{2\mathrm{q}}(t) \end{bmatrix} = \begin{bmatrix} \cos(-\omega t + \varphi_2) & \sin(-\omega t + \varphi_2) \\ -\sin(-\omega t + \varphi_2) & \cos(-\omega t + \varphi_2) \end{bmatrix} \cdot \begin{bmatrix} u_{2\alpha}(t) \\ u_{2\beta}(t) \end{bmatrix} \tag{70}$$

If the transformation angles are chosen/controlled in such a way, that the q-components are zero (phase locked loop is locked) the dq-voltages for positive sequence result in (71), while negative sequence ends up in (72).

$$\begin{bmatrix} u_{1\mathrm{d}}(t) \\ u_{1\mathrm{q}}(t) \end{bmatrix} = \begin{bmatrix} u_{1\mathrm{d}} \\ u_{1\mathrm{q}} \end{bmatrix} = \begin{bmatrix} \hat{u}_1 \\ 0 \end{bmatrix} \tag{71}$$

$$\begin{bmatrix} u_{2\mathrm{d}}(t) \\ u_{2\mathrm{q}}(t) \end{bmatrix} = \begin{bmatrix} u_{2\mathrm{d}} \\ u_{2\mathrm{q}} \end{bmatrix} = \begin{bmatrix} \hat{u}_2 \\ 0 \end{bmatrix} \tag{72}$$

Similar is valid for the currents. Again, the angles $\varphi_{1\mathrm{I}}$ and $\varphi_{2\mathrm{I}}$ are used to describe the phase shift between voltage and current in each sequence system, as shown in (73).

$$\begin{bmatrix} i_{\mathrm{L1}}(t) \\ i_{\mathrm{L2}}(t) \\ i_{\mathrm{L3}}(t) \end{bmatrix} = \hat{\imath}_1 \cdot \begin{bmatrix} \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}}\right) \\ \cos\left(\omega t + \varphi_1 + \varphi_{1\mathrm{I}} - {}^{2\pi}/_{3}\right) \\ \cos\left(\omega \mathrm{t} + \varphi_1 + \varphi_{1\mathrm{I}} + {}^{2\pi}/_{3}\right) \end{bmatrix} + \hat{\imath}_2 \cdot \begin{bmatrix} \cos\left(\omega t - \varphi_2 - \varphi_{2\mathrm{I}}\right) \\ \cos\left(\omega t - \varphi_2 - \varphi_{2\mathrm{I}} + {}^{2\pi}/_{3}\right) \\ \cos\left(\omega t - \varphi_2 - \varphi_{2\mathrm{I}} - {}^{2\pi}/_{3}\right) \end{bmatrix} \tag{73}$$

Similar as for the voltages, also the currents can be transformed into αβ-components and then split into positive and negative sequence, which results in (74).

$$\begin{bmatrix} i_{1\alpha}(t) \\ i_{2\alpha}(t) \\ i_{1\beta}(t) \\ i_{2\beta}(t) \end{bmatrix} = \begin{bmatrix} \hat{\imath}_1 \cdot \cos(\omega t + \varphi_1 + \varphi_{1\mathrm{I}}) \\ \hat{\imath}_2 \cdot \cos(-\omega t + \varphi_2 + \varphi_{2\mathrm{I}}) \\ \hat{\imath}_1 \cdot \sin(\omega t + \varphi_1 + \varphi_{1\mathrm{I}}) \\ \hat{\imath}_2 \cdot \sin(-\omega t + \varphi_2 + \varphi_{2\mathrm{I}}) \end{bmatrix} \tag{74}$$

Finally, after dq-transformation, (75) is obtained.

$$\begin{bmatrix} i_{1\mathrm{d}} \\ i_{1\mathrm{q}} \\ i_{2\mathrm{d}} \\ i_{2\mathrm{q}} \end{bmatrix} = \begin{bmatrix} \hat{\imath}_1 \cdot \cos(\varphi_{1\mathrm{I}}) \\ \hat{\imath}_1 \cdot \sin(\varphi_{1\mathrm{I}}) \\ \hat{\imath}_2 \cdot \cos(\varphi_{2\mathrm{I}}) \\ \hat{\imath}_2 \cdot \sin(\varphi_{2\mathrm{I}}) \end{bmatrix} \tag{75}$$

3.3 Conclusion

From the result shown in (63), (64) and (75), it can be seen, that the only difference between active and reactive symmetrical components currents and dq-currents is a sign flip in the angle of the negative sequence component.

With this knowledge, the following reflection is possible.

During grid faults, typically the positive sequence voltage drops at the inverter's terminal. The additional reactive current, requested by VDE-4110 for example, should somehow counteract this situation, by boosting the positive sequence voltage. Generally, it is known, that capacitive/overexcited behaviour acts voltage boosting in inductive lines. Therefore, in generator convention the additional reactive current during a fault in positive sequence, computed in classical symmetrical components should be negative.

In contrast to pure symmetrical grid faults, during asymmetrical faults, also the negative sequence is influenced. Since during healthy, ideal pre-fault situations, negative sequence is zero, during faults, the magnitude can only rise due to asymmetrical faults. In negative sequence the inverter should therefore act voltage decreasing, which means inductive behaviour. In classical symmetrical components, inductive behaviour in generator convention would mean positive reactive current. But since there is a difference between the sign of the arguments in (64) and (75), in dq-domain the negative sequence reactive current during asymmetrical faults, should be negative.

4 Investigation on Phase-Locked-Loop dynamics

4.1 Investigations on start-up process (positive sequence)

To investigate on the PLL-behaviour during start-up, some tests are carried out. The test model should emulate a 1 MW PV-park. The PV-park is connected via a 1.25 MVA transformer and a 2 km long MV-cable to the 20 kV-grid. The grid provides a short circuit power of 1 GVA at the connection point and an insulated neutral point.

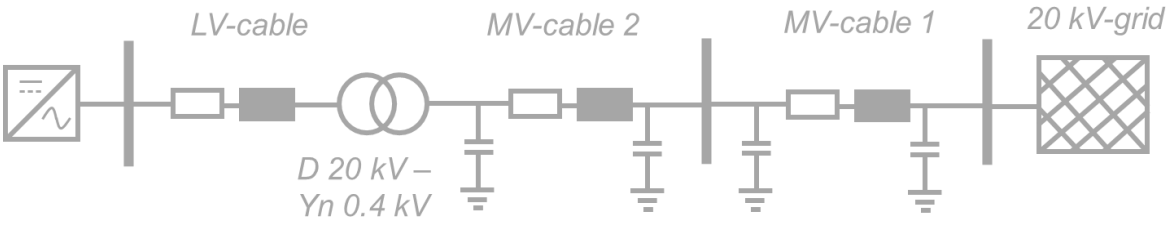

Fig. 37 Grid model for start-up investigation

Table 2 Model settings for investigation in start-up

MV-grid connection		
U_n	20	kV
S_{grid}	1	GVA
$\|Z_{grid}\|$	0.4	Ω
KXR	7	-
X_{grid}	0.396	Ω
R_{grid}	0.057	Ω
MV-cable 1 (MV-cable 2 same specifications)		
length	1	km
c_1'	300	nF/km
c_0'	175	nF/km
r_1' + jx_1'	0.075 + j0.1	Ω/km
r_0' + jx_0'	1.64 + j0.332	Ω/km
Transformer		
S_{rated}	1.25	MVA
vector group	Dyn11	-
U_{prim}	20	kV
U_{sec}	0.4	kV
u_{sc}	6	%

$u_{sc,real}$	0.5	%
i_{noload}	0.1	%
LV-cable		
length	0.02	km
section	900	mm^2
r_1'	0.0311	Ω/km
x_1'	0.12	Ω/km

In a first simulation, the positive sequence PLL-PI-controller frequency is varied and the initialization process of the PLL signals are observed.

The model is configured as described in the above table. The setting for the positive sequence PLL were varied between 10, 20 and 30 Hz. During the transient initialization process, the following signals can be observed.

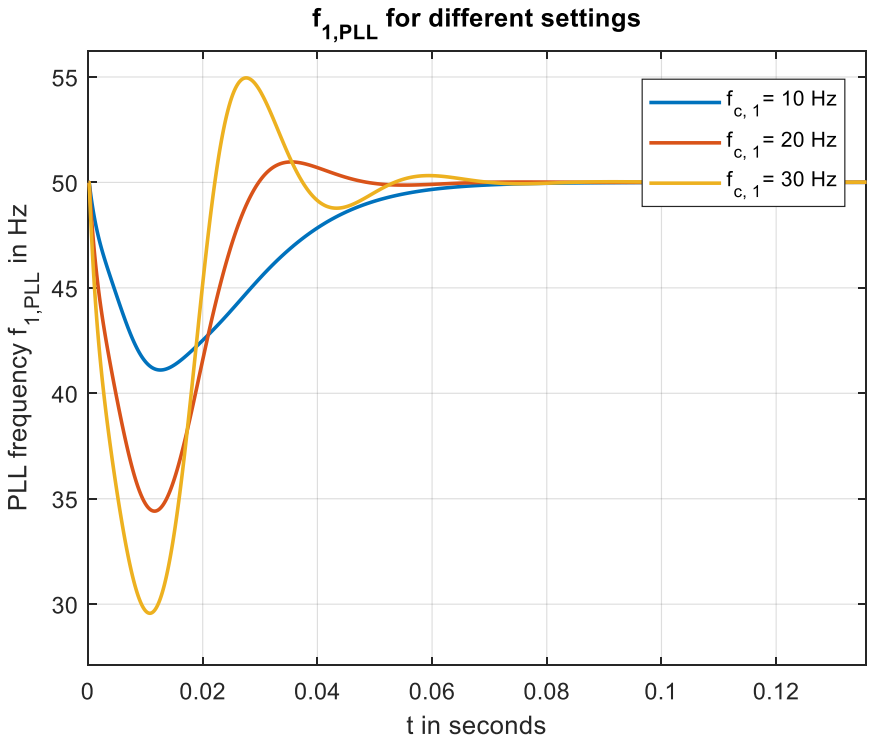

Fig. 38 PLL-frequency at start

In Fig. 38 it can be clearly observed, how the PI-controller center frequency changes the dynamic response of the PLL. The yellow signal (30 Hz) shows by far the steepest descent at the start and also the strongest over ringing before settling around the nominal frequency, while the default frequency of 10 Hz does not cause overshoot. After about four cycles (80 ms) the three settings reach the same result.

Also, in the integral of the frequency, namely the PLL-angle used for αβ-dq-transformation, the difference in the setting is clearly visible (Fig. 39).

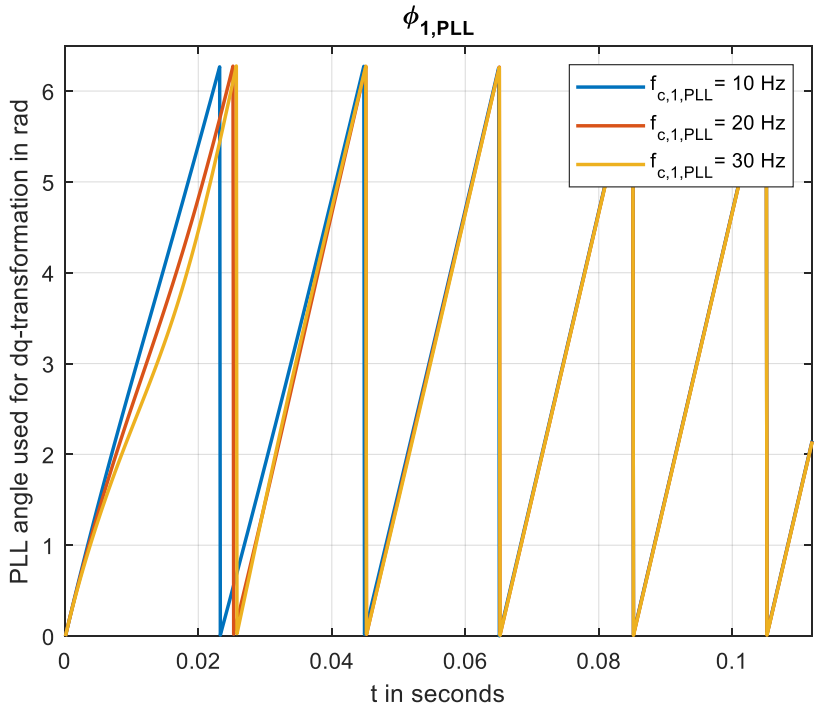

Fig. 39 PLL angle during start-up

Since during the first cycle, the 10 Hz-setting delivers higher frequency, also the computed angle rises faster. The plots cannot be distinguished visually after about 2-3 cycles.

In Fig. 38 it can be observed that the frequency starts already at the nominal value, but then drops to a setting-dependent value, before resettling again at nominal range, although the nominal frequency is set as a feedforward signal. To understand the reason for this at first glance rather strange behaviour a more detailed look into the PLL-model is necessary.

To explain this behaviour, just the positive sequence PLL is taken into account without considering the sequence decomposition logic with the SOGI blocks in front of the PLL. A set of known αβ-voltages are fed to the PLL. When knowing the voltages as a mathematical expression, also the ideal PLL-angle $\varphi_{1,PLL,ideal}$ can be found easily.

For example, when choosing the orthogonal set of αβ-voltages to be:

$$\begin{bmatrix} u_{1\alpha} \\ u_{1\beta} \end{bmatrix} = \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - {}^{\pi}/_{2}) \end{bmatrix} \tag{76}$$

Then, to simulate a locked PLL, the following has to be true:

$$u_{1q} = 0 = -\sin(\varphi_{1,PLL,ideal}) \cdot \sin(\omega t) + \cos(\varphi_{1,PLL,ideal}) \cdot \sin(\omega t - {}^{\pi}/_{2}) \tag{77}$$

It can be shown easily that this is valid, if:

$$\varphi_{1,PLL,ideal} = \omega t - \frac{\pi}{2} \tag{78}$$

Simulating this case leads to the following results (PLL setting $f_{c,1}$ = 20 Hz):

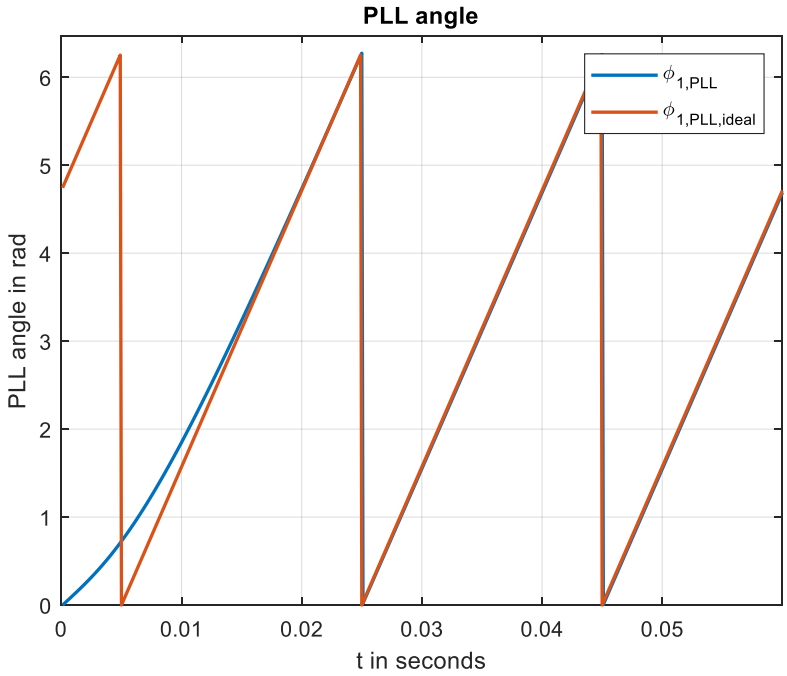

Fig. 40 PLL angle for 20 Hz PLL setting

It can be seen, how the angle computed as the integral of the frequency starts steadily from zero and therefore normally does not match instantly with the ideal angle. Jumps in the computed angle would indicate unrealistic frequency values around infinity. It can also be seen that the initial slope of the angle is smaller than the final slope. This also means that, the computed frequency (Fig. 41) at the start is smaller than the final/rated frequency.

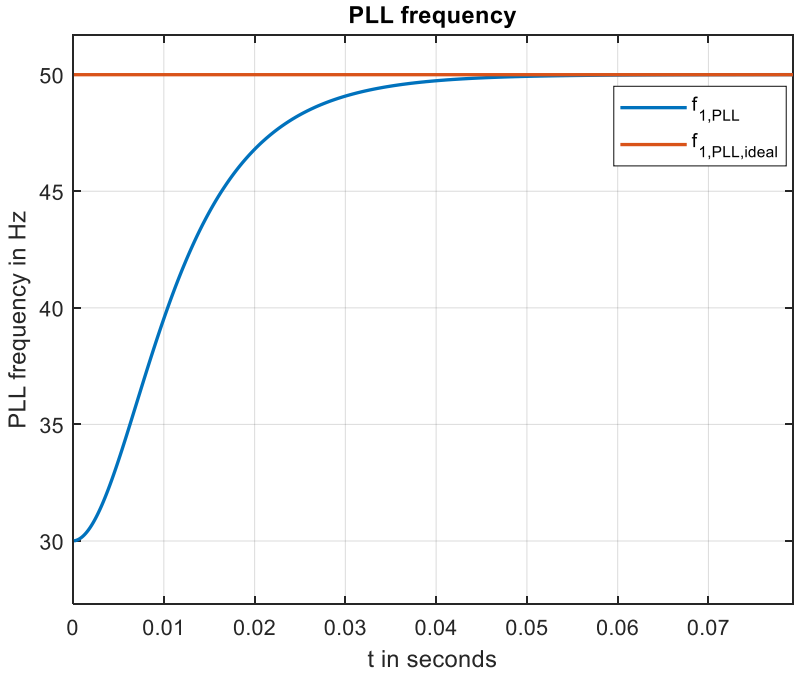

Fig. 41 PLL frequency for 20 Hz PLL setting

In the frequency of Fig. 41 a massive drop in initial frequency is visible. Where this drop comes from can be explained when observing the signal path in the general PLL model of Fig. 16.

In a more detailed way, also the inside of the PI-controller, as well as the final integrator should be explained. In the whole Simulink model all transfer functions, filters, controllers, and integrators are implemented in a discrete manner, to facilitate transferring the model into a hardware environment. In the case of the PLL-PI-controller the backward-Euler integrating method is used, while in the final PLL-integrator forward-Euler integration is used to transfer from s-domain into z-domain.

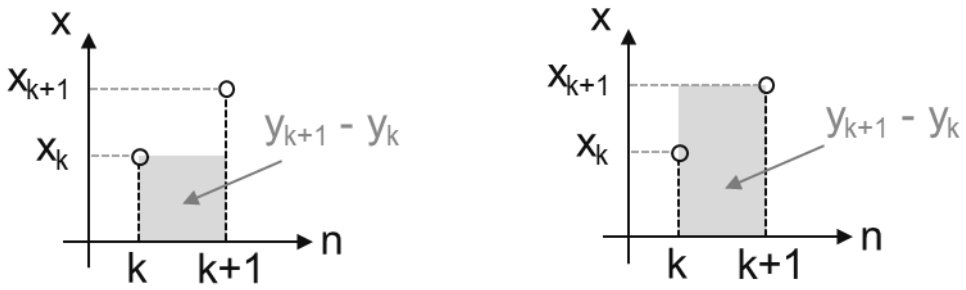

Fig. 42 Numerical integration (left: Forward-Euler, right: Backward-Euler)

For forward-Euler method the following applies:

$$y_{k+1} = y_k + x_k \cdot T_s \tag{79}$$

Where T_s is the time between one discrete time step and the subsequent one. In this case, it is the sampling/simulation time step. For too large time steps this integration method, when used in a feedback loop, can cause instabilities. On the other hand, the backward-Euler method has way less stability issues, but is harder to implement, since it has an implicit characteristic, which is obvious when observing the output equation [53].

$$y_{k+1} = y_k + x_{k+1} \cdot T_s \tag{80}$$

To transfer those two characteristics into z-domain, the time delaying property of the z-transformation has to be known: (b_n may be a series with $b_n = 0$ for $n < 0$)

$$a_n = b_{n-1} \tag{81}$$

$$a(z) = b(z) \cdot z^{-1} \tag{82}$$

For the forward Euler method, this leads to:

$$y(z) = y(z) \cdot z^{-1} + x(z) \cdot z^{-1} \cdot T_s \tag{83}$$

$$\frac{y(z)}{x(z)} = \frac{z^{-1} \cdot T_s}{1 - z^{-1}} \tag{84}$$

For the backward Euler method, this leads to:

$$y(z) = y(z) \cdot z^{-1} + x(z) \cdot T_s \tag{85}$$

$$\frac{y(z)}{x(z)} = \frac{T_s}{1 - z^{-1}} \tag{86}$$

When comparing those two transfer functions with the known transfer function of a continuous time integrator, one gets the transformation rules between s- and z-domain.

For the forward Euler method:

$$\frac{1}{s} \sim \frac{z^{-1} \cdot T_\mathrm{s}}{1 - z^{-1}} \rightarrow s \sim \frac{z - 1}{T_\mathrm{s}} \tag{87}$$

And for the backward Euler method:

$$\frac{1}{s} \sim \frac{T_\mathrm{s}}{1 - z^{-1}} \rightarrow s \sim \frac{z - 1}{z \cdot T_\mathrm{s}} \tag{88}$$

When applying the derived relation (88) on the continuous time PI-controller transfer function, the following can be derived:

$$C(s) = \frac{K_\mathrm{P} \cdot s + K_\mathrm{I}}{s} \rightarrow C(z) = \frac{K_\mathrm{P} \cdot \frac{z - 1}{z \cdot T_\mathrm{s}} + K_\mathrm{I}}{\frac{z - 1}{z \cdot T_\mathrm{s}}} = \frac{K_\mathrm{P} \cdot (z - 1) + K_\mathrm{I} \cdot z \cdot T_\mathrm{s}}{(z - 1)} = \frac{u(z)}{e(z)} \tag{89}$$

$$u(z) \cdot (z - 1) = e(z) \cdot K_\mathrm{P} \cdot (z - 1) + e(z) \cdot K_\mathrm{I} \cdot z \cdot T_\mathrm{s} \tag{90}$$

$$u(z) \cdot (1 - z^{-1}) = e(z) \cdot K_\mathrm{P} \cdot (1 - z^{-1}) + e(z) \cdot K_\mathrm{I} \cdot T_\mathrm{s} \tag{91}$$

$$u_\mathrm{k} = u_{\mathrm{k}-1} + K_\mathrm{P} \cdot (e_\mathrm{k} - e_{\mathrm{k}-1}) + K_\mathrm{I} \cdot T_\mathrm{s} \cdot e_\mathrm{k} \tag{92}$$

u_k denotes the controller output at time step k and e_k denotes the error, which is computed as difference between the controlled variable and its reference value r_k. In the case of the PLL, the controlled variable is the q-component voltage, the reference value equals zero and the controller output is a difference frequency.

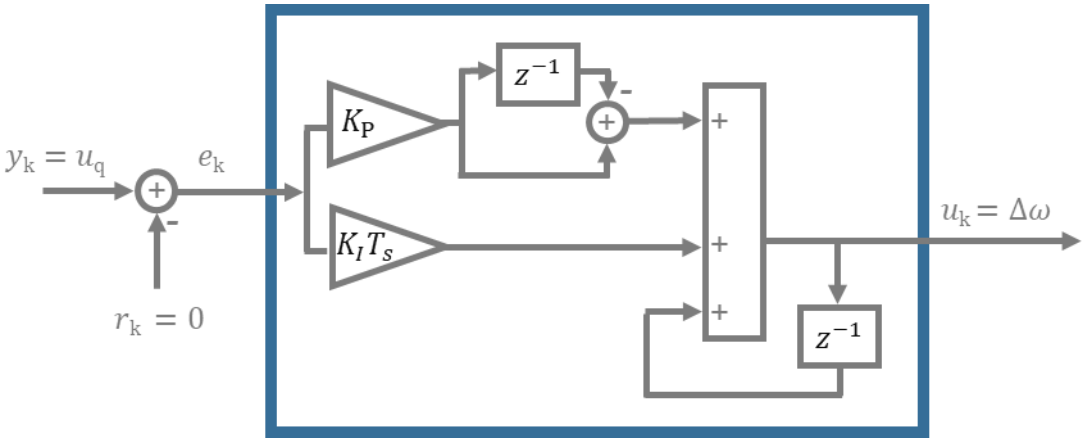

Fig. 43 PI-controller in discrete domain

To the computed difference frequency, the rated frequency is added, and the sum then integrated to get an angle value. To achieve higher accuracy the input signal into the integrating block is multiplied with the nominal frequency and divided by it before the output. In addition, in the integrator block a modulo logic is used to unwrap the computed angle into the range $0 \leq \varphi < 2 \cdot \pi(\cdot f_{\text{rated}})$.

As already mentioned for the integrator the forward-Euler method is used.

$$\frac{\varphi_{\text{PLL}}}{\omega_{\text{PLL}}} = \frac{z^{-1} \cdot T_{\text{s}}}{1 - z^{-1}} = \frac{T_{\text{s}}}{z - 1} \tag{93}$$

$$\varphi_{\text{PLL}} \cdot (z - 1) = \omega_{\text{PLL}} \cdot T_{\text{s}} \tag{94}$$

$$\varphi_{\text{PLL}} \cdot (1 - z^{-1}) = \omega_{\text{PLL}} \cdot z^{-1} \cdot T_{\text{s}} \tag{95}$$

$$\varphi_{\text{PLL,k}} = \varphi_{\text{PLL,k-1}} + \omega_{\text{PLL,k-1}} \cdot T_{\text{s}} \tag{96}$$

$$\varphi_{\text{PLL,k+1}} = \varphi_{\text{PLL,k}} + \omega_{\text{PLL,k}} \cdot T_{\text{s}} \tag{97}$$

To avoid an algebraic loop in the PLL-structure, not $\varphi_{\text{PLL,k+1}}$ but the unit-step-delayed signal $\varphi_{\text{PLL,k}}$ is taken as output signal and as current PLL-angle.

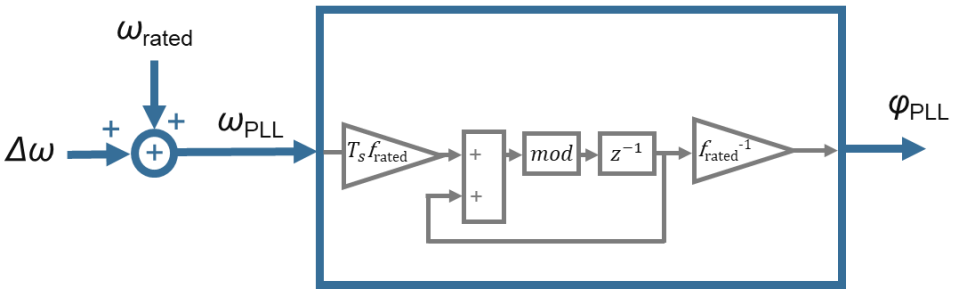

Fig. 44 PLL-Integrator block

By adding now the explained blocks together, the PLL-behaviour during start-up can be examined and explained in more detail. At first the already above mentioned situation should be examined. The positive sequence αβ-dq-block is directly fed by a set of known αβ-voltages. The PLL-controller center frequency is set to be 20 Hz, which leads to controller parameters $K_{\text{P}} = 126$ and $K_{\text{I}} = 198$. To understand the PLL-starting-process, the first few simulation time steps should be considered in detail:

At the first time-step $t_0 = 0.0$ ms only the constants are initialized, and no signal passes any logic block. At t_1=0.1 ms the simulation starts. It makes sense to start following the signal from the unit-delay-block in the integrator, since it is the only clear border between one time step and the subsequent one. At t_1, the mentioned delay block outputs zero since the input was not available at t_0 and the initial output value of the delay block is set to zero. The PLL-angle at t_1 is therefore zero too and is fed back to the αβ-block. In this situation the αβ-voltages are chosen to be: $u_\alpha = \sin(\omega t)$ and $u_\beta = \sin(\omega t - \pi/2)$. The q-component of the voltage is then computed.

$$u_{\text{q,t1}} = -\sin(0) \cdot \sin(\omega t_1) + \cos(0) \cdot \sin(\omega t_1 - {}^{\pi}/_{2}) \sim -1\,pu \tag{98}$$

Since also the unit-delays in the PI-controller output zeros, at t_1, the controller output is:

$$\Delta\omega_{t1} = u_{q,t1} \cdot (K_P + K_I \cdot T_S) = u_{q,t1} \cdot (K_P + K_I \cdot T_S) \quad (99)$$
$$= -1 \cdot (126 + 0.02) \sim -126\, rad/s$$

To the computed controller output the rated frequency is added, which leads to the initial PLL-frequency:

$$\omega_{PLL,t1} = \Delta\omega_{t1} + \omega_{rated} = 189\, rad/s \sim 30\, Hz \quad (100)$$

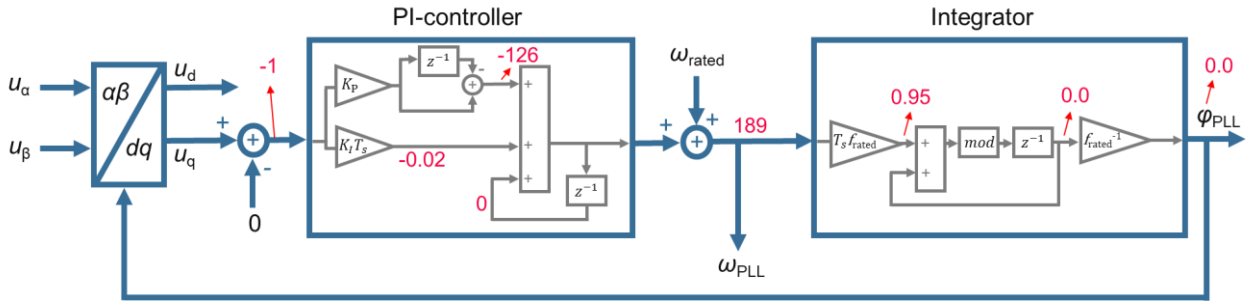

Fig. 45 PLL structure with signal values for t1 = 0.1 ms

This observation explains the massive drop in initial PLL-frequency in Fig. 41. It can also be distinguished, which blocks and parameters mostly influence the PLL start-up.

The initial drop in frequency strongly depends on the αβ-voltage offset angle or simply the exact starting time, since it influences directly the first computed q-voltage with PLL angle = 0.

To show this dependency different αβ-offset angles are set:

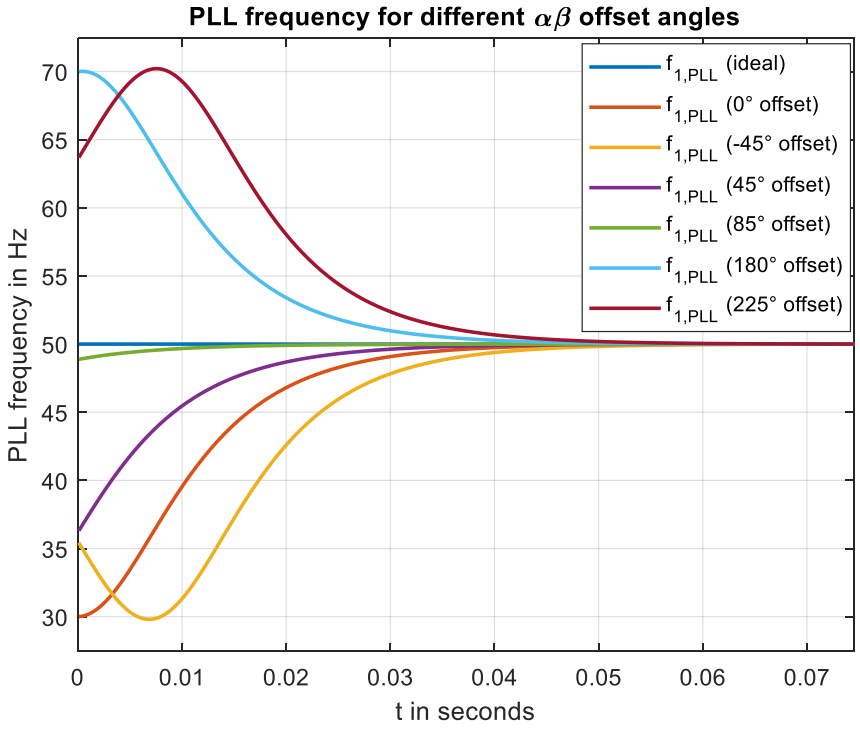

Fig. 46 PLL start up for different voltage offset angles

The situation with 85° offset angle (green line) on the αβ-voltage set leads to a nearly ideal start-up process. The initial ideal PLL-angle is apparently close to zero, which leads to a fast transition of PLL-

frequency and angle into the steady state. Dependent on the offset angle, the initial frequency can also rise above the nominal value (180° light blue, 225° red). It can also be observed that the maximum deviation from the nominal frequency does not have to be right at the start but can also occur later during the first cycle (for example -45°, yellow or 225°, red).

Another major influence factor on the dynamic PLL behaviour are the PLL-PI-controller settings. Since the output of the controller is the difference frequency, this is obvious. To observe the dependency again, settings should be varied, and results observed. The positive sequence PLL is directly fed by a known set of αβ-voltages, the offset angle is set to be zero and the sequence decomposition block is again omitted for the start.

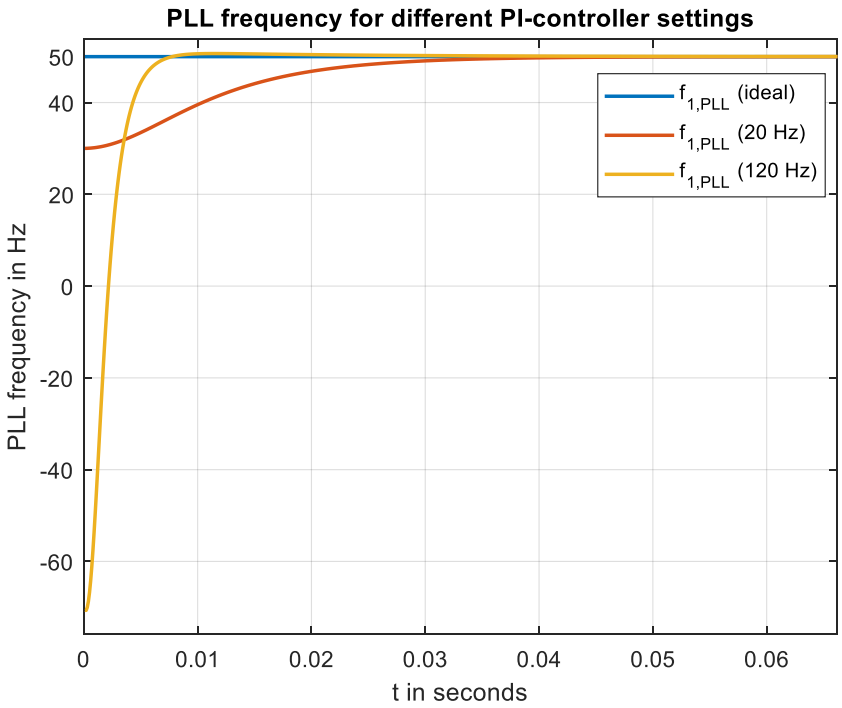

Fig. 47 PLL frequency for different PLL settings (without sequence decomposition)

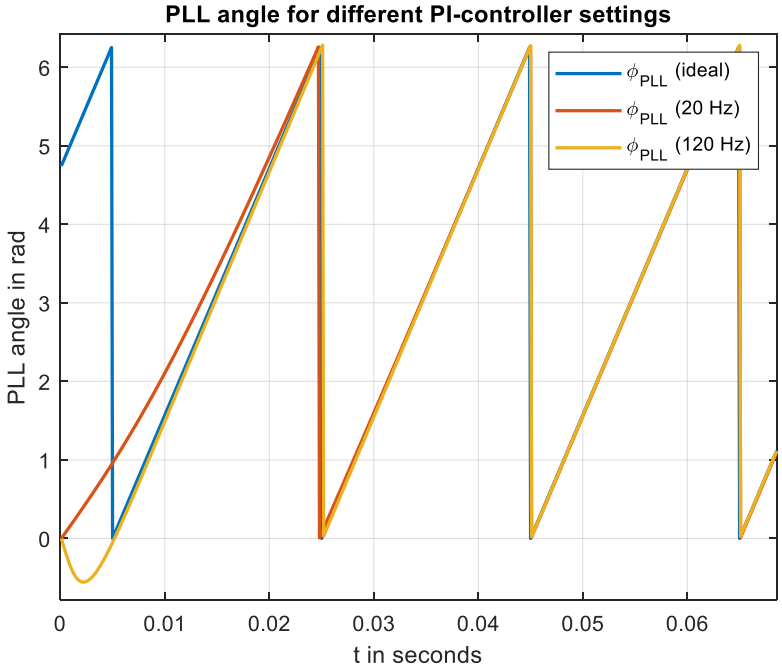

Fig. 48 PLL frequency for different PLL settings (without sequence decomposition)

It can be seen, how a very high controller center frequency influences the start-up process. For a value of 120 Hz the initial PLL-frequency even drops to a negative value, which leads to an angle oscillation into the negative direction.

As often in control systems, very aggressive control settings, such as the 120 Hz-setting, tent more to cause instabilities. In this case with fixed input voltage although no controller setting can be found easily, which eventually ends in a trajectory off the ideal one. Therefore, the simplification of omitting the sequence decomposition block (includes the SOGI) is undone and the behaviour is checked again with the more complex structure.

Extending the general structure with the previously explained SOGI, leads to the following layout.

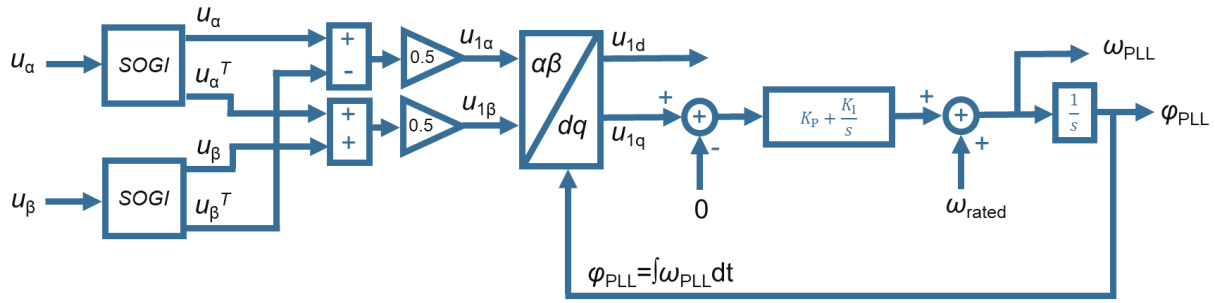

Fig. 49 Model with SOGI (only positive sequence shown)

The first test is again done with a known pure positive sequence set of αβ-voltages. In this case the input αβ-voltages should be the same as the αβ-voltages fed to the positive sequence PLL, after a start-up process. The results for the same αβ-voltage and the same controller settings look like the following:

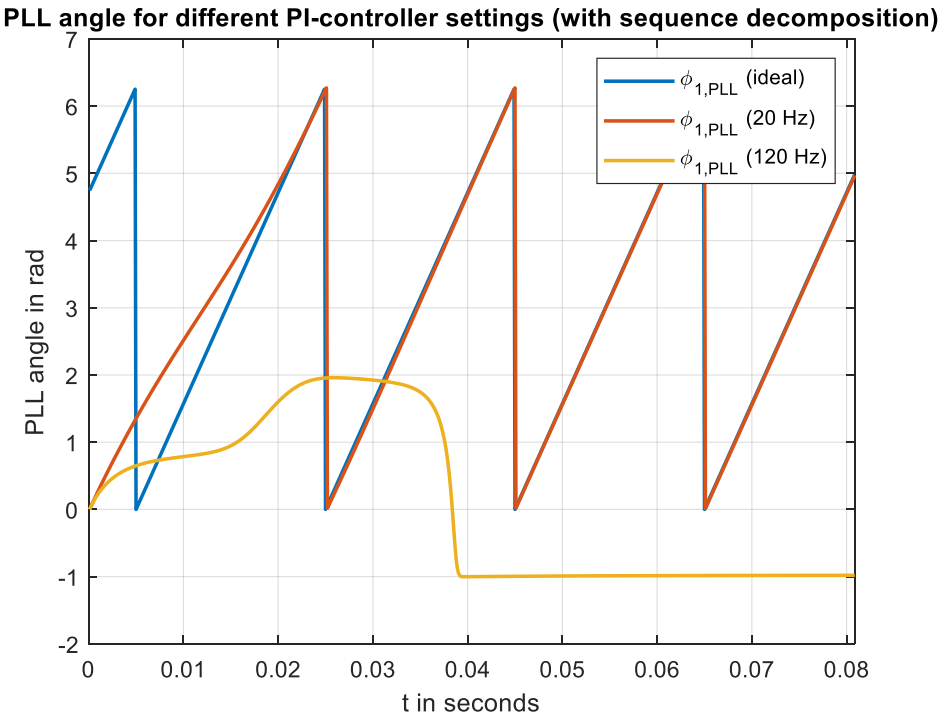

Fig. 50 PLL angle during start-up (with sequence decomposition)

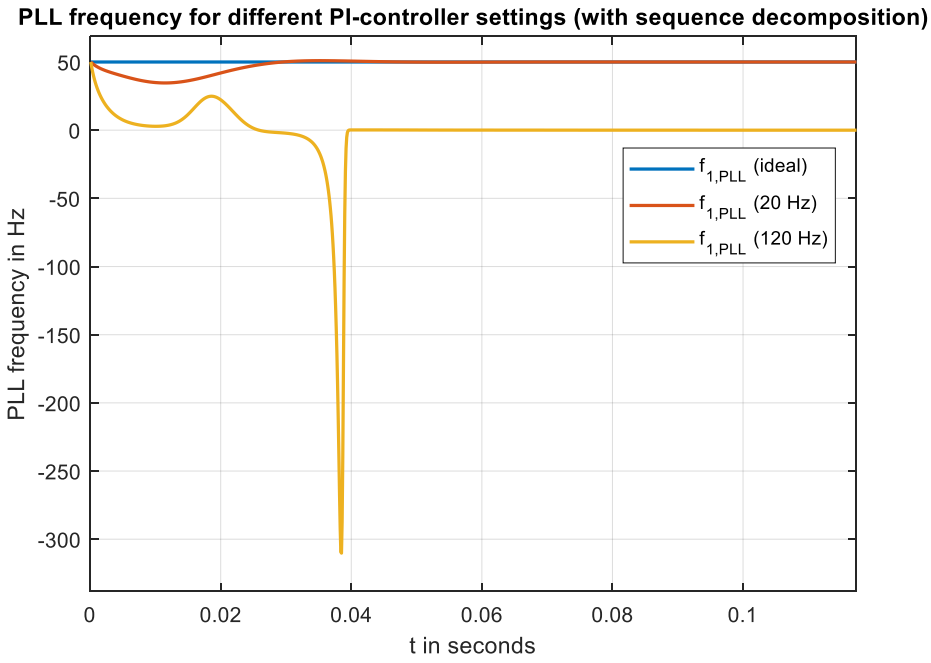

Fig. 51 PLL frequency during start-up (with sequence decomposition)

As it can be seen, with the SOGI in front of the PLL, the controller setting with 20 Hz still leads to the desired results, while with the 120 Hz-setting apparently no useful results are achieved. The frequency settles at zero Hz after a big undershoot, while the angle settles at a rather random constant value.

Apparently the SOGI-block changes the behaviour massively. To understand the cause, a more detailed look into the as a quarter cycle delayer acting SOGI is useful.

From the SOGI structure shown in Fig. 13, the structure consisting of elementary blocks can be derived easily, when deriving the relation between input signal *u*, original signal output *y* and orthogonal signal output y^{T}:

$$y^{\mathrm{T}} = y \cdot \frac{\omega_{\mathrm{c}}}{s} \tag{101}$$

$$y = [k \cdot (u - y) - y^{\mathrm{T}}] \cdot \frac{\omega_{\mathrm{c}}}{s} \tag{102}$$

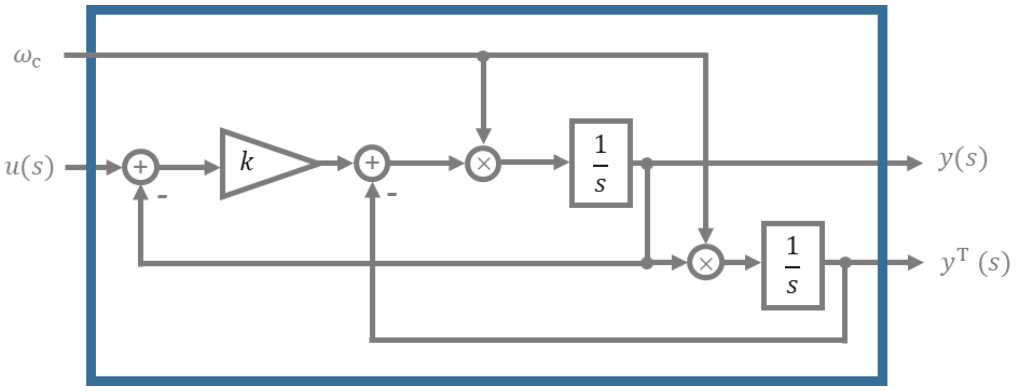

Fig. 52 SOGI structure

When observing the inner structure, it is obvious that a frequency of zero, which can happen during strong oscillations, leads to a constant output, since the last block is an integrator.

The output of the SOGI is then defined by the last transmitted frequency component. If this constant output and the instantaneous angle result in a q-voltage of zero, the PLL will not move from there. Such a situation must be avoided, since the computed dq-values are not related correctly to the relevant time dependent phase values. Finding the highest working controller-setting for different environments is not trivial and a large enough safety space should be considered. To avoid the above-mentioned undesired situation a simple limiting block is inserted at the output of the PLL-PI controller after the rated angular frequency feedforward, which limits the minimum angular frequency to 100 rad/s. This block can also be used to set a warning signal if the controller settings seem too aggressive.

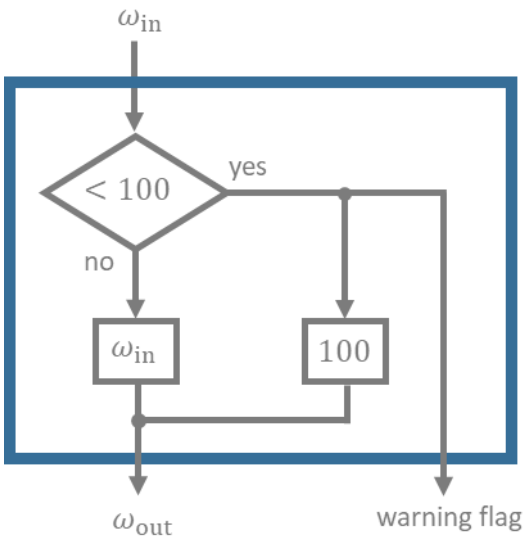

Fig. 53 Limiting minimum angular frequency

To show the usefulness of this block, the following example can be shown. In this situation the positive sequence PLL controller center frequency is set to 117.2 Hz and the inverter models' output is deactivated.

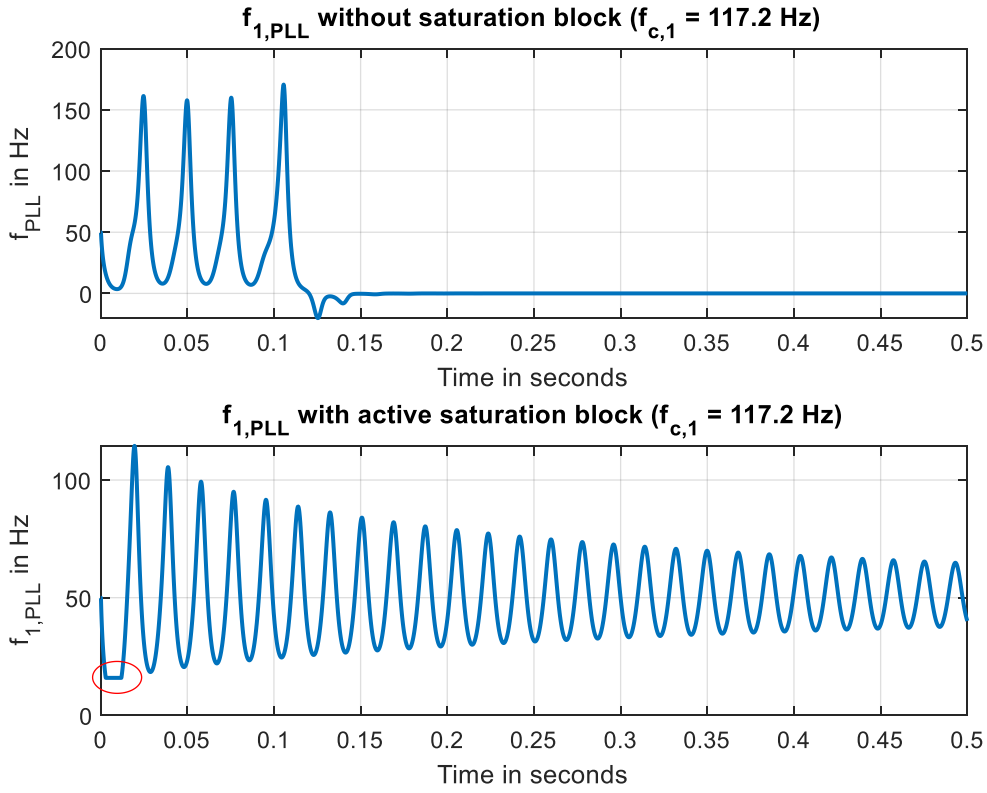

Fig. 54 Example for use of frequency limiting safety block

It can be seen, in the above plot, how this setting leads eventually to a frequency of zero, when no saturation is active. In the second subplot, right at the start at about 0.01 seconds, the saturation action can be recognised in the red ellipse. The frequency here, does not drop to zero, although approaches the rated angular frequency only accompanied with a strong oscillation. In this case the warning flag could be used to take into consideration a possible reduction of the controller center frequency.

Concluding it can be said that the shape of the PLL-signals during start-up mainly depend on the voltage offset angle and the PLL-PI-controller settings. In addition, it was shown, that high frequency oscillations can cause a diverging behaviour caused by the sequence decoupler, if no countermeasures are met. Compared to fault situations, which also offer phase jumps, the start-up process is totally independent of currents, since the current injection is only activated after PLL-start-up.

4.2 Criterion for PLL stability during faults

4.2.1 Analytical stability evaluation during faults [31, 47]

To understand the relation between PLL-stability and grid parameters, especially during three phase faults, the following reflections are necessary.

The structure consisting of inverter/current-source, grid impedances, a fault impedance and grid voltage source can be modelled easily in positive sequence. For symmetrical faults this representation is enough.

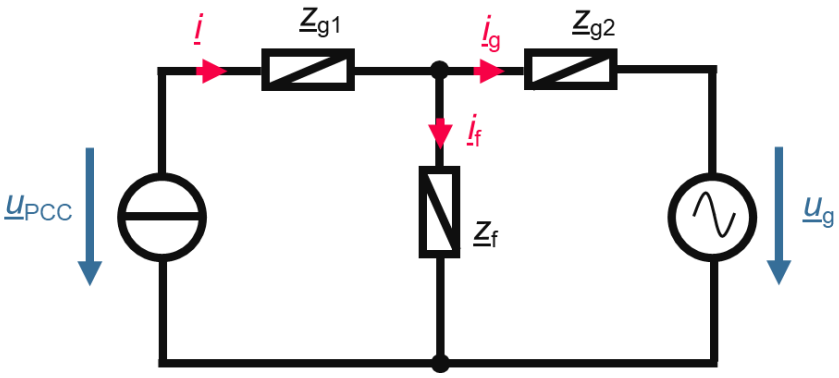

Fig. 55 Model of inverter, fault and grid

The current source models the inverter (or a whole park), z_{g1} and z_{g2} model line and grid impedances, while z_f models the fault path.

The following relations between voltages, currents and impedances can easily be derived:

$$\underline{u}_{\mathrm{PCC}} = \underline{i} \cdot \underline{z}_{\mathrm{g1}} + \underline{i}_{\mathrm{f}} \cdot \underline{z}_{\mathrm{f}} \tag{103}$$

$$\underline{u}_{\mathrm{PCC}} = \underline{i} \cdot \underline{z}_{\mathrm{g1}} + \underline{i}_{\mathrm{g}} \cdot \underline{z}_{\mathrm{g2}} + \underline{u}_{\mathrm{g}} \tag{104}$$

$$0 = \underline{i} - \underline{i}_{\mathrm{g}} - \underline{i}_{\mathrm{f}} \tag{105}$$

Solving this equation system leads to the following expression for the inverter terminal voltage u_{PCC}:

$$\underline{u}_{\mathrm{PCC}} = \underline{i} \cdot \underbrace{\frac{\underline{z}_{\mathrm{f}} \cdot \left(\underline{z}_{\mathrm{g1}} + \underline{z}_{\mathrm{g2}}\right) + \underline{z}_{\mathrm{g1}} \cdot \underline{z}_{\mathrm{g2}}}{\underline{z}_{\mathrm{g2}} + \underline{z}_{\mathrm{f}}}}_{\underline{z}_{\mathrm{g}}} + \underbrace{\frac{\underline{z}_{\mathrm{f}}}{\underline{z}_{\mathrm{f}} + \underline{z}_{\mathrm{g2}}}}_{\underline{K}_{\mathrm{g}}} \cdot \underline{u}_{\mathrm{g}} \tag{106}$$

In time-dependant phasor domain, this equation can be written as:

$$\underline{u}_{\mathrm{PCC}}(t) = i \cdot e^{\mathrm{j}(\theta_{\mathrm{i}}+\omega t)} \cdot z_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{z_{\mathrm{g}}}} + u_{\mathrm{g}} \cdot e^{\mathrm{j}(\theta_{u_{\mathrm{g}}}+\omega t)} \cdot K_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{K_{\mathrm{g}}}} \tag{107}$$

To change into dq-coordinate system, a multiplication with $e^{-\mathrm{j}\varphi_{\mathrm{PLL}}}$ is necessary.

When the PLL is locked, and φ_{PLL} equal to the angle of $\underline{u}_{\mathrm{PCC}}$, the $\underline{u}_{\mathrm{PCC}}$ in dq-system would be a set of constant values. To describe the PLL behaviour, this case wouldn't be beneficial. The voltage $\underline{u}_{\mathrm{g}}$ is taken as reference and therefore its angle set to zero. It is also assumed, that the inverter reference current equals the current source output current and can therefore easily be written in dq-system.

$$\underline{u}_{\mathrm{PCC,dq}}(t) = \underline{i}_{\mathrm{dq,ref}} \cdot z_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{z_{\mathrm{g}}}} + u_{\mathrm{g}} \cdot e^{\mathrm{j}(0+\omega t-\varphi_{\mathrm{PLL}})} \cdot K_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{K_{\mathrm{g}}}} \tag{108}$$

The only time dependant angle remaining is $\theta_{\mathrm{PLL}}(t) = \omega t - \varphi_{\mathrm{PLL}}(t)$.

The term ωt denotes here the angle at time t, of space vectors rotating with rated frequency, while $\varphi_{\mathrm{PLL}}(t)$ is the by the PLL computed instantaneous angle, which is used for dq-transformation.

$$\underline{u}_{\mathrm{PCC,dq}}(t) = \underline{i}_{\mathrm{dq,ref}} \cdot z_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{z_{\mathrm{g}}}} + u_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{PLL}(t)} \cdot K_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{K_{\mathrm{g}}}} \tag{109}$$

The term θ_{PLL} is then the difference of the previous two terms and can be understood as the integral of the output of the PLL-PI controller still before the feedforward summation with the rated frequency. In a schematic drawing this should be illustrated.

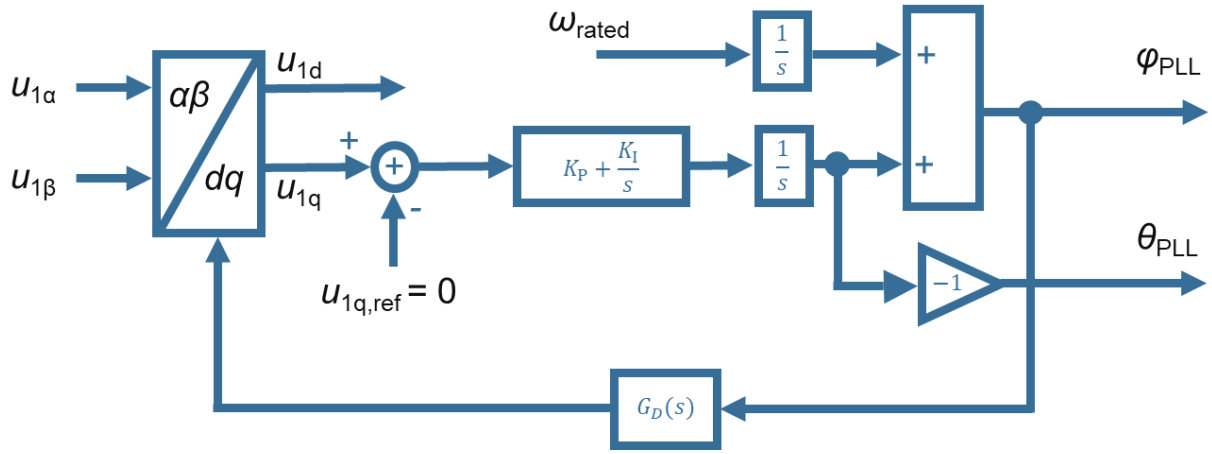

Fig. 56 Schematic explanation of different PLL-angles

For a stable settling process, typical signal curves should be shown for better understanding.

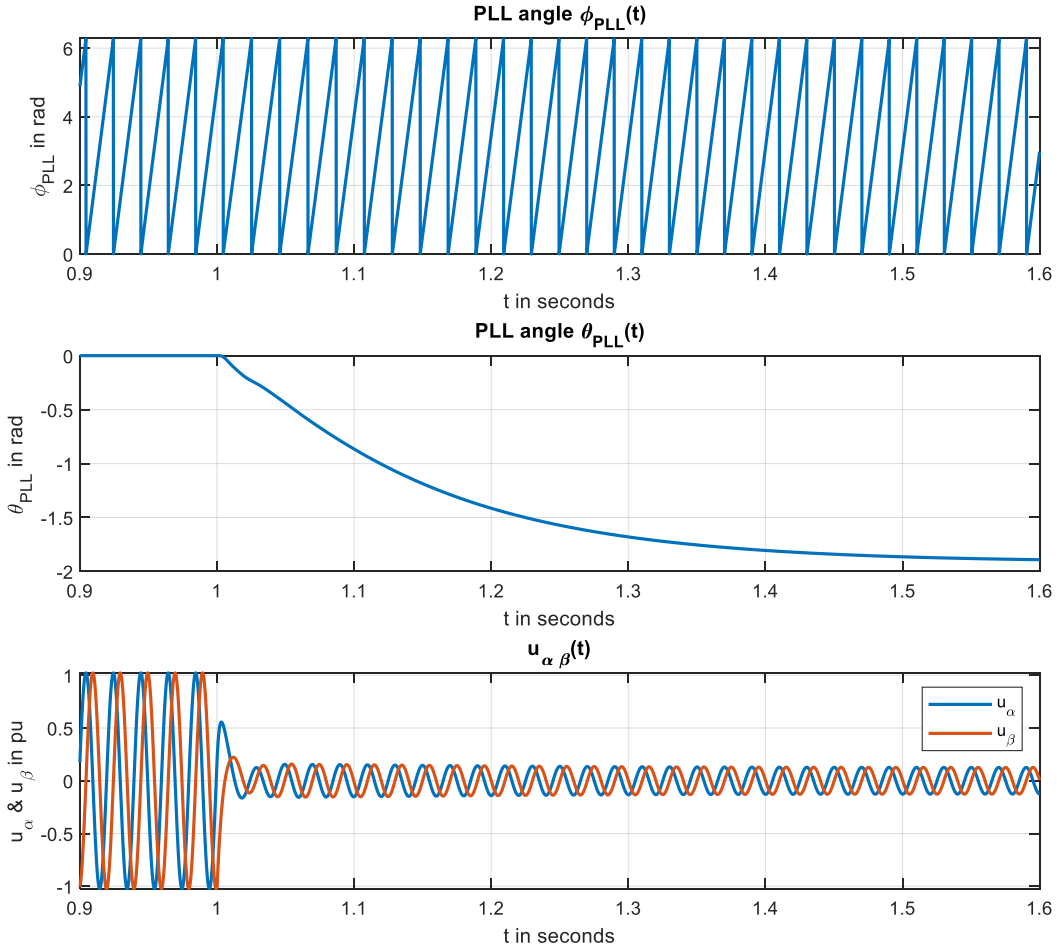

Fig. 57 Illustration of difference between φ_{PLL} and θ_{PLL}

In this situation at second 1.0 a three phase grid fault occurs, which causes a change in the waveform of $u_{\alpha\beta}$. Also the angle θ_{PLL} starts to change at the fault start time, since a grid fault normally also means a phase jump in the voltage waveform. After about 0.6 seconds of fault time the angle settles at a new steady state value. In the actual PLL-angle φ_{PLL} the fault start is not visible, since a major part of this angle consists of the integral of the constant feed-forward rated frequency.

The dynamic behaviour of the PLL is visible when observing the q-component of the voltage, which can easily be derived from the equation (103) above.

$$u_{\mathrm{PCC,q}}(t) = \underbrace{|\underline{i}_{\mathrm{dq,ref}}| \cdot |\underline{z}_{\mathrm{g}}| \cdot \sin(\theta_{\mathrm{i,dq,ref}} + \theta_{\mathrm{z_g}})}_{m_c} + \underbrace{|\underline{u}_{\mathrm{g}}| \cdot |\underline{K}_{\mathrm{g}}|}_{m_g} \cdot \sin(\theta_{\mathrm{PLL}}(t) + \theta_{\mathrm{K_g}}) \qquad (110)$$

An equilibrium point or simpler steady state behaviour can only be reached, if $u_{\mathrm{PCC,q}}$ gets zero.

Assuming m_{c} to be constant (since only dependant on current reference and constant impedances), $u_{\mathrm{PCC,q}}$ may have the following look:

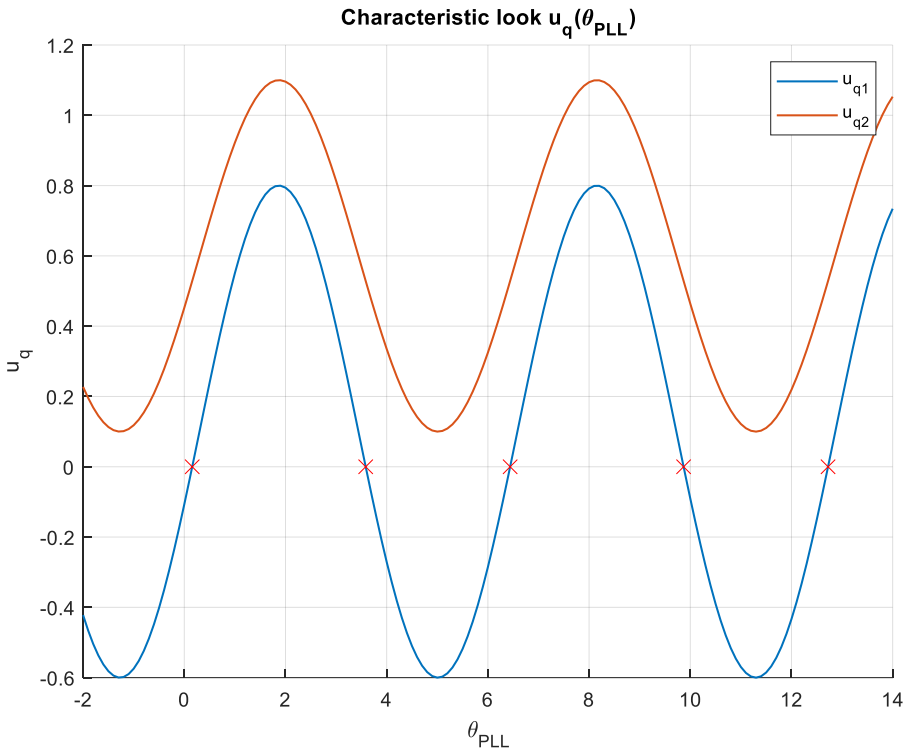

Fig. 58 Dependency between u_{q} and θPLL

It can be seen, how the setting in u_{q2} leads to no equilibrium point (u_{q} = 0), while u_{q1} crosses the zero line periodically (equilibrium points marked with red cross). To divide the u_{q1} equilibrium points into stable and unstable ones, the observation of schematic Fig. 56 is necessary. A positive u_{q} after being PI-controlled and integrated, reduces the value of θ_{PLL}. Now considering a small deviation of u_{q} from zero away, it can be stated that those equilibrium points are stable, where the derivative of u_{q} with respect to θ_{PLL} is positive, since a small deviation in voltage always leads eventually back to the stable starting point.

To estimate the existence of equilibrium points, the following consideration is required:

$$u_{\mathrm{PCC,q,equi}} = 0 = m_c + m_g \cdot \sin(\theta_{\mathrm{PLL,equi}} + \theta_{\mathrm{K_g}}) \qquad (111)$$

$$\rightarrow \theta_{\mathrm{PLL,equi}} = \arcsin\left(-\frac{m_c}{m_g}\right) - \theta_{\mathrm{K_g}} \qquad (112)$$

To assure that this is possible, m_{c} and m_{g} have to be in such a range, that a variable θ_{PLL} can always lead to a total value of zero.

To assure a real valued angle, the magnitude of the *arcsin* argument has to be limited to 1.

Therefore, the following has to be true:

$$\left|\frac{m_c}{m_g}\right| = \frac{|m_c|}{m_g} \leq 1 \tag{113}$$

This criterion can be used to check the existence of an equilibrium point. It only contains values dependant on current reference value, grid impedances, fault impedances and grid voltage (typically 1 p.u.). It does not give information about how the transition between two different equilibrium points works dynamically and can therefore not assure safely stable PLL-operation, since the dynamic behaviour also depends on the PI-controller parameters. Therefore, if the criterion indicates a stable operating condition, it does not mean, that in this situation the stable operating point can also be found. On the other side if the criterion indicates the non-existence of a stable operating point, also the simulation should run into an instability.

4.2.2 Simulation examples and verification of derived criterion

From the previously shown medium voltage PV-park model the transformer, the LV-cabling, as well as line capacitors are omitted, which ends in an inverter model directly connected to an insulated 20 kV-grid.

In this section, the derived criterion should be applied and verified.

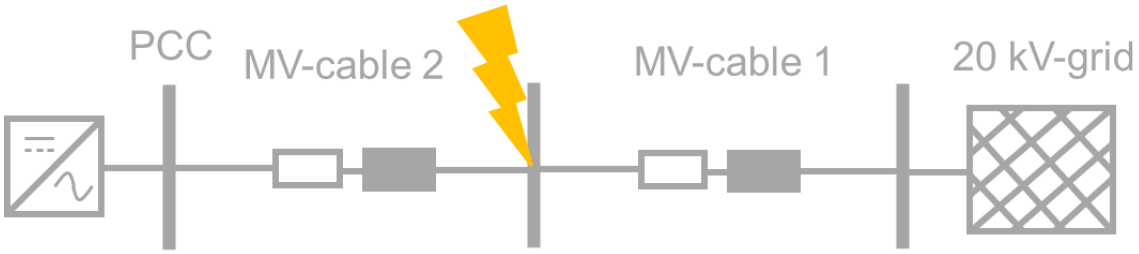

Fig. 59 Grid model to investigate stability during faults

To cause a PLL-instability during a three-phase fault between the two cables, the following settings are found, which will be the default settings for this chapter.

Table 3: Model setting for verification simulations

MV-grid connection		
U_n	20	kV
S_{grid}	1.5	MVA
$\|Z_{grid}\|$	267	Ω
KXR	7	-
X_{grid}	264	Ω
R_{grid}	37.7	Ω
MV-cable 1		
length	1	km
$r_1' + jx_1'$	0.075 + j0.1	Ω/km
MV-cable 2		
length	5	km
$r_1' + jx_1'$	0.075 + j0.1	Ω/km
Inverter		
P_{rated}	1	MW
U_{rated}	20	kV
f_c (PLL-PI setting positive sequence)	10	Hz
P_{ref} (Pre-fault Reference power)	No load	p.u.
Reactive current injection ratio k	2	-
Three Phase fault		
$R_f + jX_f$	1 + j0	Ω

The drastic reduction of the short circuit capacity of the grid from initially 1 GVA to little more than the rated inverter power is necessary to observe PLL-instabilities during faults, since they are uncommon in strong grids, which is explained later while evaluating the derived criterion. Also, the length of the cable connecting the inverter to the grid is extended to assure an unstable situation.

4.2.2.1 Unstable default case

As already mentioned, this setting leads to an undesired inverter behaviour during the fault. This can especially be observed in the plots of PLL-frequency and q-component voltage.

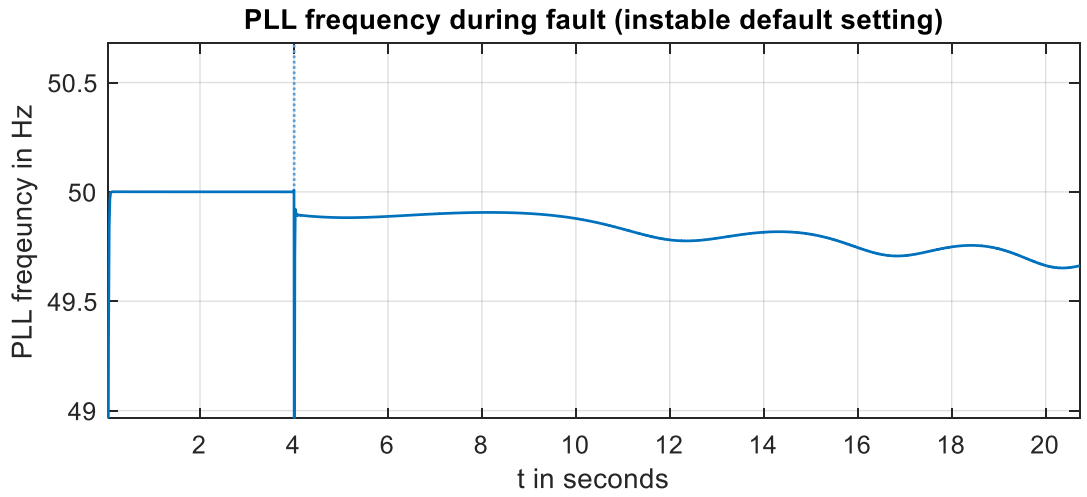

Fig. 60 PLL frequency (unstable default case)

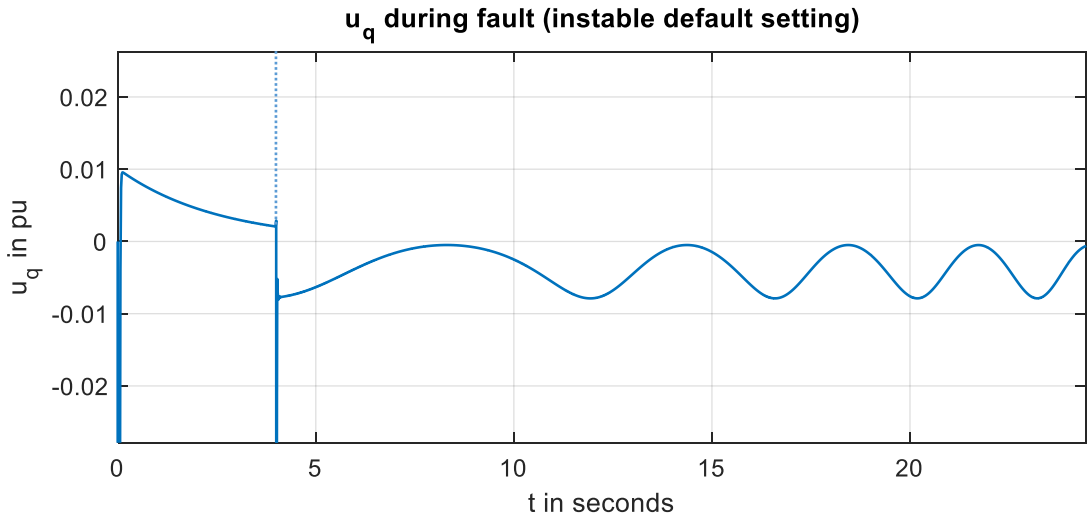

Fig. 61 u_q during fault (unstable default case)

As it can be seen in the plots above, after a start-up process the PLL works properly until the fault start at 4 seconds. Before the fault is active, the PLL frequency is at the rated frequency of 50 Hz and also the q-component of the voltage (positive sequence) seems to be converging against zero. Then at the time 4 seconds, a three phase fault causes the PLL frequency, as well as u_q, to drop massively. This happens due to the voltage jump, typical for grid faults. After the drop, both values rise again, but don't reach the pre-fault level. The frequency stops somewhere between 49.5 and 50 Hz and starts to

decrease again, overlayed by an oscillation. During the fault the voltage u_q doesn't reach the desired value of zero. It seems that this grid-fault setting doesn't offer an equilibrium point.

In the frequency plot it can be seen how the frequency differs only by 0.3 Hz from the rated value after an unrealistic long fault time of about 16 seconds, although this observed fault is a major grid fault with a remaining voltage at the inverter terminal of 0.01 p.u.

Therefore, to demonstrate this unstable behaviour in a more eye-catching way, the PLL-PI-controller is changed from the default setting (f_c = 10 Hz) to a way more aggressive setting of f_c = 30 Hz. To illustrate the difference between those two settings, equations (41) and (42) can be used to identify an increase of the proportional controller element by a factor 3, while the integrating constant increases by even a factor of 27.

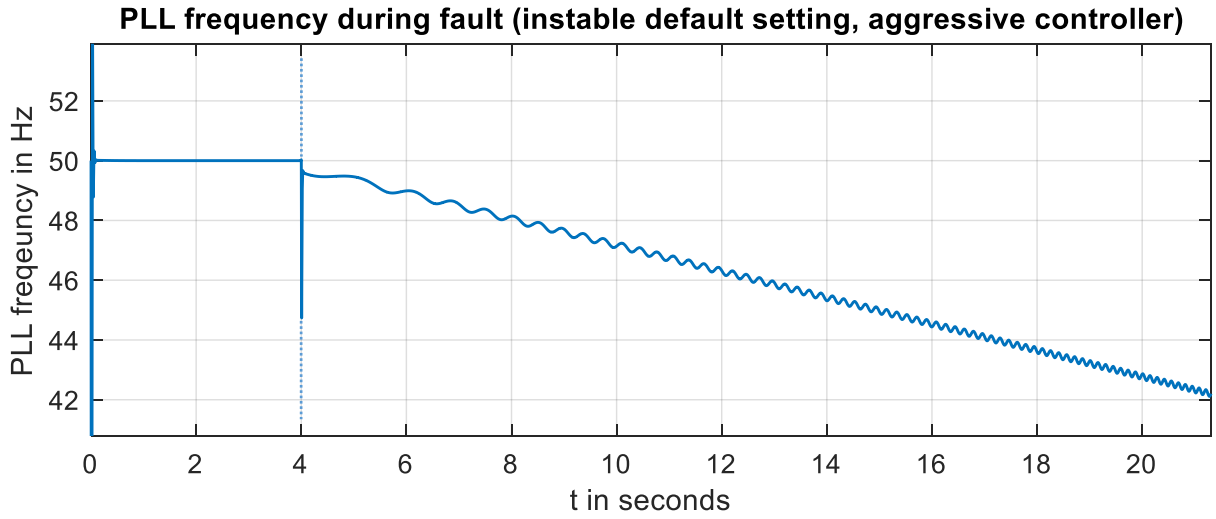

Fig. 62 PLL-frequency with aggressive PI-controller setting

With the more aggressive setting, the frequency moves away much faster during the fault.

With such a behaviour no control functions can be accomplished since the mathematical link between grid voltages and currents to internal modelling signals is invalid. Such a behaviour for longer time has strictly to be avoided and is therefore monitored by different protection units in hard- and software.

Using the before derived criterion this instability could be predicted, if like in this case all grid impedances are known.

Before evaluating the impedance dependant constants, the used impedances have to be transformed into per-unit values. In the whole simulation model as base-values the peak values of nominal phase-to-ground voltage, as well as peak nominal current are used, since this choice is beneficial when dealing with instantaneous values.

Table 4: Base Values for p.u.-calculation

P_{rated}	U_{rated} (RMS)	I_{rated} (RMS)	U_{base}	I_{base}	Z_{base}
MW	kV	A	kV	A	Ω
1	20	28.87	16.33	40.83	400

Since this severe symmetrical fault causes a massive voltage collapse, the whole available current has to be used as positive sequence reactive current. The grid voltage remains always 1 p.u.:

Table 5: Voltage and current values

$\underline{i}_{dq,ref}$	$\lvert\underline{v}_g\rvert$
p.u.	p.u.
1.2 ∠-90°	1

Applying the relations of eq. (106) to the p.u.-impedances, leads to the following constants:

Table 6: Impedance dependent constants

$\underline{z}_g$	$\underline{K}_g$
p.u.	-
0.0037 ∠20.13°	0.0037 ∠-81.64°

Now, applying eq. (110) onto the values of Table 5 and Table 6 leads to the evaluation of the criterion:

$$\left|\frac{m_c}{m_g}\right| = \frac{\left|\underline{i}_{dq,ref}\right| \cdot \left|\underline{z}_g\right| \cdot \sin(\theta_{i,dq,ref} + \theta_{zg})}{1 \cdot \left|K_g\right|} = 1.13 > 1 \tag{114}$$

The result of eq. (114) indicates the non-existence of an equilibrium point. The PLL can therefore not run stably during a fault with this setting.

4.2.2.2 Change of fault resistance

In this case from the default settings just the fault resistance is changed from 1 to 20 Ohm.

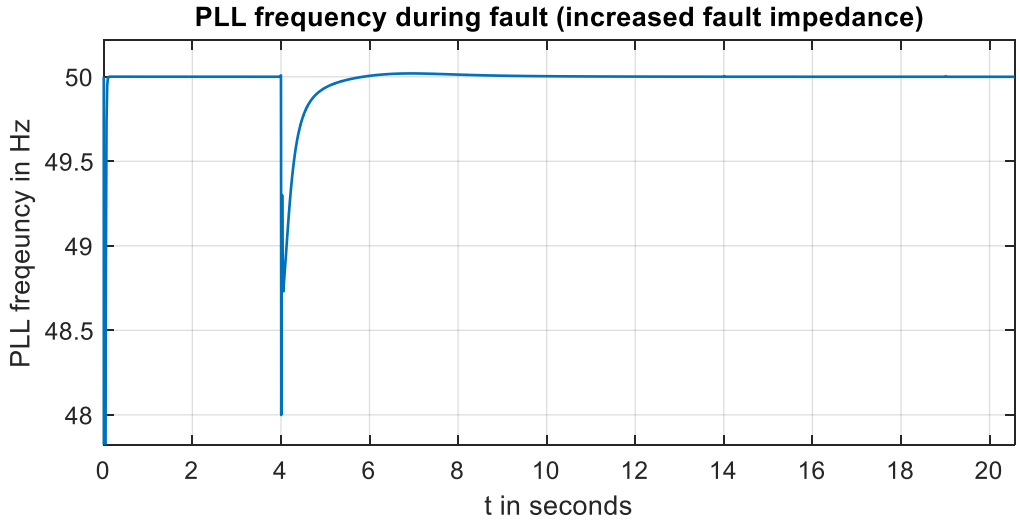

Fig. 63 PLL frequency during fault (Rf = 20 Ohm)

With the higher fault resistance, the PLL is able to control the frequency to the rated frequency also during the fault. Again, with the criterion this stable operating condition can be predicted.

The higher fault resistance changes the relevant constants:

Table 7: Results for 20 Ohm setting

$\underline{z}_g$	$\underline{K}_g$	$\lvert m_c/m_g \rvert$
p.u.	-	-
0.0504 ∠5.54°	0.0740 ∠-77.66°	0.81

Since, the criterion also depends on impedance angles, not always a higher fault impedance magnitude reduces the risk of instability. Evaluating the criterion for different impedance values, the following plot can be generated.

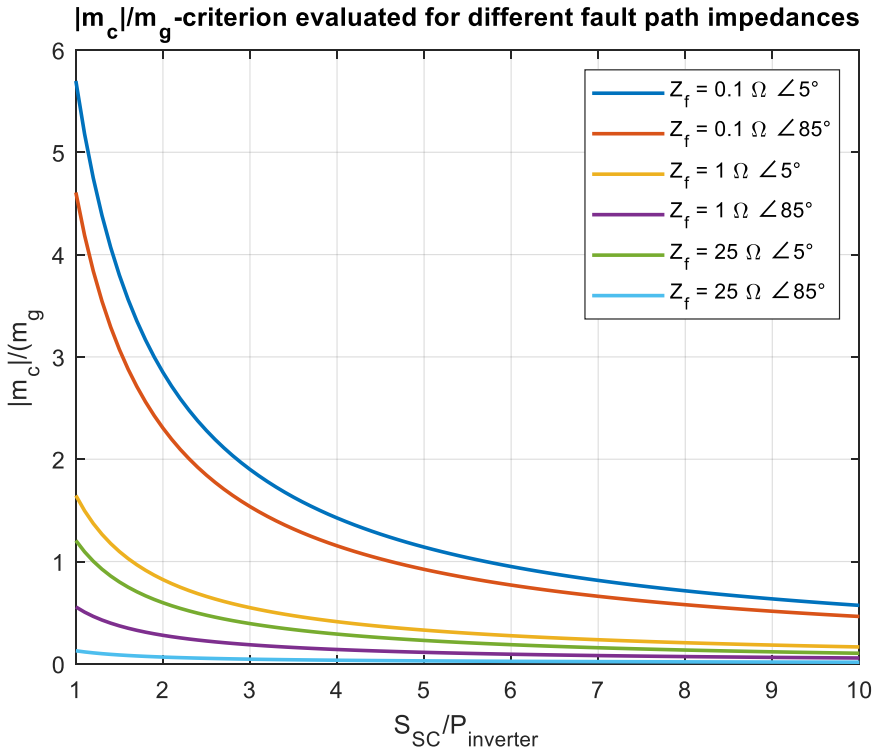

Fig. 64 |mc|/mg for different impedance values, reactive injected current

As it can be seen in Fig. 64, the 0.1 Ω setting, shows higher risk for instability, compared with situations, where the magnitude of $\underline{z}_f$ is higher. When comparing the green (25 Ω, 5°) and the purple graph (1 Ω, 85°), this trend is not followed anymore. Here the higher impedance magnitude leads to more critical situations, due to the lower phase angle. It can be therefore stated, that above a magnitude-threshold, also the impedance angle has strong influence on the result of the $|m_c|/m_g$-evaluation.

4.2.2.3 Change of grid short circuit level (higher S_{SC})

Now, compared to the default settings, the short circuit level of the MV-grid connection is changed from 1.5 to 5 MVA.

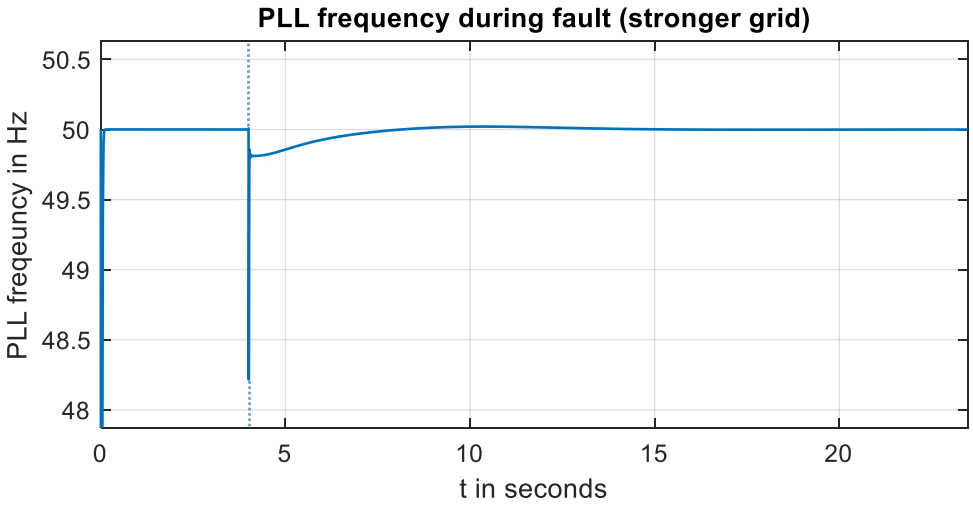

Fig. 65 PLL frequency during fault (S_{SC} = 5 MVA)

Similar to the increase of fault resistance, also an increase in short circuit capacity leads to a stable fault behaviour.

The change of short circuit level inherently changes grid impedance and therefore also $\underline{z}_g$ and $\underline{K}_g$.

Table 8: results for stronger grid infeed

$\underline{z}_g$	$\underline{K}_g$	$\lvert m_c/m_g \rvert$
p.u.	-	-
0.0037 ∠20.46°	0.0125 ∠-81.12°	0.33

That an increase of grid short circuit level has positive influence in PLL-stability can be explained in a simple manner. In a stronger grid a fault causes a smaller voltage dip, compared to a weak grid condition. A smaller voltage dip is beneficial for PLL-operation since less effort is necessary to control u_q back to zero. Partly this explanation applies also to an increased fault impedance, although in that case the impedance angle has also strong influence.

Although, the influence of the short-circuit power influences the $|m_c|/m_g$-criterion in multiple ways (z_{g2} included in m_c and m_g), a clear trend can be observed, when observing, the previous Fig. 64, where an increase in short circuit level always resulted in a decreased instability risk.

4.2.2.4 Injection of only active current

As it is obvious, when looking at eq. (110) and (114), also the phase angle of the injected current has influence on the PLL-stability. Although it is not possible to say in general, which angle could be advantageously since this is dependent on the angle of z_g. (see eq. (110))

In this grid topology, when changing, compared to the default case, the current injection from a pure reactive current to a pure active current, the operation becomes stable.

Table 9: Results for changed injection current angle

$\underline{z}_g$	$\underline{K}_g$	$\underline{i}_{dq,ref}$	$\lvert m_c/m_g \rvert$
p.u.	-	p.u.	-
0.0037 ∠20.46°	0.0125 ∠-81.12°	1.2 ∠0°	0.41

Varying the angle of the complex fault path impedance, as well as the phase angle of the injected current, the following results can be achieved.

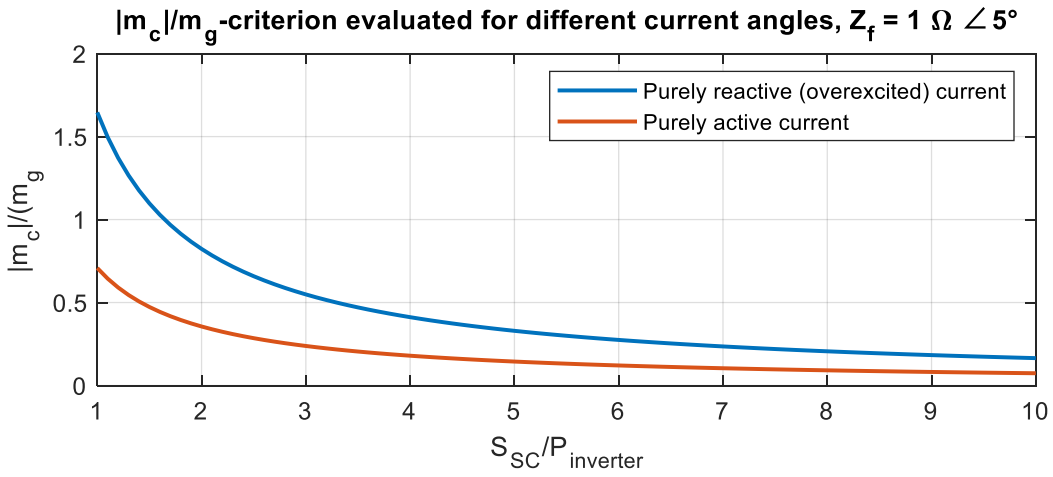

Fig. 66 $|m_c|/m_g$-criterion for 5° impedance angle

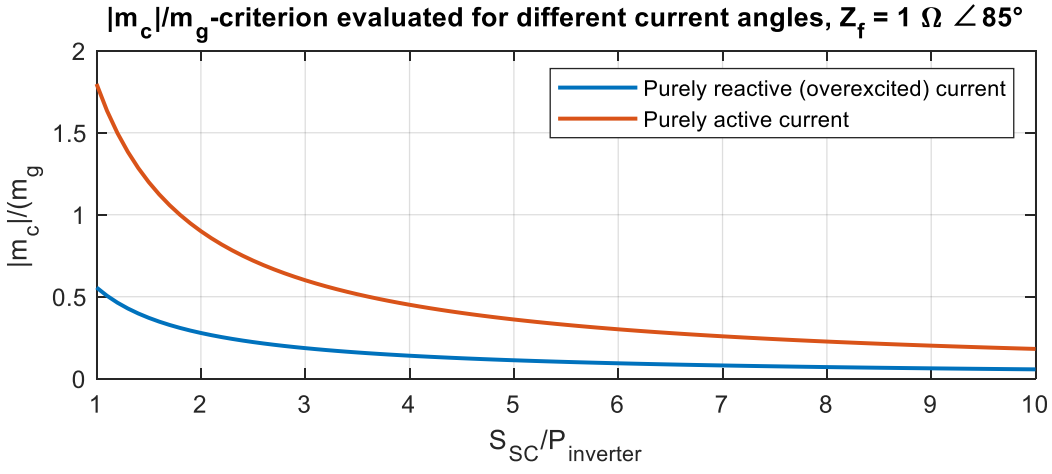

Fig. 67 $|m_c|/m_g$-criterion for 85° impedance angle

As visible in Fig. 66 and Fig. 67, dependent on the angle of the relevant impedances, either reactive or active current offer higher possibility for instability due to a non-existing PLL-operating point.

4.2.3 Conclusion

As mentioned earlier this criterion can be used in an easy way, to estimate if an equilibrium PLL operating point exists in a certain symmetrical situation. This analysis can although be extended to unsymmetrical faults, when the derivation is applied to positive and negative sequence [32].

In practice, values such as fault impedance are rather hard to estimate, which causes uncertainty when working with this method.

In general, PLL stability is very often (for example in [54]) compared to synchronous generator angle stability. When assuming inductive line impedance the transferable active power over a line can be assumed to be of the following structure.

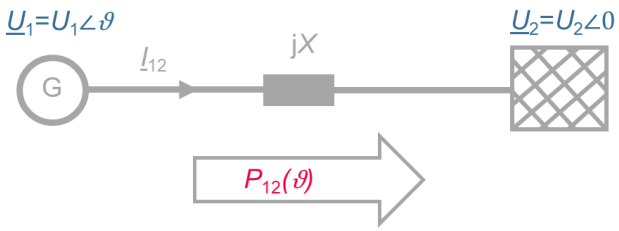

Fig. 68 Active power flow from generator into grid

$$P_{12}(\vartheta) = \frac{U_1 \cdot U_2}{X} \cdot \sin(\vartheta) \leq \frac{U_1 \cdot U_2}{X} \tag{115}$$

Apparently, the transferable active power is limited, and the maximum value depends on voltages and impedance. If now the mechanical input power of the generator exceeds the maximum transferable power, the exceeding energy is used to accelerate the rotating mass, which means also an increase of the phase angle ϑ.

To come back to the PLL, the criterion described in this chapter, can somehow be compared to checking if the mechanical input power exceeds the maximum transferable power and if an equilibrium point exists. If in PLL operation no operating point exists, where u_q can become zero, the PLL-frequency will either rise or fall.

Although, to check PLL-stability in dynamic transition processes, such as faulty to healthy grid transition a more sophisticated approach is necessary. Again, there exists an easy analogue in the world of synchronous machines (SM), namely the ‘Equal Area criterion’.

A big difference between PLL stability and SM-angle stability, is that in PLL operation periodically new stable points occur, and it could happen, that after fault clearance ‘another’ stable point is reached. In the world of synchronous machines such a situation is avoided by pole slip protection devices to prevent from damages.

4.3 Dynamic stability analysis

Since the existence of a stable operating point is not a sufficient condition for stable operation, a more detailed investigation, including the PLL settings, is necessary. To check, how long a grid fault, causing PLL instability, can be applied, to assure stable PLL operation after fault clearance, is for example a way more complex task, than the simple check for existence of equilibrium points. Besides the grid configuration, during this dynamic process, the PI-controller in the PLL logic, has a huge impact, since the controller settings affect the relation between u_q and $\Delta\omega_{PLL}$.

In this chapter a brief idea should be given, how dynamic PLL-stability investigations could be carried out.

Again, the following structure should be used, in this case to describe the PLL-dynamics by a state space model.

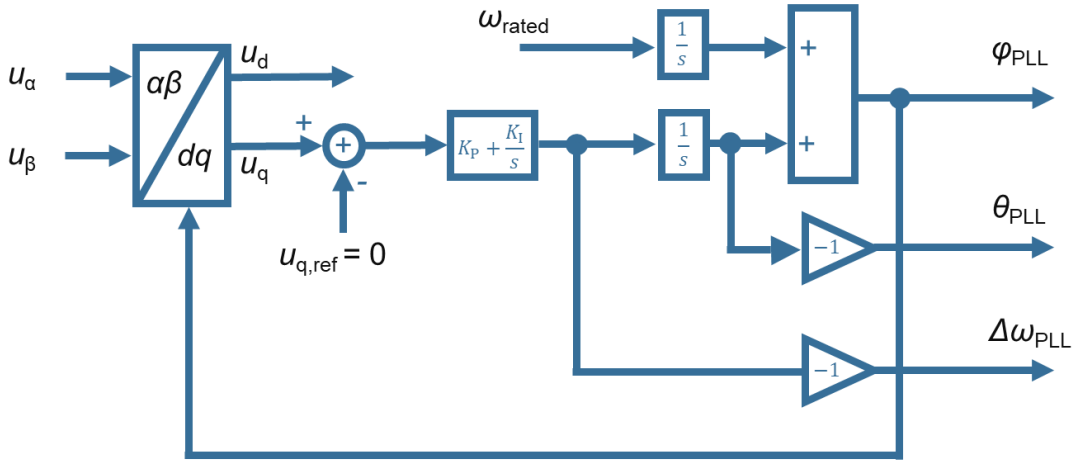

Fig. 69 PLL structure for state space model derivation

The computed voltage u_q can again be calculated according to eq. (110):

$$u_q(t) = m_c + m_g \cdot \sin(\theta_{PLL}(t) + \theta_{K_g}) \tag{116}$$

The difference angular frequency $\Delta\omega_{PLL}$ can then be computed as the output of the PI-controller:

$$\Delta\omega_{PLL}(t) = -K_P \cdot u_q(t) - K_I \cdot \int u_q(t)\,dt \tag{117}$$

The angle θ_{PLL} is:

$$\theta_{PLL}(t) = \int \Delta\omega_{PLL}(t)\,dt \tag{118}$$

Now, choosing θ_{PLL} and $\Delta\omega_{PLL}$ as state variables, the following state space model can be set up:

$$\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \begin{bmatrix} \theta_{PLL}(t) \\ \Delta\omega_{PLL}(t) \end{bmatrix} \tag{119}$$

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} x_2(t) \\ -K_P \cdot m_g \cdot cos(x_1(t) + \theta_{K_g}) \cdot x_2(t) - K_I \cdot \left[m_c + m_g \cdot \sin(x_1(t) + \theta_{K_g}) \right] \end{bmatrix} \tag{120}$$

With this simple model, numerical analyses can be executed with a greatly reduced computational effort.

Although, this approach only considers positive sequence and can therefore only be used for symmetrical conditions. An extension to unsymmetrical conditions is possible.

For example, it would be interesting to know, for which starting state vector $x(t)=[x_1(t), x_2(t)]$, the system described by PLL parameters K_P, K_I and by grid- and current-dependant constants, converges.

In such a way, it could be stated for example, which fault ending time or fault impedance, leads to a stable operating point after fault clearance.

The system described in (120), could be simulated for different initial values and the system response could be used to decide on stable or unstable operation.

The converging region, plotted on x_1-x_2-plane is called *domain of attraction* (DOA).

As an example, a simplified DOA should be created and compared to simulation examples. Compared to the model described in Table 3, the following settings are varied:

- Positive sequence PLL-PI controller center frequency is changed from 10 to 50 Hz
- Fixed current injection, i_{1d} = 1.0 pu, i_{1q} = 0.0
- SOGI deactivated, $u_{\alpha\beta}$ fed directly to positive sequence park transformation block
- Minimum frequency saturation block omitted (not necessary without SOGI)
- MV2-cable length extended to 20 km
- Short circuit level reduced to S_{grid} = 1.0 MVA
- Fault resistance = 25 Ω

For different starting values (x_1 and x_2) in MatLab the System (eq. (120)) is simulated for 20 seconds with a fixed-step solver. When at the end of simulation time the magnitude of state $x_2 = \Delta\omega_{PLL}$ is higher than 0.1 rad/s, then the setting is declared unstable/non-converging. At the end a x_1-x_2-heatplot is generated, where the colour indicates if the previously described criterion decided on stable or unstable situation. In contrast to this simplified and computationally inefficient method, in scientific world mathematical methods, such as Lyapunov [33] or Monte-Carlo simulations are used.

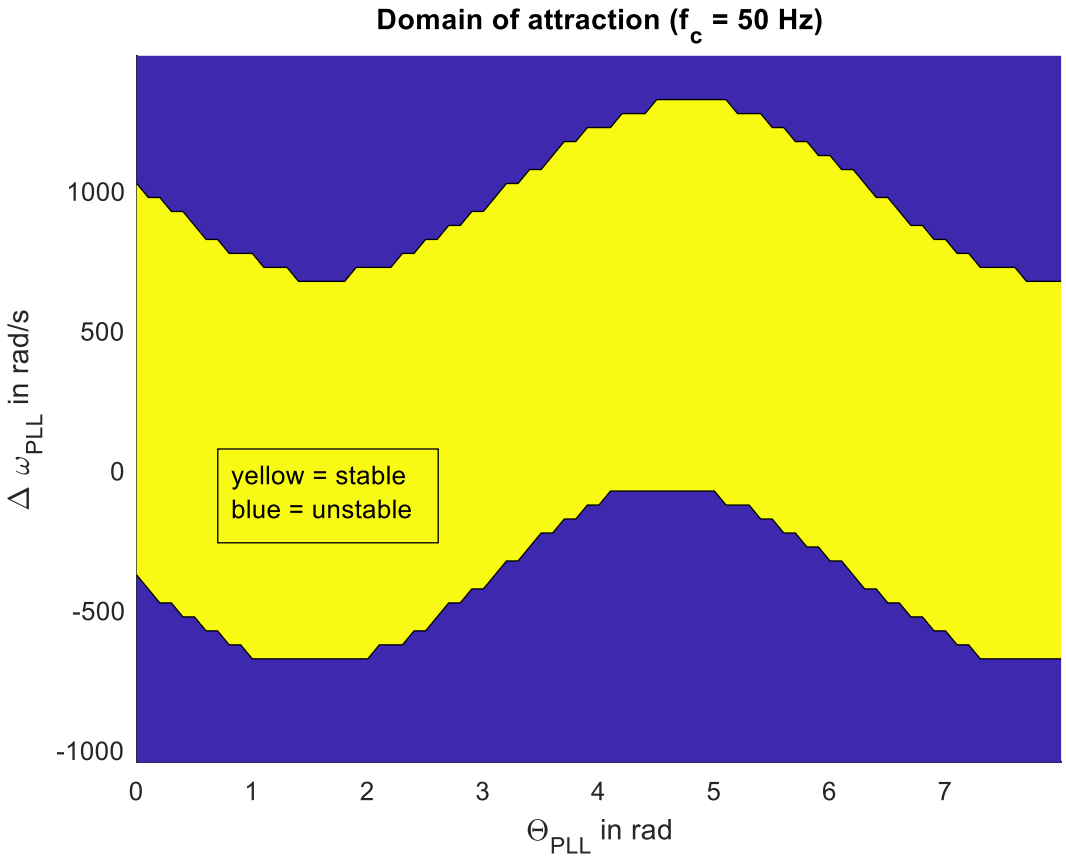

Fig. 70 Domain of attraction

In Fig. 70, it can be seen, that stable areas arise periodically, as mentioned earlier. Now it would be interesting, how accurate this simplified model is, compared to different detail stages of the actual model.

A first comparison should be carried out, using a model, which does not use a circuit simulation to compute the terminal voltages, but rather uses directly the PLL-computed angle to determine the terminal voltage (called *method 1*).

With equation (107) the terminal voltage can be computed, which consists of a part directly influenced by the inverter's current injection and one part dependent on grid configuration.

$$\underline{u}_{\mathrm{PCC}}(t) = \underbrace{\underline{i} \cdot e^{\mathrm{j}(\theta_{\mathrm{i}}+\omega t)} \cdot z_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{z_{\mathrm{g}}}}}_{inverter's\ influence} + \underbrace{u_{\mathrm{g}} \cdot e^{\mathrm{j}(\theta_{u_{\mathrm{g}}}+\omega t)} \cdot K_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{K_{\mathrm{g}}}}}_{grid's\ influence} \tag{121}$$

Since in this example the output current is a fixed value and not dependent on voltage measurement values, it can be written as:

$$\underline{i} = i \cdot e^{\mathrm{j}(\theta_{\mathrm{i}}+\omega t)} = |i_{\mathrm{dq,ref}}| \cdot e^{j\theta_{\mathrm{i,ref}}} \cdot e^{j\varphi_{\mathrm{PLL}}} \tag{122}$$

$$\underline{u}_{\mathrm{PCC}}(t) = |i_{\mathrm{dq,ref}}| \cdot z_{\mathrm{g}} \cdot e^{\mathrm{j}(\theta_{\mathrm{i,ref}}+\varphi_{\mathrm{PLL}}+\theta_{z_{\mathrm{g}}})} + u_{\mathrm{g}} \cdot e^{\mathrm{j}(\theta_{u_{\mathrm{g}}}+\omega t)} \cdot K_{\mathrm{g}} \cdot e^{\mathrm{j}\theta_{K_{\mathrm{g}}}} \tag{123}$$

By taking the imaginary part of this expression, a time-domain signal is extracted. For symmetrical situations this represents the phase *L1* and can be transferred to the other two phases via shifting by ±120°. In this way, the dynamic behaviour of the discrete PLL implementation can be illustrated in a simple simulation model. By changing from one set of grid configuration dependent constants to another,

a transition from a healthy to a faulty situation and vice-versa can be modelled, while the form of the equation used to get from the PLL-angle to the terminal voltage stays the same. Although, it has to be mentioned, that this transition is modelled totally without transients coming from the switching process between different states or at the fault start and end process.

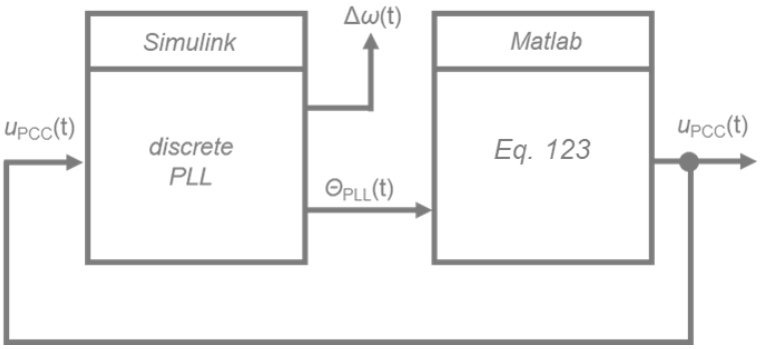

Fig. 71 Method 1

In a first test, a three-phase fault should be activated at 2.133 seconds, the fault is cleared after 100 ms at 2.233 seconds and the results show clearly stable operation after fault clearance.

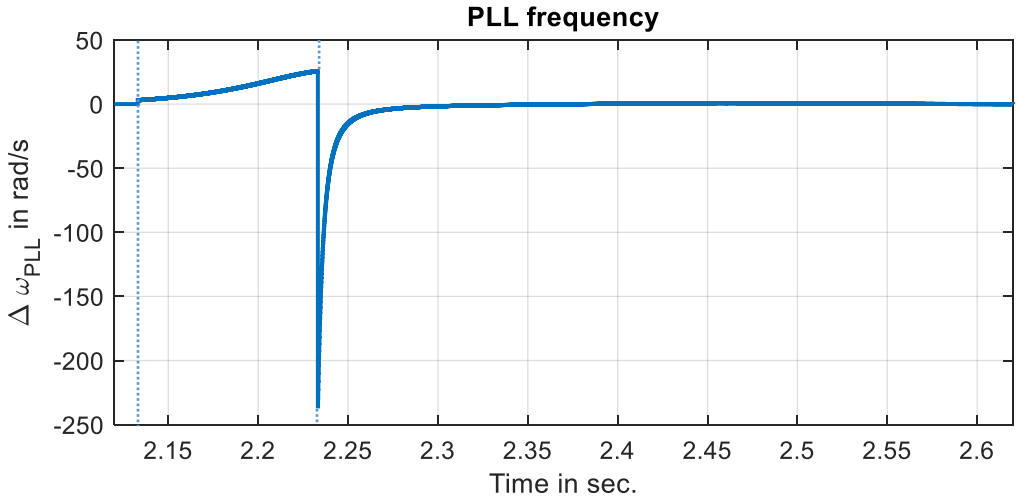

Fig. 72 PLL frequency during stable situation (method 1)

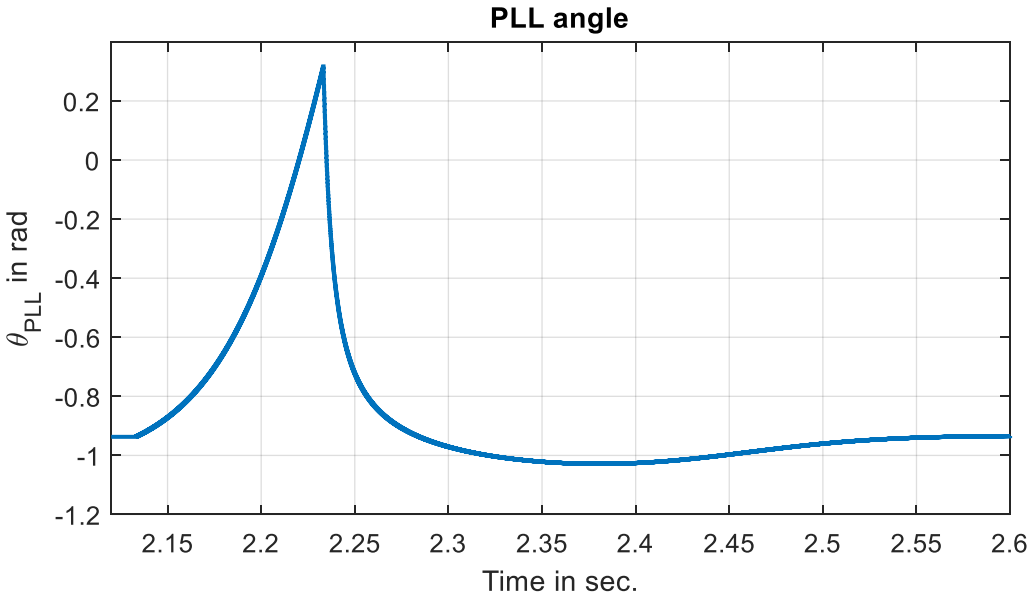

Fig. 73 PLL angle during stable situation (method 1)

It can be seen, how before the fault is active, the PLL works in steady state, Θ_{PLL} is constant and $\Delta\omega_{PLL}$ is zero. Then at fault start, the computed frequency is abruptly increased. During the fault both states change, and the trajectory moves away from the initial values. Apparently, this fault condition brings the PLL in difficulties, since until fault clearance no steady state is achieved. At fault clearing time (2.233 s) the frequency shows a massive drop and also the angle changes rapidly from increasing to decreasing. From there the trajectory moves into steady state in the course of a settling process.

Now it should be checked if the behaviour of this setting corresponds to the predictable behaviour deduced from the DOA. Plotting the *Θ*-*Δω* trajectory on the DOA plot, leads to:

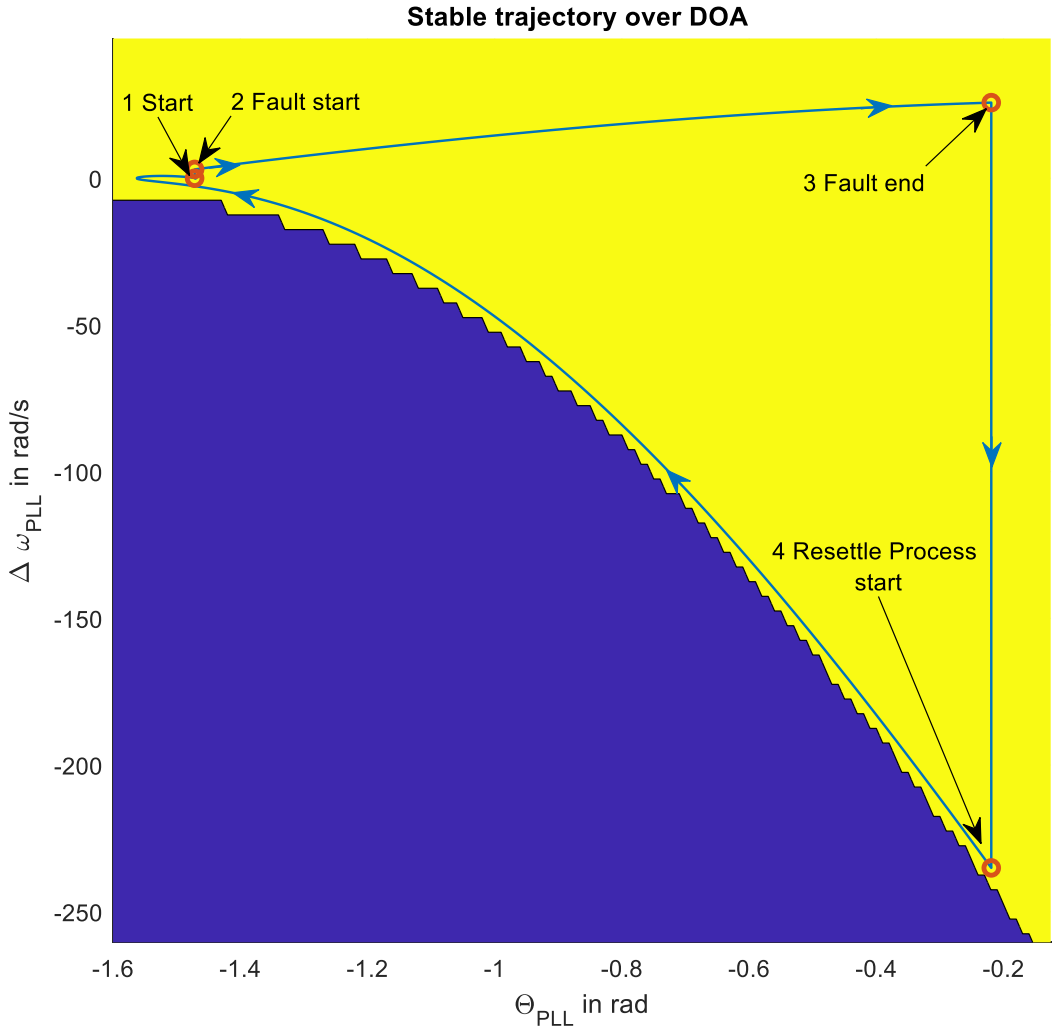

Fig. 74 Stable trajectory over DOA (trajectory computed with method 1)

It can be observed how the trajectory jumps at fault end but stays inside the yellow (stable, converging) area. Therefore, also the DOA method indicates a stable fault clearance.

As it can be seen in the last few plots, apparently the PLL-frequency is not continuous during transitions. When the structure of the system changes (healthy to faulty and vice-versa) jumps can be observed. This gets clear, when remembering the control structure of the PLL. When for example the impedance changes from one moment to another, also the voltage changes abruptly, when no filters or capacitors are considered. The jump in voltage is also visible in the computed q-component of the voltage, when the slightly inert SOGI-block is omitted, as did here. The q-voltage is fed to the PLL-PI-controller, where the proportional part of the controller transfers the jump in voltage to a jump in computed frequency. This explains the discontinuity in frequency. On the other hand, the computed PLL-angle has no discontinuities since it is directly the output of an integrator.

This must be considered when modelling the system purely through differential equations (called *method 2*). The initial conditions during the transitions at system changes, have to comply with the mentioned (dis-)continuities. To set all initial conditions the system must be split again, to achieve two additional states. Namely, in addition to the PLL angle and frequency, also the separate outputs of the PI-controller, the P- and the I-parts are used as state variables. With this method it is possible to simulate the PLL dynamics through a simple and easy-to-handle system. The results are the same, as with the before used discrete Simulink-PLL and phasor domain calculation to achieve the voltage signal. This second method is mainly used to check, whether the PLL dynamics of the discrete model in method 1, can be described accurately enough in an alternative way, without Simulink environment.

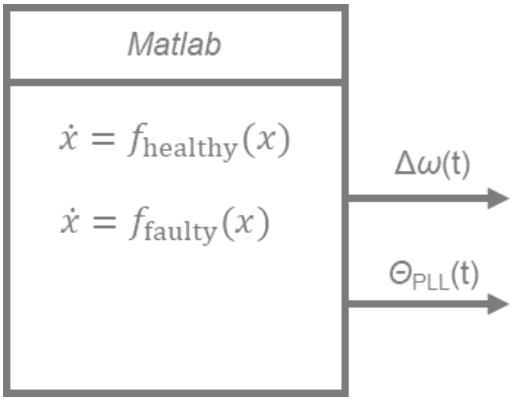

Fig. 75 Method 2

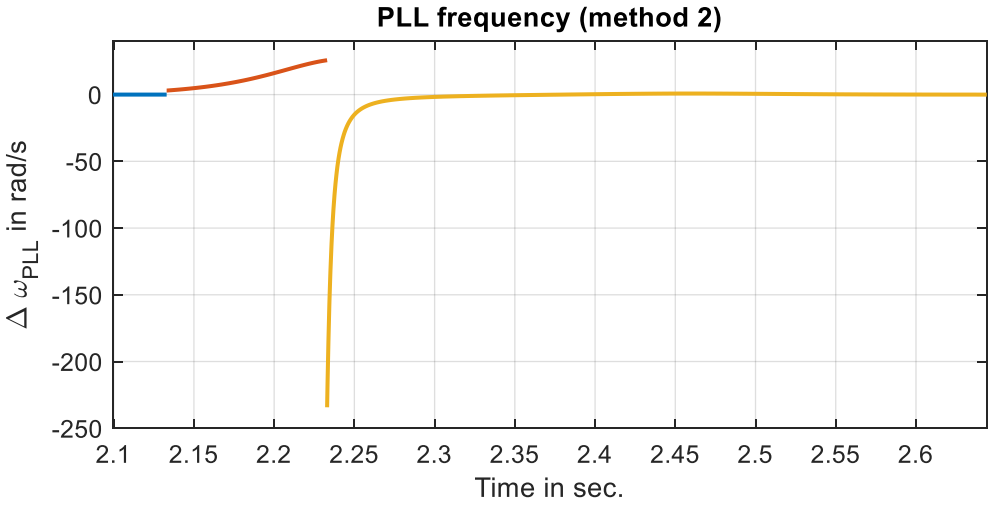

Fig. 76 PLL frequency (method 2)

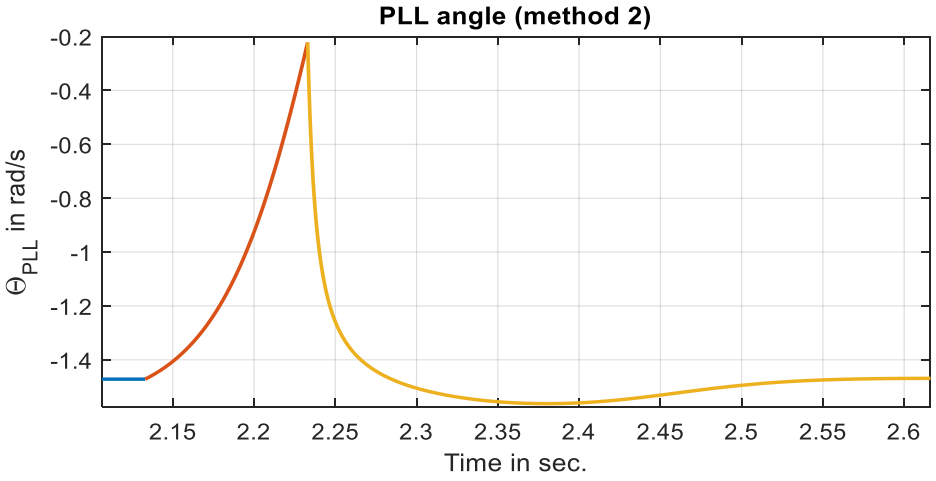

Fig. 77 PLL angle (method 2)

The three different plot lines indicate that these plots were generated by three different simulations, with different starting points and different model equations (healthy and faulty). Since the results are the same is with method 1, method 2 is not further considered.

When now extending the fault clearing time by 50 ms to a total of 150 ms, the results are not showing stable behaviour anymore.

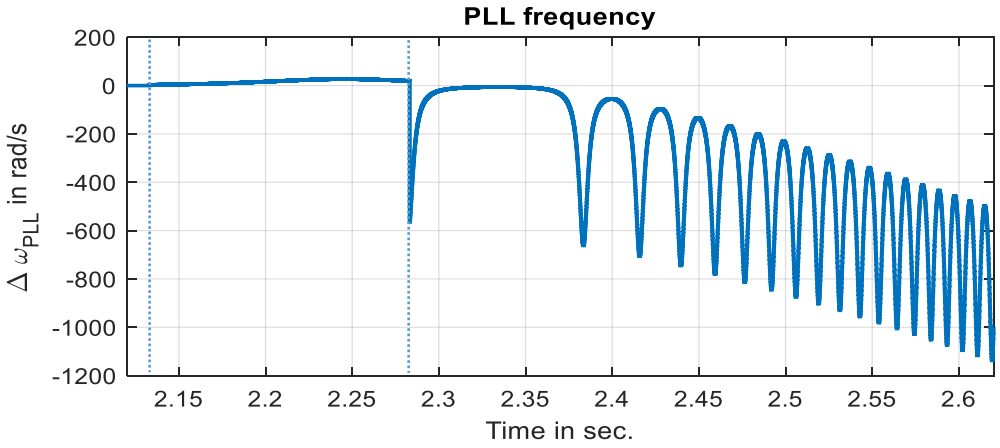

Fig. 78 PLL frequency during unstable situation (method 1)

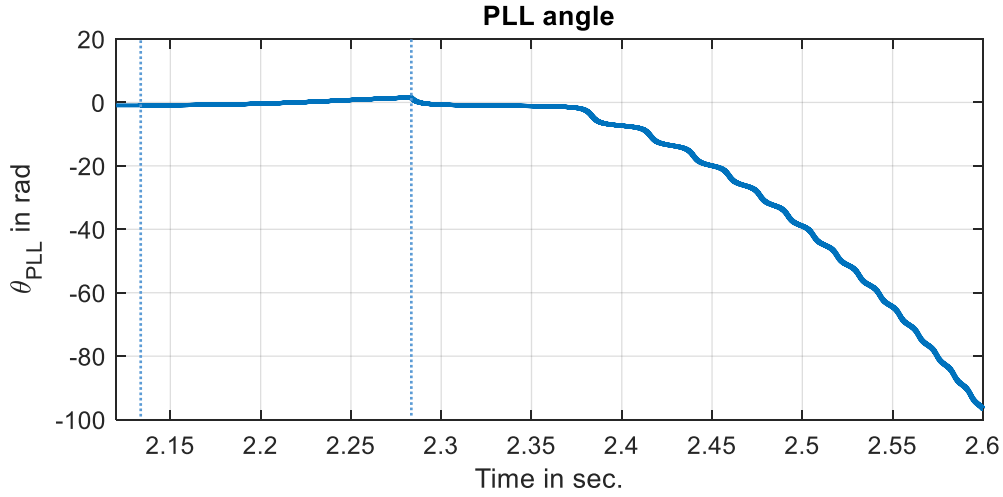

Fig. 79 PLL angle during unstable situation (method 1)

As it can be seen in the DOA plot, in the case of the increased fault clearing time, the jump at the fault end, ends slightly in the blue-unstable DOA-region. The trajectory does not reach the starting point anymore afterwards.

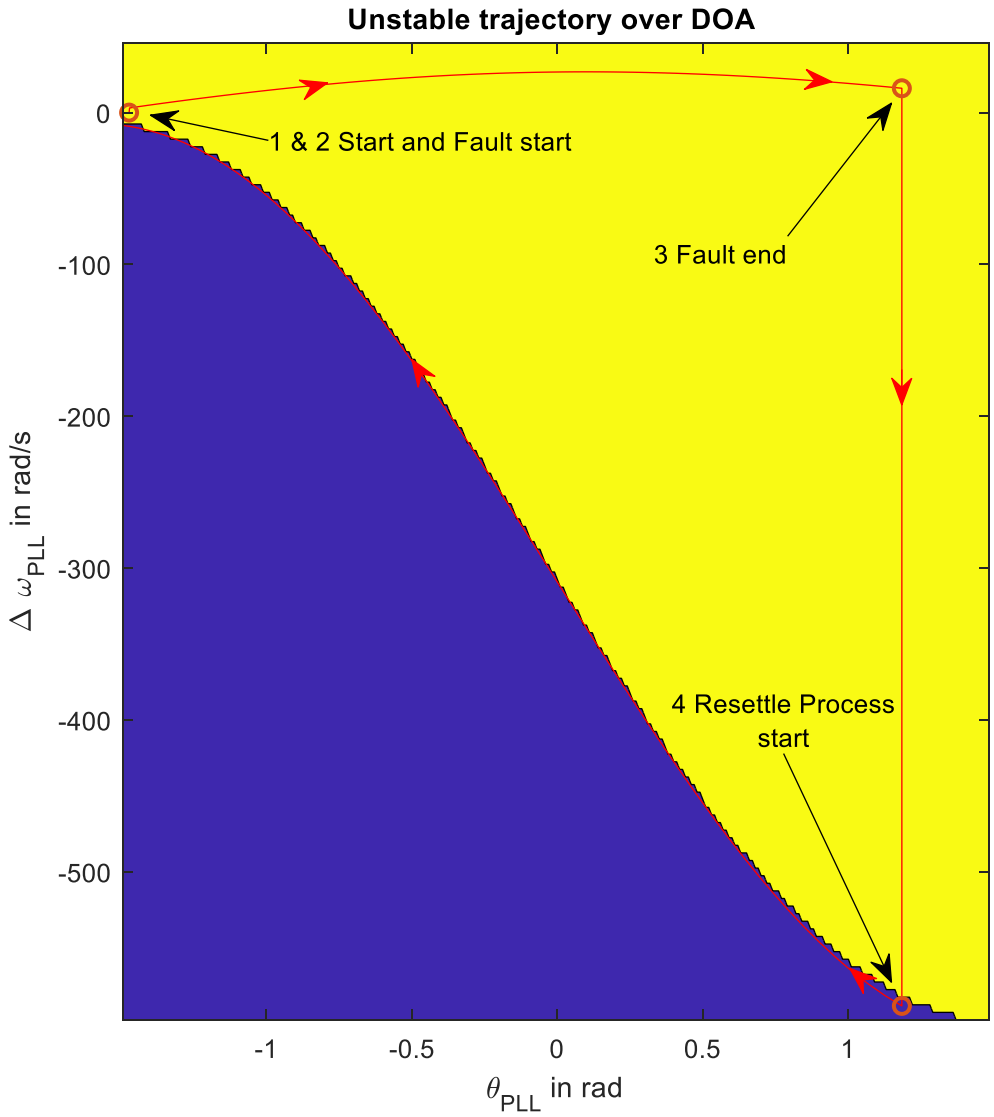

Fig. 80 Trajectory of unstable fault clearance

As it can be seen in this example if a stable situation can be reached after fault clearance strongly depends on the exact clearing time. When the clearing time is rather small or the PLL setting in such a way, that the trajectory moves quite slowly during a fault, a short clearing time is beneficial, since the distance to the original starting point is rather small. But if the trajectory moves fast during a fault and also the PLL-angle changes respectively fast, it cannot be stated securely which fault clearing time is beneficial. In such a case also a new operating point ($n \cdot 2\pi$ “later” or “earlier”) could be reached.

In a next step a simulation should be carried out using the Simulink model for the PLL and also for modelling the electrical network (called *method 3*). Since the network consists of high inductive impedances, current discontinuities stemming from the current source reference calculation lead to overvoltages and can destabilize therefore the PLL easily. That's why filtering the output signals is unavoidable. Since in this chapter, only constant current references (in dq-domain) are used for simplicity, the PLL angle used for the transformation must be filtered, otherwise already the PLL-start-up may diverge. With a 25 Hz-Second Order Butterworth filter, the simulation is carried out.

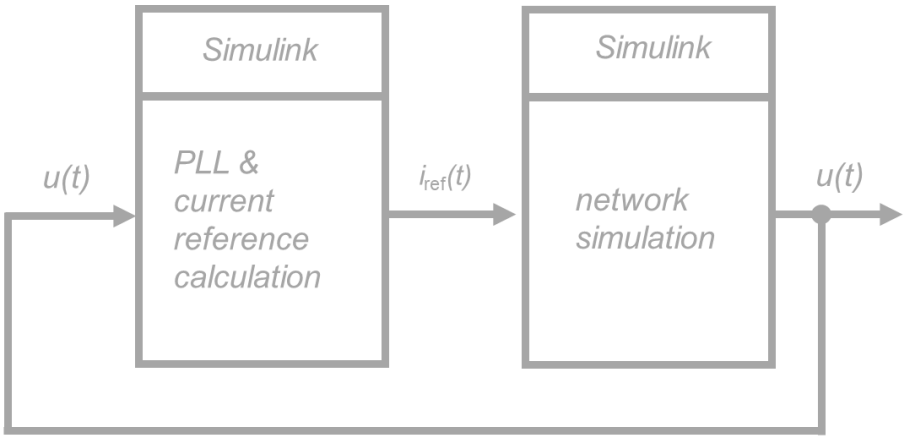

Fig. 81 Method 3

The first simulation with a clearing time of again 100 ms leads to a diverging result, in contrast to the previous used method.

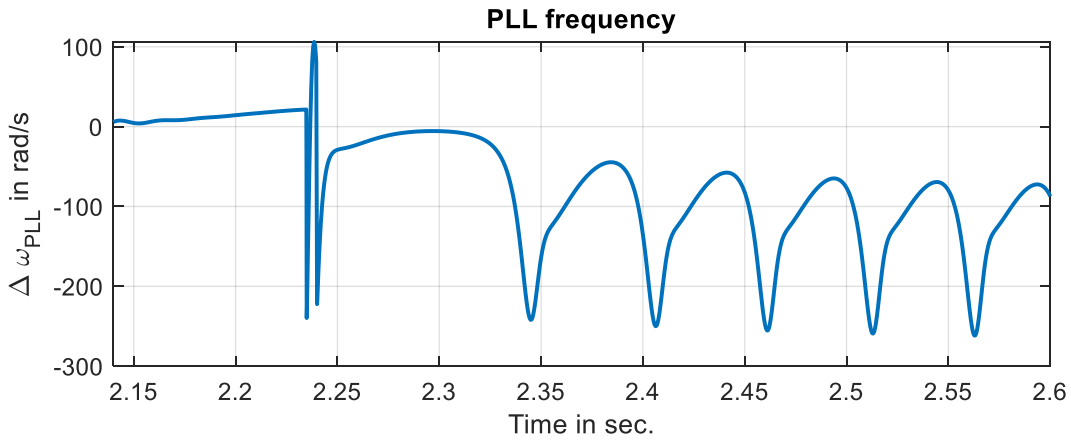

Fig. 82 PLL frequency (100 ms clearing time, method 3)

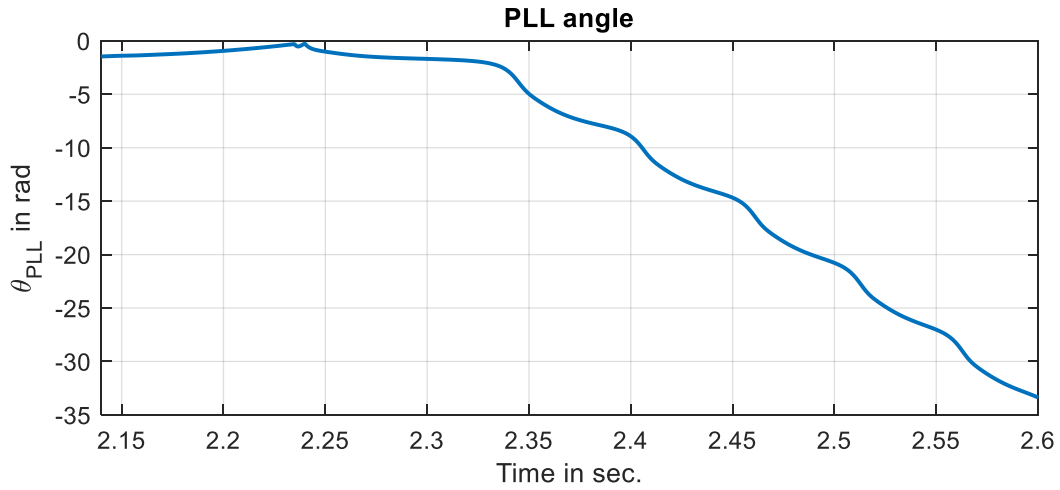

Fig. 83 PLL angle (100 ms clearing time, method 3)

As it can be seen in the plots in the case of *method 3*, the fault clearing modelled in transient domain causes a rather strong transient response, which leads to an oscillation in computed PLL-frequency, which is directly the output of the PLL-PI-controller and therefore directly influenced by changes in terminal voltage. It can also be observed, that the PLL-angle is increasing slower, then compared to the previous unstable simulation result. It is assumed, that the reason for this is the additional low-pass filter in the angle-path.

Plotting the trajectory over the DOA, leads to:

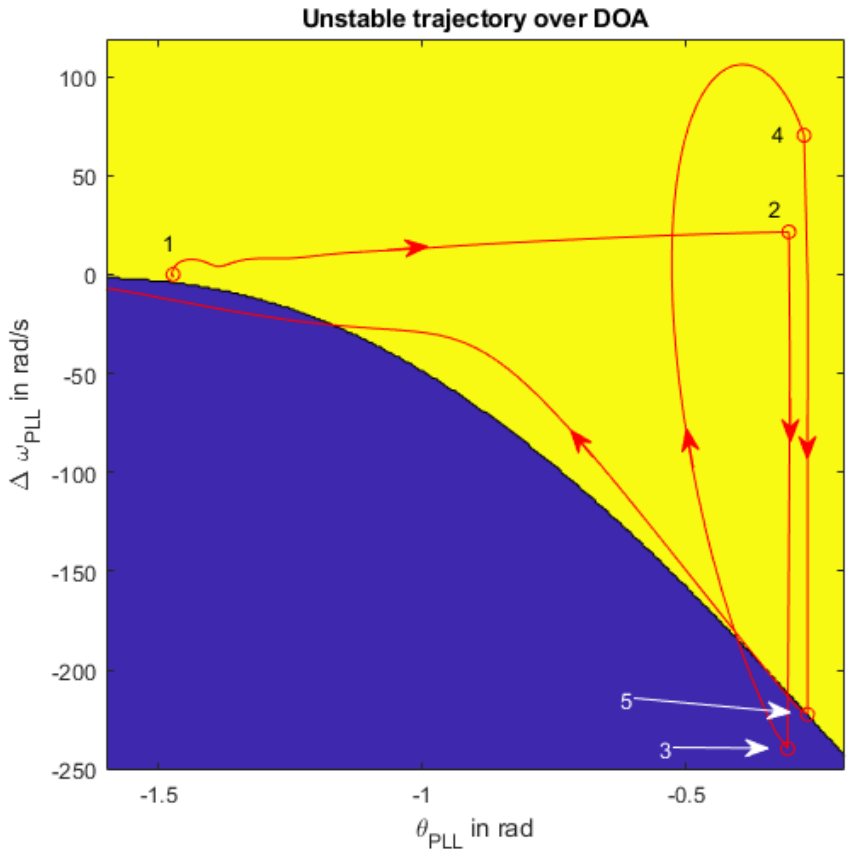

Fig. 84 DOA for 100 ms clearing time

Compared to the previous shown trajectories, in the case of the method with time-domain network solution, the trajectory is more complex and has some remarkable points. At point *1*, the fault is initialised. Before, the frequency $\Delta\omega$ is zero and the angle Θ constant, as obvious for a stable steady state situation. After *1*, due to the static instability of the fault, the trajectory moves towards *2*, while increasing frequency and angle. At point *2*, the fault on phase L3 is cleared, which leads to an abrupt change in voltage, which causes a frequency jump from *2* to *3*. Between *3* to *4* the system represents a two-phase fault between L1 and L2. At *4* the faults on the two faulty phases are also cleared, which again leads to a frequency jump to *5*. From *5*, the trajectory should move towards the starting point, but since *5* is already in the blue/diverging region, the trajectory doesn't reach the starting point anymore.

With a reduction of clearing time, to 50 ms, the situation can again be brought to a beneficial result.

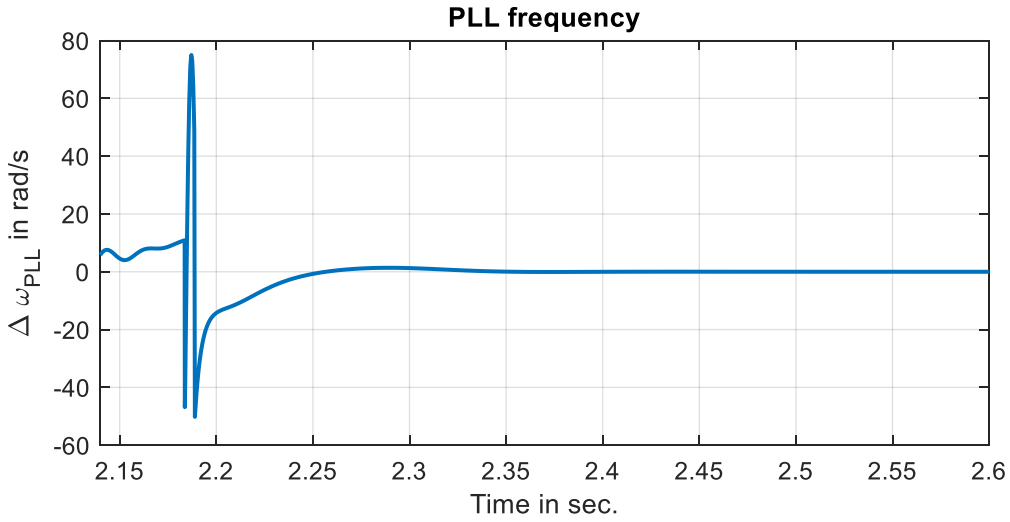

Fig. 86 PLL frequency (50 ms clearing time, method 3)

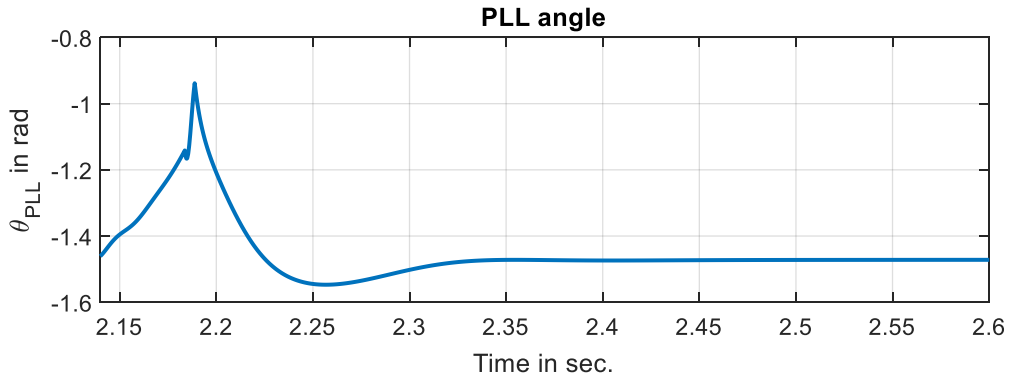

Fig. 85 PLL angle (50 ms clearing time, method 3)

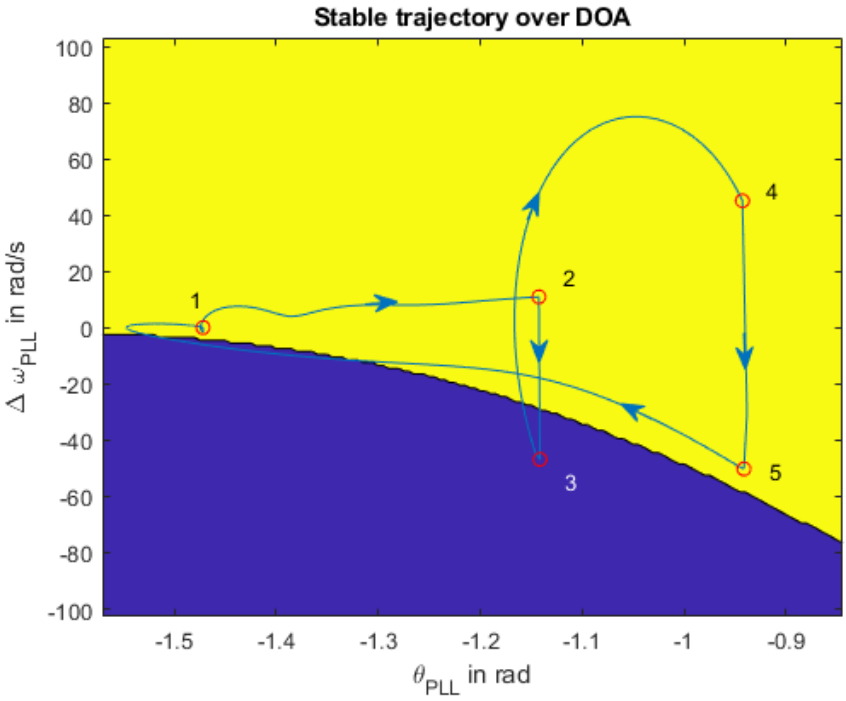

Fig. 87 DOA for 50 ms clearing time

Also, in the case of the reduced fault clearing time, the position on the DOA of point *5*, matches with the final result obtained from simulation. For the five points the previously explained description is valid.

Finally, it can be stated, that the reduced order system describes the full model accurately enough, to predict the convergent behaviour, when knowing the starting point of the transient resettling process, after the fault is cleared completely. This can be used advantageously, to find a critical fault clearing time for a specific situation.

Since the reduced order model does not consider single pole breaking and electromagnetic transients due to charging/discharging processes, this method cannot be used to describe the whole trajectory during a fault transition.

With this reduced order method, it can be easily shown, that stable PLL operating points arise periodically, in contrast to synchronous machine operating points.

In addition, the main impacts on transient PLL stability can be listed:

- PLL settings (PI-controller)
- transient fault condition (overvoltage, electromagnetic response)
- static fault properties (fault impedance, fault type, short circuit level)
- fault clearing time and breaker properties (current chopping, etc.)
- additional control blocks (e.g. sequence decoupling)
- filter elements (in signal processing and hardware)

Due to the high number of variables and challenges in predicting them, transient PLL stability analysis remains a very complex task, which may not be solved accurately enough without detailed simulations and experiments.

5 Validation of simulation example

In a final, realistic example various setting will be changed in a realistic range and previously explained phenomena observed. The likelihood of transient PLL-instabilities under realistic conditions will be investigated in an empirical way.

The model will demonstrate a 100 MW-Windpark, connected to the HV-grid. The model consists of one 100 MW-inverter (machine transformer not modelled) and a 120 MVA park transformer. The park is connected via a double overhead line to the resonant grounded 110 kV-grid. To set the correct arc-suppression coil inductance, the earth capacitance of the to be protected grid is known. To get more realistic values, the capacitance value is increased, through an additional unloaded line, which emulates the rest of the grid.

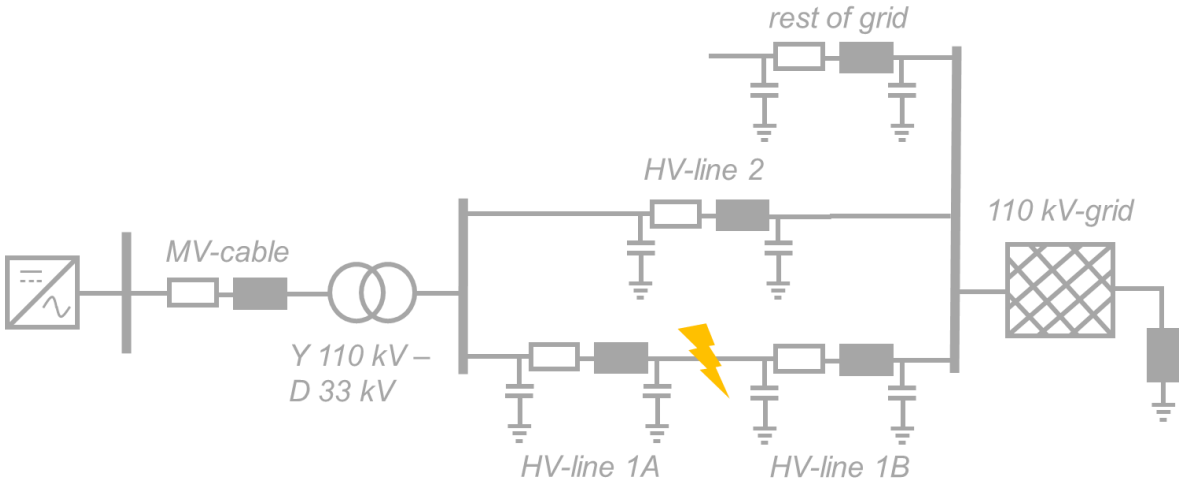

Fig. 88 Used grid model

To check an appropriate setting of the arc-suppression inductance, a single line fault between 1.0 and 1.5 seconds is simulated with inactive inverter and the results compared to a single line fault, but with isolated neutral point.

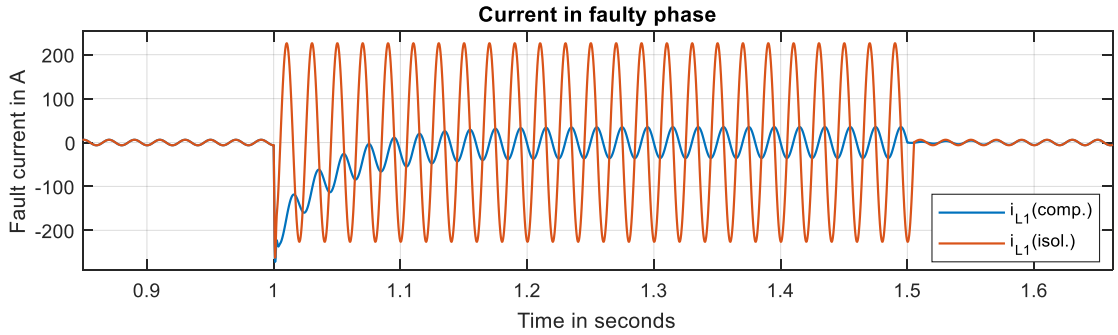

Fig. 89 Fault current for different neutral point treatment methods

As it can be seen, the fault current with arc-suppression coil in neutral point path, leads to a way lower fault current. The transient behaviour at fault start comes from the capacitance and inductance of the line elements and the arc-suppression coil itself. The current values of the two remaining healthy phases

do not differ between isolated or compensated neutral point, with both methods they rise with factor $\sqrt{3}$ in steady state.

The default model settings for this chapter should be listed in the following table. Further variations are then mentioned later.

Table 10 Model data

HV-grid connection		
U_n	110 (slightly unsymmetric)	kV
S_{grid}	4	GVA
$\|Z_{grid}\|$	3.025	Ω
KXR	7	-
X_{grid}	2.995	Ω
R_{grid}	0.428	Ω
MV-cable		
length	7	km
$r_1' + jx_1'$	0.020+ j0.061	Ω/km
c_e'	120	nF/km
HV-lines		
length	5 (HV 1A & 1B); 10 (HV 2)	km
$r_1' + jx_1'$	0.076 + j0.228	Ω/km
c_e'	22	nF/km
g_e'	220	nS/km
Transformer		
S_{rated}	120	MVA
Vector group	Yd1	-
U_{prim}	110	kV
U_{sec}	33	kV
u_{sc}	15	%
$u_{sc,real}$	0.3	%
Inverter		
P_{rated}	100	MW
U_{rated}	33	kV
$f_{1,c}$ (PLL-PI setting positive sequence)	10	Hz
$f_{2,c}$ (PLL-PI setting negative sequence)	30	Hz
$\underline{S}_{ref}$ (Pre-fault Reference power)	1 + j0.1	p.u.
Reactive current injection ratio *k*	2	-
Fault impedance (per phase)		
$R_f + jX_f$	1 + j0	Ω

As a first test, a single line-to-ground should be simulated with activated inverter. In this occasion it is interesting to mention that the *point of common coupling* (*PCC*) in this example should be at the HV-terminal of the transformer. This measured voltage is used to determine the reference current dependent on the reference power. But since the inverter's current source injects on the 33 kV-side, a transformation from the HV reference current to the 33 kV-current is necessary. Since the shunt leg impedance of the transformer is neglected and the modelling is done in per-unit values, this transformation gets very simple and only the phase rotation due to the transformer vector group must be considered.

$$i_{1\mathrm{d,33\,kV}} + \mathrm{j} \cdot i_{1\mathrm{q,33\,kV}} = \left(i_{1\mathrm{d,110\,kV}} + \mathrm{j} \cdot i_{1\mathrm{q,110\,kV}}\right) \cdot e^{\mathrm{j}(-\pi/6)} \tag{124}$$

$$i_{2\mathrm{d,33\,kV}} + \mathrm{j} \cdot i_{2\mathrm{q,33\,kV}} = \left(i_{2\mathrm{d,110\,kV}} + \mathrm{j} \cdot i_{2\mathrm{q,110\,kV}}\right) \cdot e^{\mathrm{j}(+\pi/6)} \tag{125}$$

Due to the high zero sequence impedance, during a single-phase fault in a resonant grounded grid, the zero-sequence voltage is the clearest indicator for a single-phase fault. In positive and negative sequence, the voltages do only change minimally due to the limited fault current and low sequence impedances. Since the used model only contains PLL and control for positive and negative sequence, the reference current may not really change in the occasion of a single-phase fault in resonant grounded grid. In addition, also the FRT mode and thus additional reactive reference current request may not be triggered, since the change of zero sequence is not visible in the line-to-line voltage used for fault detection in this model.

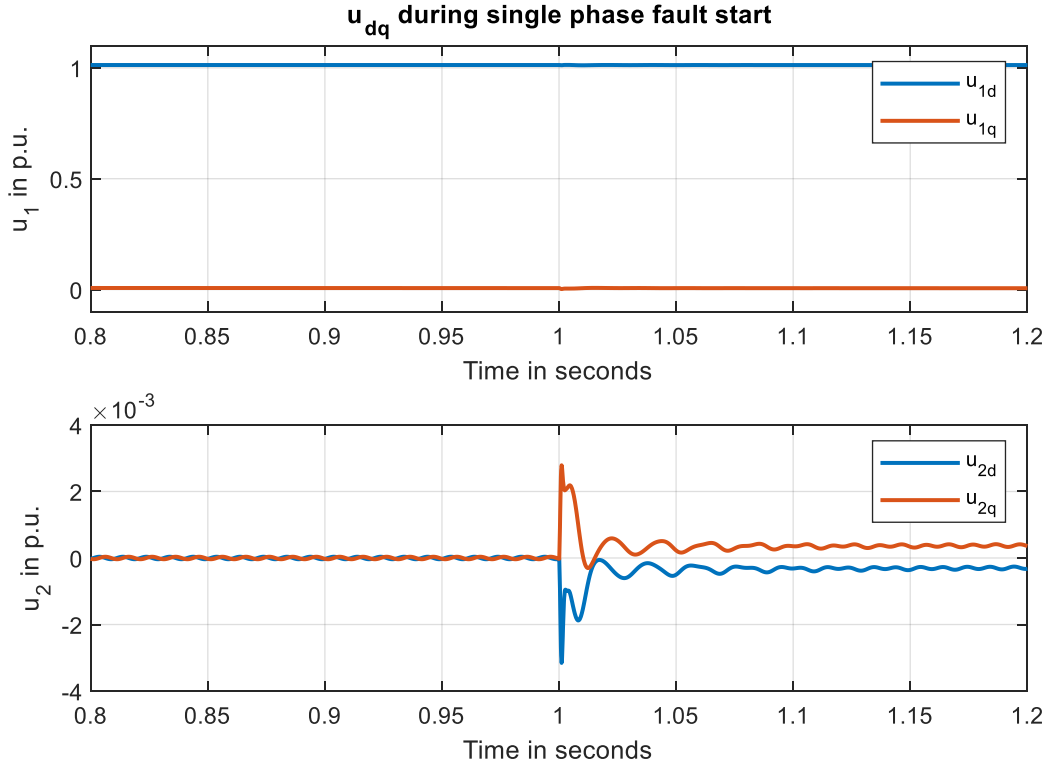

Fig. 90 u_{dq} during single phase fault

This also means, that there is practically no chance of PLL-instability during or after a fault in such condition.

Therefore, in this chapter only the following fault types are considered:

- Three-phase fault (L1-L2-L3)
- Two-phase fault (L1-L2)
- Two-phase fault with earth connection (L1-L2-GND)

To analyse the impact of settings such as fault impedance, PLL settings and so on, fault tests are carried out and the short circuit level of the 110 kV-connection stepwise reduced until a clear PLL instability is observed. The fault remains active for 0.5 seconds, if not otherwise stated and is cleared by disconnecting HV lines 1A and 1B from the rest of the model. Of interest are conditions, which offer a stable pre-fault situation, but do not reach steady state after 1 second after fault end. To facilitate negative sequence PLL operation, a small realistic voltage asymmetry (U_{L2} = 1.02 p.u.) is set at the infeed.

This results in a slight negative sequence voltage during healthy grid situation:

$$\underline{U}_2 = \frac{1}{3} \cdot \left(\underline{U}_{L1} + e^{-j 2\pi/3} \cdot \underline{U}_{L2} + e^{j 2\pi/3} \cdot \underline{U}_{L3} \right) \tag{126}$$

$$|U_2| = \frac{1}{3} \cdot \left| 1 + 1.02 \cdot e^{-j 4\pi/3} + 1 \cdot e^{j 4\pi/3} \right| = 0.0067\ p.u. \tag{127}$$

As a first test, the fault impedance of 1 Ohm is used and for all interesting fault types the critical short circuit level searched, by reducing it stepwise in 25 MVA-steps. This leads to the following results shown in Table 11 (green fields indicate stable behaviour, orange/red fields indicate unstable behaviour):

Table 11: Default setting

Default settings													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

When remembering that the original short circuit level was set to 4 GVA, it is clear that the instabilities shown in this chapter are related to extraordinary, weak grid situations, that can stem for example from feeding line tripping due to faults or power plant failures.

As it can be seen in this first variation, the unsymmetric situation apparently tends easier to instability, than the symmetrical fault condition.

The symmetrical fault at 325 MVA short circuit level should be investigated in more detail.

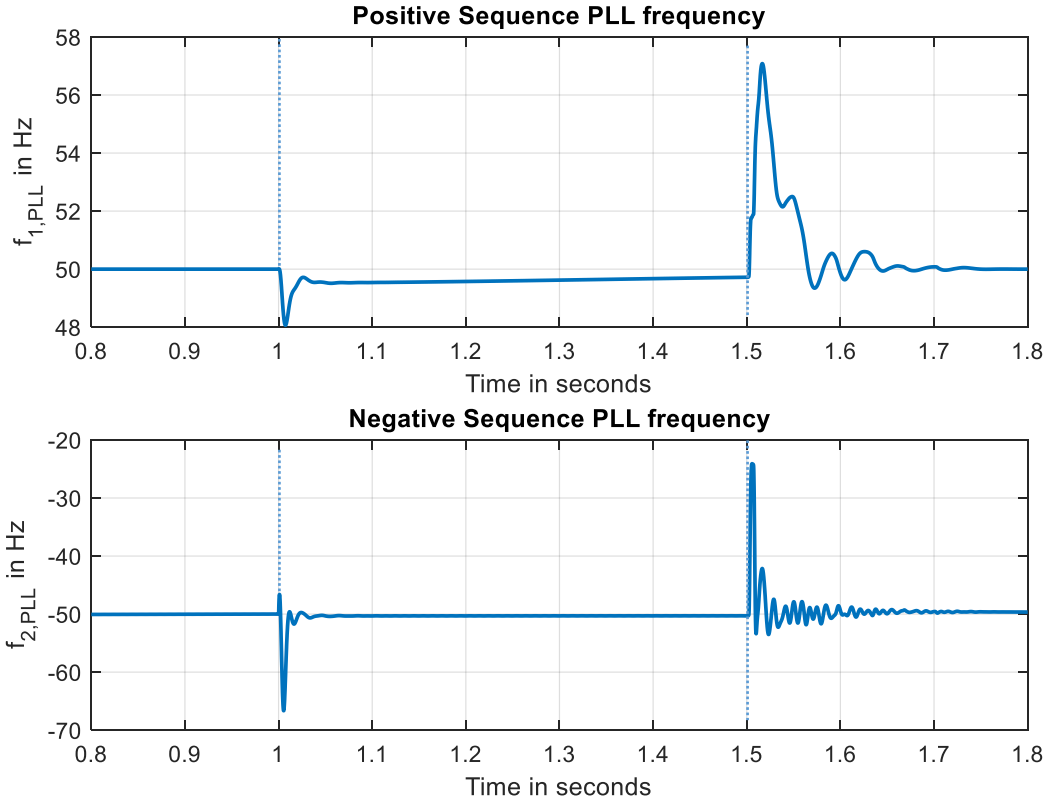

Fig. 91 PLL frequency for three-phase default case

Even though, during the symmetrical fault, no negative sequence should be affected, it can be seen, how the fault start and end (1.0 and 1.5 seconds) causes an oscillation not only in the positive sequence PLL frequency but also in the negative sequence one. The reason for this is the asymmetrical transient voltage behaviour stemming from electromagnetic phenomena, as well as the non-ideal behaviour of the sequence decomposition block. For example, when feeding the SOGI-based block with a symmetrical voltage set and switching ideally to another symmetrical set, the following negative sequence output can be observed.

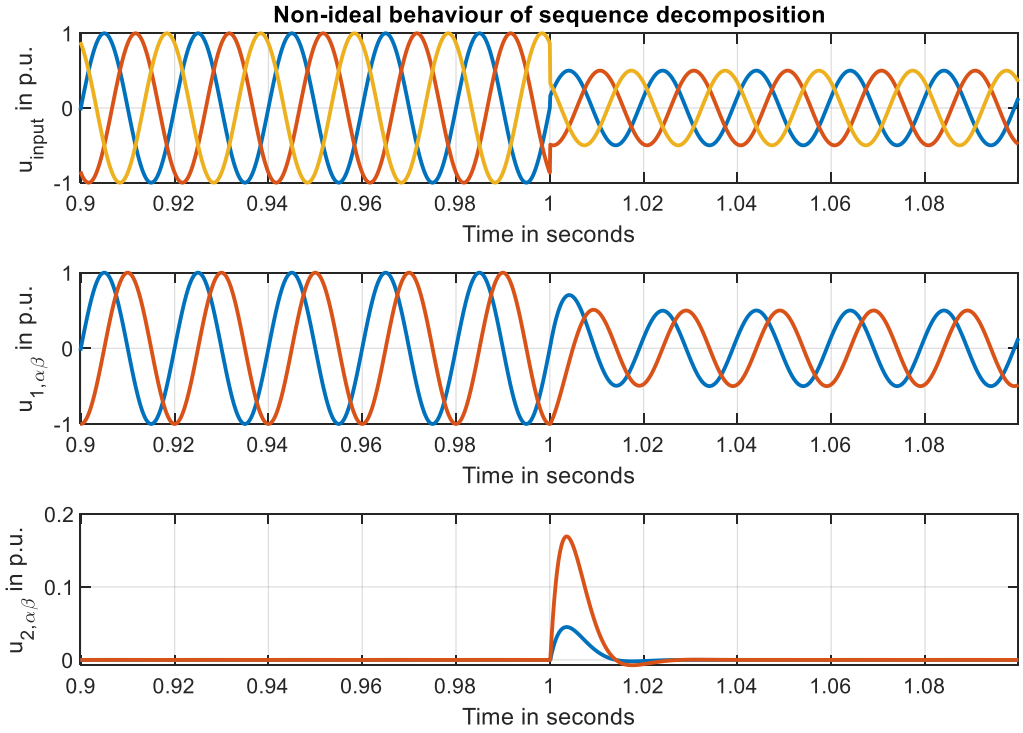

Fig. 92 Non-ideal SOGI-behaviour

Due to this non-ideal sequence decomposition, also during symmetrical transitions, negative sequence PLL is affected. In this first case the oscillation of negative sequence is even more significant than the positive sequence. Also, the frequency of the oscillation seems to be quite higher in negative sequence. This comes from the more dynamic PLL setting applied to negative sequence (30 Hz compared to 10 Hz). All in all, both PLL's manage to track the ideal frequency after fault start and also after fault end. Although, in positive sequence, during the fault, the frequency deviates more obvious from the ideal frequency and does not reach its ideal value until the fault end.

In case of the L1-L2 fault with 325 MVA short circuit level, the PLL frequencies look like the following:

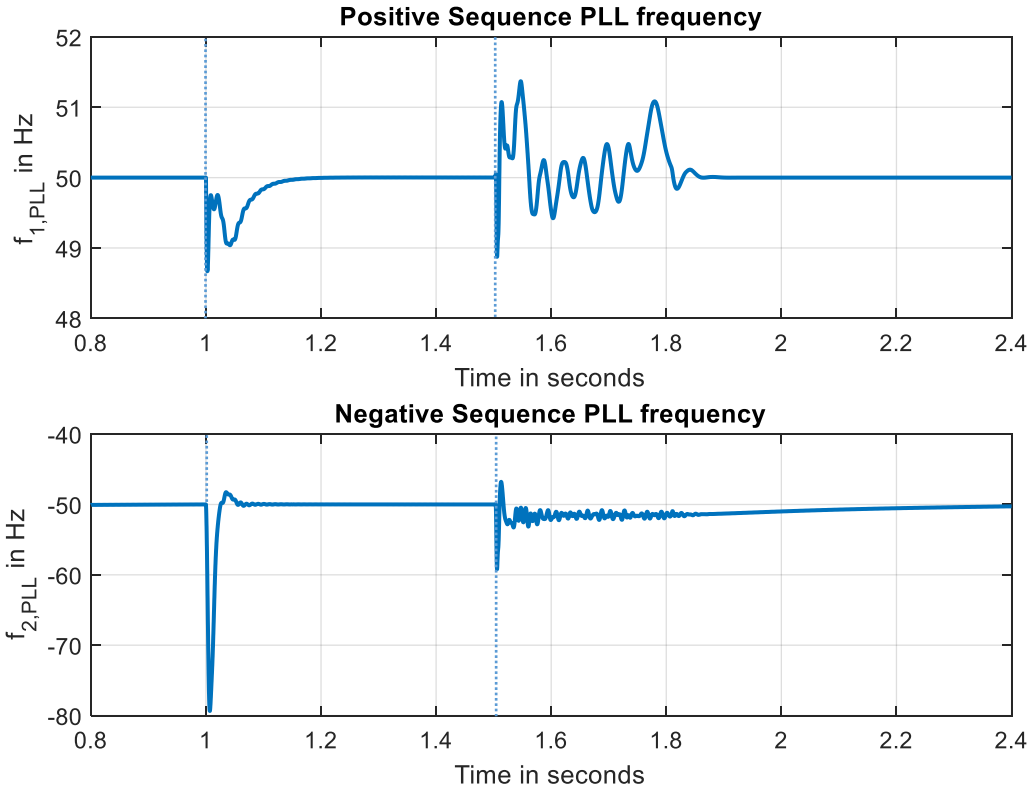

Fig. 93 PLL frequencies during two-phase fault

Also in this case, both PLL's eventually lock on the ideal phase and reach the ideal frequency. But it is also clearly visible, that both frequencies oscillate at fault end much longer than in the symmetrical case. Apparently the positive PLL works better with symmetrical faults, which should be justified. When simulating the same problem, but with disabled negative sequence current injection, it gets clear, that the negative sequence PLL behaviour influences the positive sequence PLL negatively and causes the problem, by affecting the terminal voltage badly.

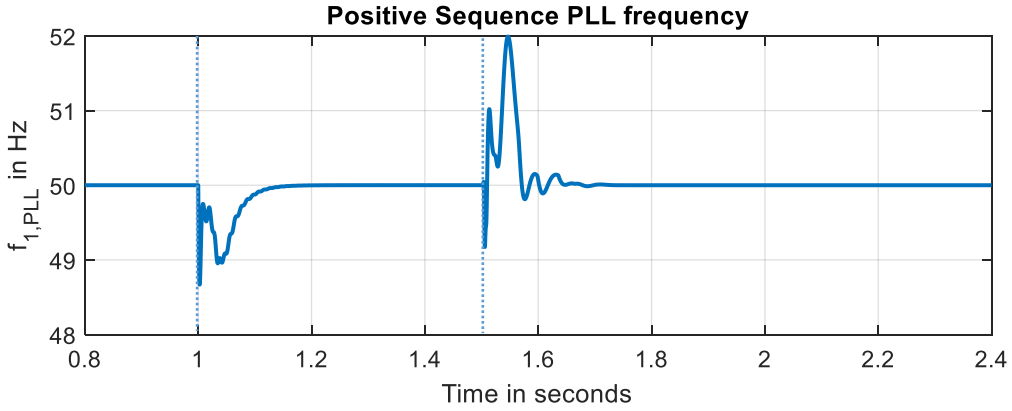

Fig. 94 Positive sequence PLL during two-phase fault, with disabled I_2

In Fig. 93 it can also be seen, that the negative sequence PLL takes more time to reach the rated frequency, as the positive sequence PLL. It seems, that the negative sequence frequency is already

close to the ideal one but does not reach it exactly. This can be explained when remembering the very small unbalance during healthy grid situation. The small negative sequence voltage also means, that the computed q-component is small, even with an angle far off the ideal one, which means that the frequency only changes slowly. It can be shown, that by increasing the voltage asymmetry, the negative sequence PLL and subsequently the influenced positive sequence PLL show less problems in tracking the phase.

By also varying the amplitudes of phase L1 and L3 of the 110 kV infeed, the following negative sequence voltage can be reached.

$$|U_2| = \frac{1}{3} \cdot \left| 0.98 + 1.02 \cdot e^{-\mathrm{j}4\pi/3} + 0.99 \cdot e^{\mathrm{j}4\pi/3} \right| = 0.012\ p.u. \tag{128}$$

With this nearly doubled unbalance, the results of the variation test are improved:

Table 12: Variation test with higher voltage asymmetry

Default settings, higher infeed voltage asymmetry													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

The dark filled field show the difference compared to the default case results.

Comparing the negative sequence PLL frequencies in Fig. 91 and Fig. 93, it is obvious, that in the unsymmetrical case, it takes longer time to reach the rated frequency after fault clearing. This can be explained, when observing the negative sequence PLL angles (integral of PI-controller output without rated frequency) during both cases.

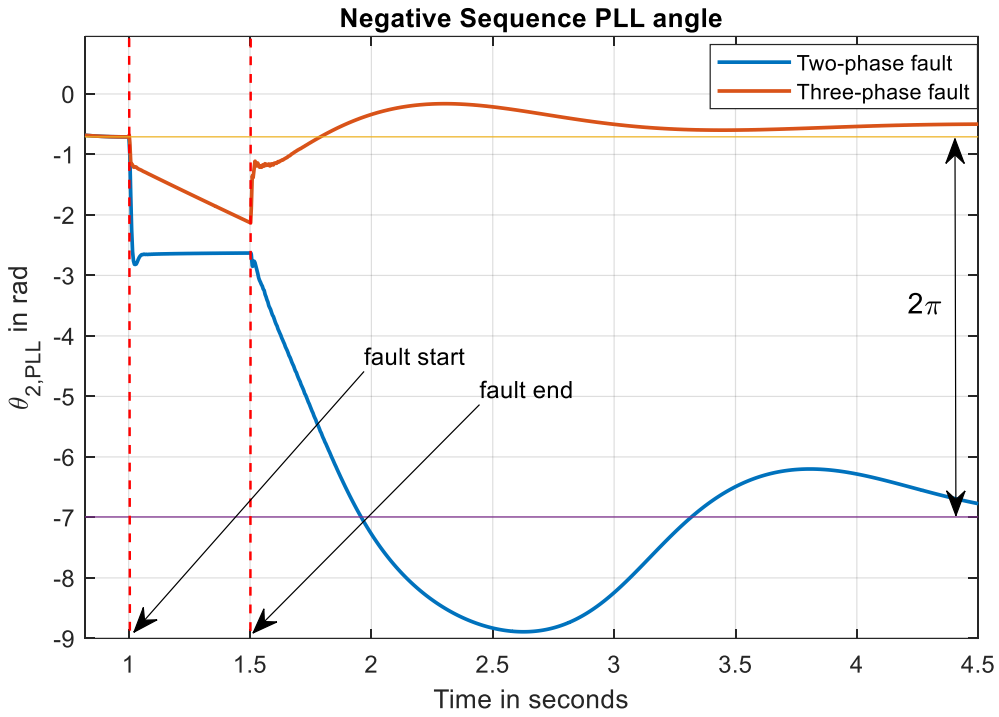

Fig. 95 Negative sequence PLL angle during two different fault types

Due to the different voltage phase jump in the unsymmetrical fault, also the angle jump at fault start looks different. In this case after fault end, in the symmetrical fault case, the original operating point is reached again, while in the unsymmetrical case, another operating point (2π away) is followed, which causes the PLL to take longer time to reach rated frequency. Since this behaviour strongly depends on the exact fault start and clearing time, as well as characteristics such as PLL control settings, no general statement can be made.

Fault timing in general has a huge impact on the transient PLL behaviour. For example, by reducing the fault duration by only 5 ms, the results change considerably. Depending on whether at fault clearing the PLL-trajectory lies in a converging region of the DOA or outside of it, as explained earlier, the transient stability is affected.

Table 13: Decreased fault duration

Default settings, fault duration decreased by 5 ms													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

In a next test series, the fault resistance is increased to 100 Ω. For a typical grid fault such an impedance is rather high, although this situation makes sense since it could illustrate the behaviour during the start-up of a significant ohmic load.

Table 14: Increased fault resistance

Default settings, R_f = 100 Ω													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

The result show a more stable behaviour, where the instability always stems from the negative sequence PLL.

During the 100 Ω fault the inverter's terminal voltage during the fault is only slightly changed, which results also in a weak phase jump. For the three-phase 325 MVA setting the 100 Ω variant even offers a stable operating point during the fault, while the negative sequence phase angle in the 1 Ω variant keeps changing, when simulated with an extended fault time.

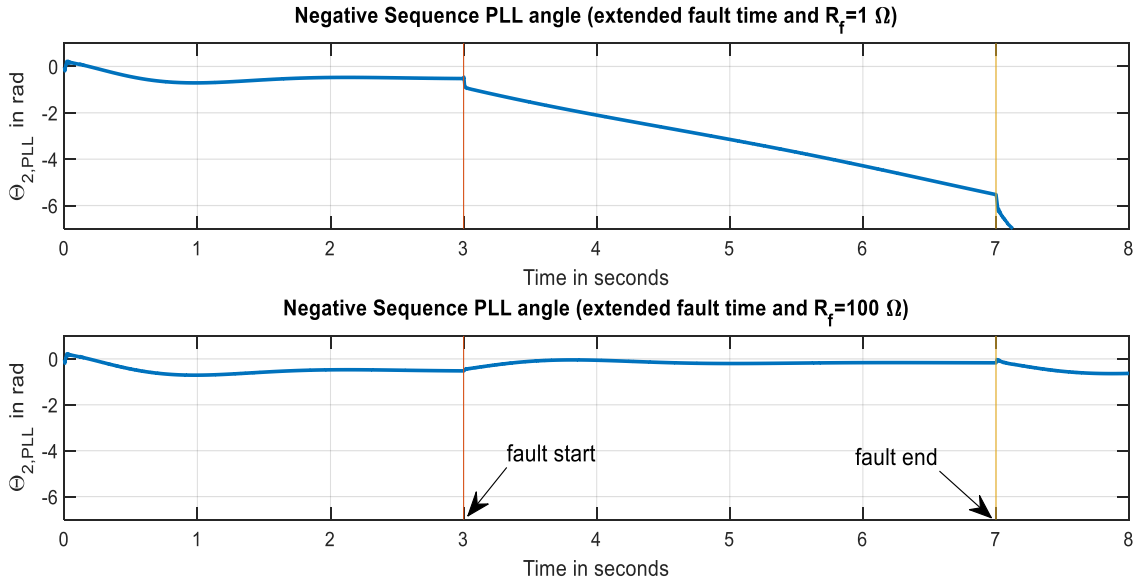

Fig. 96 Negative sequence PLL angle during three-phase fault (extended fault time)

Dependent on the fault clearing time, the phase jump back to the healthy voltage can therefore be rather pronounced with the 1 Ω settings, which increases the risk for transient instability at fault clearing.

Also, by changing the negative sequence PLL settings, no better results can be achieved.
By reducing the fault resistance to a solid-fault like value of 1 mΩ, the same results as with default 1 Ω-settings are achieved.

Table 15: Decreased fault resistance

Default settings, R_f = 1 mΩ													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

As a next variation, the PLL setting is changed. In a first variation series, the PLL setting for positive and negative sequence is set to a more dynamic level (30 Hz for positive sequence and 50 Hz for negative sequence). The results show that with this change the probability of transient instability is increased.

Table 16: Settings for faster PLL

Default settings, $f_{1,c}$ = 30 Hz and $f_{2,c}$ = 50 Hz													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

It can be observed, how the changed PLL settings influence the transient behaviour massively. For this purpose, a plot comparing the results of the three-phase fault with S_{SC} = 250 MVA, once with the stable default PLL setting, and once with the more dynamic setting, should be shown.

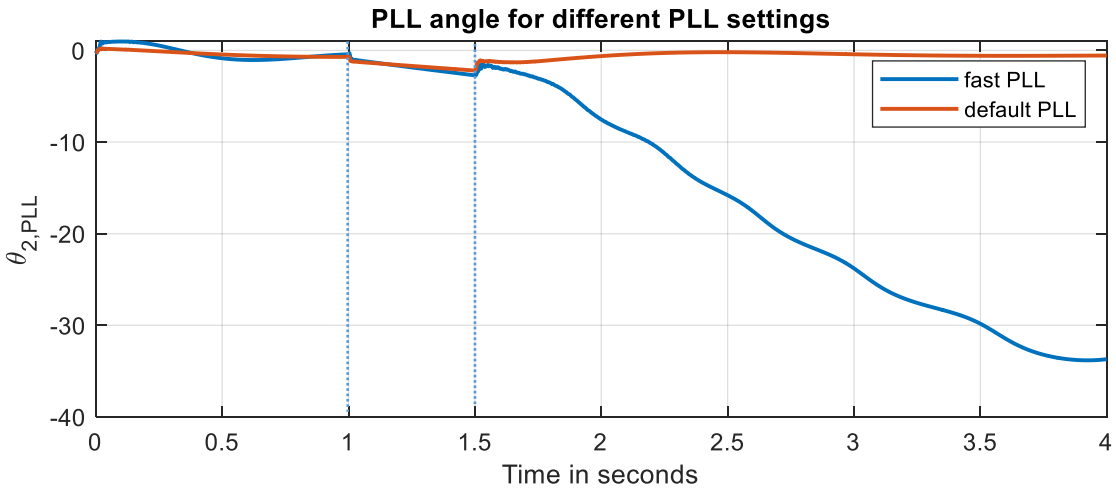

Fig. 97 PLL angle for two different PLL settings

As a last variation, the *k*-factor (additional reactive current injection) is set to zero so that also during fault situations the same current reference method is used as during healthy situations.

Table 17: Disabled additional reactive current

Default settings, k = 0													
S_{SC} in MVA / Fault type	450	425	400	375	350	325	300	275	250	225	200	175	150
L1-L2-L3													
L1-L2													
L1-L2-GND													

As it can be seen in the table above all tested situations lead to stable satisfying results. The first instability occurs at a S_{SC} of 100 MVA, which equals the connected inverters rated power. Apparently, the disabling of the additional reactive current is beneficial concerning transient stability. As already explained in 4.2.2, mainly the relevant impedances define, which current injection angle is beneficial or not, although in this case two further possible reasons can be named.

The first one is, when *k* equals zero, negative sequence current is never injected, which avoids terminal voltage distortions stemming from the negative sequence PLL as shown in previous results. The second reason is, the voltage phase jump, may be smaller, when during the fault, the current must not change its phase angle to much. This facilitates stable transient PLL behaviour.

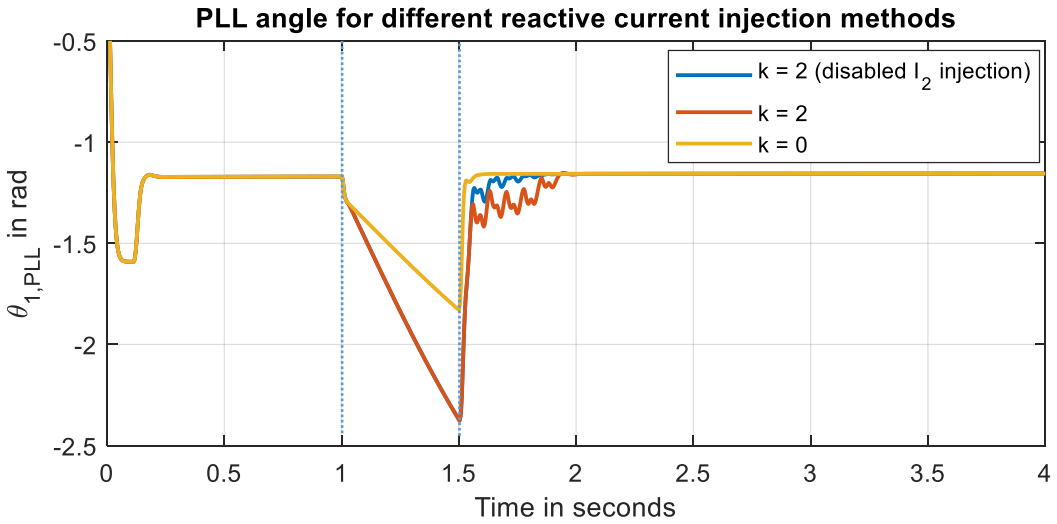

Fig. 98 Different reactive current injection methods (three-phase fault, S_{SC} = 200 MVA)

As it can be seen, in this case, the active additional reactive current, causes the PLL angle to decrease faster during fault, which causes a bigger needed phase jump at fault end, which is stressing the PLL respectively more. The blue graph shows the setting with disabled negative sequence current injection. In that case, the fault clearing happens slightly faster, due to reduced stress caused by the negative sequence PLL.

In the previous explained simulations, it was shown, how different parameters influence the transient stability of the inverters PLL. Weak grid situations and respectively low short circuit levels, have the biggest influence on the PLL stability. The weaker the grid is, the stronger the voltage changes during faults. Also, the inverter influences the terminal voltage more, when the grid is weak, which can end up in destabilizing the PLL itself. For practical applications, simulating the inverter with the relevant grid infrastructure, can point out, which short circuit levels can cause critical situations and which levels are high enough to make PLL instability very unlikely.

The fault impedance influences the voltage during the fault and subsequently the whole transient process. Since the fault impedance cannot be predicted, during the design process different values must be assumed, remembering that lower impedance values are not always leading to higher risks of instability, due to the non-linear behaviour of the PLL.

Since the fault clearing time also influences the transient behaviour, realistic values extractable from relay settings and circuit breaker times should be considered, assuming although a large enough tolerance band.

The PLL setting itself also affects the transient process strongly. In real life a trade-off must be found between stability (lower PLL dynamic) and minimum requests from standard (minimum settling time of additional reactive current). In this regard it is also interesting, which voltage asymmetry can be assumed during healthy grid situations, since that influences the negative sequence control, as shown in this chapter. In addition, it cannot be stated which fault type generally causes more problems for the PLL.

Depending on grid infrastructure (line, cables, etc.) and star point treatment, also electromagnetic phenomena during fault start and end must be considered and should not be ignored in simulations.

All in all, transient PLL stability remains a complex topic, which cannot be solved solely by simulations and theoretic considerations but must be tackled also with real-life measurements or/and Hardware-in-the-Loop (HIL) tests. In addition, due to simplifications and uncertainties in software models, in real life generous safety margins should be considered, to avoid critical boundaries.

6 Conclusion and outlook

In this work it was shown, how a modern grid-following inverter control including PLL, fault detection, reference current calculation and current limiting can be modelled. The general behaviour of the PLL circuit was analysed and explained, with special focus on grid faults. Due to the high variety of parameters in the model, it was difficult to achieve very clear conclusions about dependencies, relations and influences considering PLL-stability.

For the existence of stable operating points, a method [31, 47] was used, with which an estimation about stability is possible, solely knowing the values of the relevant impedances, as well as the injected current. The validation with the simulation model, showed great applicability for rough estimations for symmetrical faults. Although the method also showed strong dependency on accuracy, since already small phase angle changes, especially in the fault impedance, can change the outcome. The simulation results showed a satisfying stable model behaviour, since only extreme weak grid situations lead to severe instabilities.

For dynamic observations, a reduced order model was used to determine the domain of attraction, as well as specific PLL-trajectories for different symmetrical fault situations. The resulted domain of attraction showed periodical stable operating points, as discussed in several publications. Compared to synchronous generators this characteristic is new for power systems. The results were compared with the full simulation model including transient network calculation. The results showed that the shape of the trajectory itself cannot be modelled very accurately by the simplified equations, due to neglected electro-magnetic phenomena. Although it was shown that the achieved information about stability included in the domain of attraction can also be used in combination with trajectories from the full model. Whit that it was shown that also dynamic stability analyses can be carried out rather easily in Matlab or similar solutions, without the use of Simulink and its proprietary toolboxes.

Both, the methods tested for static and dynamic stability in this work are restricted to positive sequence signals and can therefore only applied for symmetrical situations. The extension to unsymmetrical situations is although theoretically possible but would have gone beyond the scope of this work. Although, especially in the final example chapter it was shown, that the negative sequence PLL behaviour would require a closer examination, since due to the low negative-sequence voltage before and after grid-faults, the behaviour differs from the positive-sequence PLL.

As mentioned in the abstract of this work, the final model version should be used in *Omicron*'s system-based protection testing software *RelaySimTest*. In *RelaySimTest* it is possible to simulate a power system consisting of infeeds, lines, cables, transformers, loads, motors, etc. with the scope of determining the voltages and currents a protection relay at a specific location in the power system would process for its operation during healthy or faulty grid situations. The determined signals can be applied to real-life relays using an amplifier kit, which at the same time also works as a measurement kit to receive the relevant relay reactions. With the novel inverter model, it would be possible for the customer to test its protection equipment in the surroundings of inverter-based resources, which is unavoidable

with the rising number of installed inverter units. At the current time, December 2022, a first inverter prototype, on basis of the model explained in this work, is implemented in *RelaySimTest* and will be tested in selected customer projects in near future.

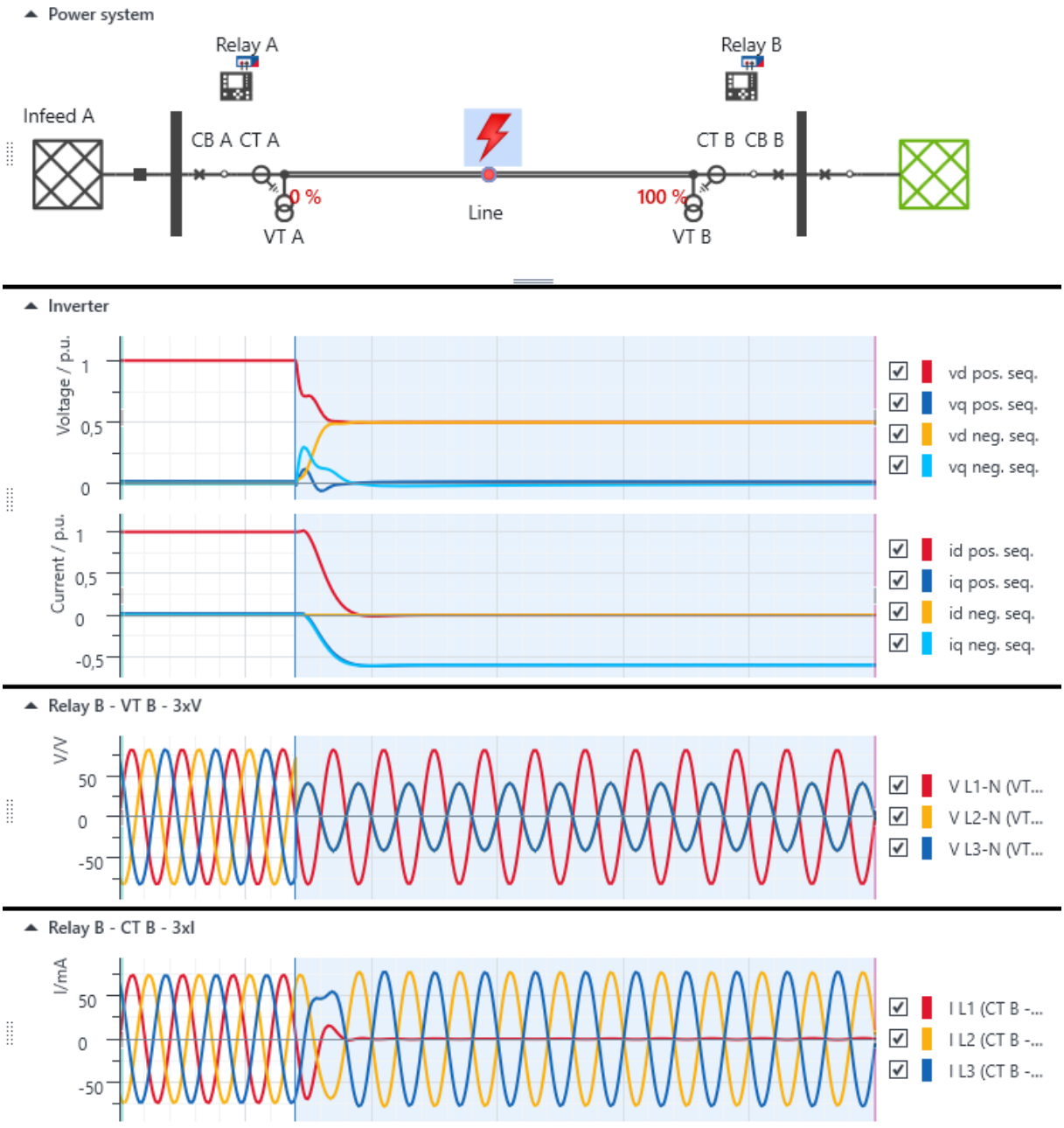

Fig. 99 Screenshot of RelaySimTest inverter prototype

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