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Development of a Protection Concept for the Implementation of Static Synchronous Series Compensators (SSSC) into Transmission Grids

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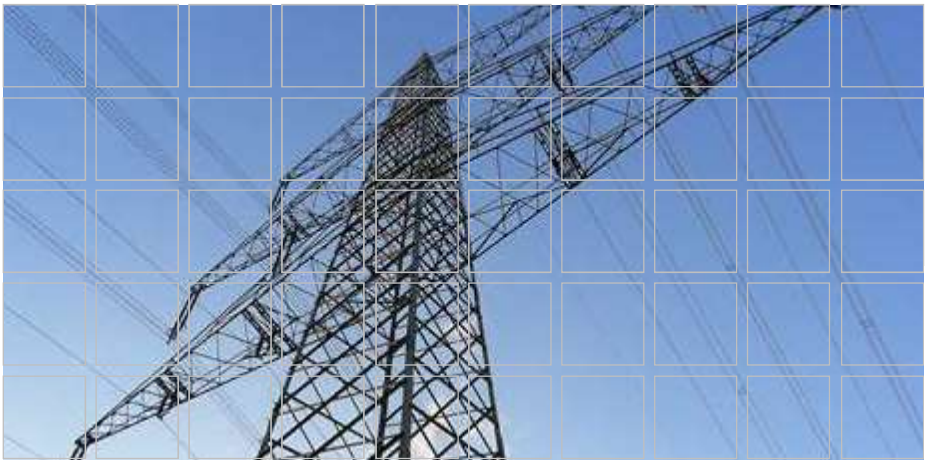

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Abstract

Power system protection is the fundamental basis for the high level of supply security in our electrical energy system. It ensures that faults are cleared, damage to equipment is avoided, and risks to humans and animals are minimized.

The goal of this work is to examine the influence of a Static Synchronous Series Compensator (SSSC) on distance protection, which is frequently used for line protection in high and ultra-high voltage networks. The first step of this investigation consists of a literature review focused on the topics of power system protection, Flexible AC Transmission Systems (FACTS), SSSCs and existing knowledge about the interactions between series compensation systems and distance protection devices.

Subsequently, the influence of SSSCs on distance protection systems is analysed by simplified calculations to allow for initial estimate. Additionally, an analytical examination of the effect of SSSCs on the measured fault loops of distance protection devices is investigated.

A use case scenario is then defined, based on which the effects of SSSCs on the impedance measurement of distance protection devices are further investigated. For this purpose, a model of a SSSC is developed in Matlab / Simulink, which represents the essential functions of the SSSC. The consideration of the automatic bypass function of the SSSC plays a crucial role, as the bypass is responsible for protecting the hardware of the SSSC during a fault event.

The analysis of the use case is based on offline simulations in Matlab/Simulink and on Protection Hardware In the Loop (ProtHIL) tests in a real-time simulation environment with the integration of protection devices used in field. The Hardware In the Loop tests are used to examine the influence of the time delay from fault start to bypass activation to investigate its impact on protection devices.

The findings can be summarised as follows:

- In case of the unlikely event of a bypass failure of the SSSC, there may be a shift of the fault detection into an incorrect zone of the distance protection. This shift can be counteracted by using teleprotection schemes.
- The timing of the bypass activation has a significant impact on the shifting of faults into incorrect zones.
- During terminal short circuits, it may occur that the fault direction is incorrectly detected. This effect can be countered by using memorised voltages.
- The coordination of the pickup of the protection device must be synchronized with the activation of the SSSC bypass. Ideally, the bypass activation should occur before the pickup of the protection device. An additional communication interface between SSSCs and protection devices can ensure this.

Keywords: Power System Protection, Distance Protection, FACTS, SSSC, Protection Hardware In the Loop

Kurzfassung

Schutztechnik bildet die Grundbasis für das hohe Maß an Versorgungssicherheit unseres elektrischen Energiesystems. Sie garantiert, dass Fehler geklärt, Schäden an Betriebsmittel vermieden und die Risiken für Mensch und Tier minimiert werden.

Das Ziel dieser Arbeit besteht darin, den Einfluss eines Static Synchronous Series Compensator (SSSC) auf die häufig eingesetzte Schutzfunktion Distanzschutz zu untersuchen. Der erste Schritt dieser Untersuchungen setzt sich aus einer Literaturrecherche zusammen, die mit den Schwerpunktthemen Schutztechnik, SSSCs und bereits vorhandenen Erkenntnissen zwischen der Wechselwirkung von seriellen Kompensationsanlagen und von Distanzschutzeinrichtungen beschäftigt.

Anschließend wird der Einfluss von SSSCs auf Distanzschutz-Einrichtungen durch vereinfachte Berechnungen analysiert, um erste Abschätzungen zu ermöglichen. Zusätzlich erfolgt die analytische Betrachtung der Auswirkung von SSSCs auf die eingemessenen Fehlerschleifen von Distanzschutzeinrichtungen.

Folgend ist ein Use-case-Szenario definiert, auf dessen Basis die Auswirkungen von SSSCs auf die Impedanzmessung von Distanzschutzgeräten weiter untersucht wird. Hierfür wird ein Modell eines SSSCs in Matlab / Simulink entwickelt, das die maßgeblichen Funktionen des SSSCs abbildet. Die Berücksichtigung der automatischen Bypassfunktion des SSSC spielt dabei eine wesentliche Rolle, da der Bypass für die Überbrückung des SSSCs im Fehlerfall verantwortlich ist.

Die Analysen dieses Szenarios basieren auf Offline-Simulationen in Matlab / Simulink sowie auf Protection Hardware In the Loop Tests in einer Echtzeit-Simulationsumgebung mit der Einbindung von realen Schutzgeräten. Die Hardware In the Loop Tests werden genutzt, um den Einfluss der zeitlichen Verzögerung von Fehlerstart bis zur Aktivierung des Bypasses auf die Beeinflussung des Distanzschutzgerätes zu untersuchen.

Die gewonnen Erkenntnisse lassen sich wie folgt zusammenfassen:

- Im Fall des Bypass-Versagens des SSSCs kann es zu einer Verschiebung der Fehlererkennung in eine falsche Zone des Distanzschutzes kommen. Dieser Verschiebung kann durch die Verwendung von Signalvergleichsverfahren entgegengewirkt werden.
- Der Zeitpunkt der Aktivierung des Bypasses hat einen maßgeblichen Einfluss auf die Verschiebung von Fehlern in falsche Zonen.
- Beim Klemmenkurzschluss kann es auftreten, dass die Richtung des Fehlers falsch erkannt wird. Diesem Effekt kann durch die Nutzung von gespeicherten Spannungen für die Richtungserkennung entgegengewirkt werden.
- Die Koordination der Anregung des Schutzgerätes muss mit der Aktivierung des Bypasses des SSSCs koordiniert sein. Die Aktivierung des Bypasses sollte idealerweise vor der Anregung durch das Schutzgerät erfolgen. Eine zusätzliche Kommunikationsschnittstelle zwischen SSSCs und Schutzgeräten kann dies gewährleisten.

Stichwörter: Schutztechnik, Distanzschutz, FACTS, SSSC, Protection Hardware In the Loop

Symbolverzeichnis

α	Angel correction for quadrilateral impedance characteristics
C	Capacitance
ΔE_{LB}	Upper boundary of energy band
ΔE_{UB}	Lower boundary of energy band
Δu_c	Capacitor voltage ripple
$\Delta u_{c,max}$	Maximum capacitor voltage ripple
φ_{line}	Line characteristic angle
f	Frequency
i	Instantaneous current (generalised)
$\underline{I}$	Current phasor of the fundamental (generalised, complex)
$I>$	Lower current threshold for U / I – and U / I / φ – pickup (distance protection)
$I>>$	Upper current threshold for U / I – and U / I / φ – pickup (distance protection)
$I>>$	High Current Stage I>> Stage (DTO)
$I>_{stage,i}$	Pickup Threshold I> Stage *i* (DTO)
$\underline{i}_\alpha$	α – component of current space vector (generalised)
$\underline{i}_\beta$	β – component of current space vector (generalised)
i_c	Capacitor current
$\underline{I}_d$	d – component of current (generalised)
$\underline{I}_q$	q – component of current (generalised)
I_{pickup}	Pickup Threshold (distance protection)
$I_{rated,max}$	Maximum rated current
$\underline{I}_E$	Earth current (complex, generalised)
$I\varphi>$	Upper pickup threshold for U / I / φ – pickup (distance protection)
$\underline{I}_k$	Phasor of the fundamental of the short-circuit current (complex)
$i_k(t)$	Short-circuit current in the time domain
$I_{k,max}$	Maximum short-circuit current

$I_{k,min}$	Minimum short-circuit current
I_{load}	Load current
I_{HV}	High-voltage side current of the current transformer
I_{rated}	Rated current
$\underline{i}_s$	Current space vector (complex)
I_{SC}	Instantaneous current threshold
$\underline{I}_{SSSC}$	Rated current of SSSC
$\underline{I}_{R,L1}$	Current phase L1 at Relay R (complex)
I_{LV}	Low-voltage side current of the current transformer
$K_{I,PLL}$	Integral parameter of PLL
$k_{P,PLL}$	Proportional parameter of PLL
θ	Reference angle of space vector (generialised)
$\underline{k}_E$	Ground factor (complex)
$\underline{k}_M$	Mutual coupling factor (complex)
k_s	Safety factor (context-related)
L_k	Short-circuit inductance
n	Relative fault distance in %
P	Active power (generalised)
R	Resistance (generalised)
$R1$	Parameter setting resistance Zone 1 (quadrilateral characteristic)
$R1B$	Parameter setting resistance overlap zone (quadrilateral characteristic)
$R2$	Parameter setting resistance Zone 2 (quadrilateral characteristic)
R_f	Fault resistance
R_k	Short-circuit resistance
R_{arc}	Arc resistance
R_f	Fault resistance
S_k''	Transient short-circuit power (generalised)
t_I	Transformer ratio current transformer

$T_{I>stage,i}$	Time delay of stage *i* (DTO)
$T_{inst.}$	Instantaneous trip time (DTO)
t_U	Transformer ratio voltage transformer
U_R	Rated voltage (generalised)
$\underline{U}$	Voltage phasor of the fundamental (generalised, complex)
$U_{1,A}(t)$	Positive sequence voltage at node A (absolute)
$U_{1,Q}(t)$	Mains positive sequence voltage (absolute)
$\underline{U}_{1,Q,A}(t)$	Mains positive sequence voltage at node A (complex)
$\underline{U}_{1,Q,B}(t)$	Mains positive sequence voltage at node B (complex)
u_c	Capacitor voltage
U_{DC}	Ideal DC voltage of the DC link capacitor
$U_{I>}$	Lower voltage threshold for U / I – and U / I / φ – pickup (distance protection)
$U_{I>>}$	Upper voltage threshold for U / I – and U / I / φ – pickup (distance protection)
u_{inj}	Instantaneous injected voltage
$U_{inj,ref}$	Reference RMS of the injected voltage
$\underline{U}_k$	Phasor of the fundamental of the short-circuit voltage (complex)
$u_k(t)$	Short-circuit voltage in the time domain
U_{LB}	Lower boundary of voltage band
U_{HV}	High-voltage of the voltage transformer
U_{rated}	Rated voltage (RMS of the Line-to-Line voltage)
U_{UB}	Upper boundary of voltage band
$\underline{U}_{R,LE}$	Line-to-ground voltage at relay R1 (complex)
U_{LV}	Low-voltage side of the voltage transformer
ω_{ff}	Feed forward angular frequency
X1	Parameter setting reactance Zone 1 (distance protection)
X1B	Parameter setting reactance overlap zone (distance protection)
X2	Parameter setting reactance Zone 1 (distance protection)
X_{SSSC}	Injected reactance of the SSSC

X	Reactance (generalised)
$\underline{Z}$	Impedance (generalised, complex)
$\underline{Z}_0$	Zero sequence impedance (complex)
$\underline{Z}_1$	Positive sequence impedance (complex)
$Z_{1,A}(t)$	Positive sequence impedance at node A (absolute)
$\underline{Z}_{1,line}$	Positive sequence impedance of line (absolute)
$\underline{Z}_{1,Q,A}$	Positive sequence impedance of source A
$\underline{Z}_{1,Q,B}$	Positive sequence impedance of source B
$\underline{Z}_{(2)}$	Negative sequence impedance (complex)
$\underline{Z}_{Line}$	Line impedance (generalised)
$Z_{operation}$	Steady-state impedance during normal operation
Z_{fault}	Steady-state fault impedance
$Z_{fault}(t)$	Fault impedance (absolute)
Zi_{Rk}	Parameter setting of Zone i at protection relay k (1. zone of relay 1: $Z1_{R1}$)
$\underline{Z}_k$	Short-circuit impedance (complex)
$Z_{swing}(t)$	Power swing impedance (absolute)
Z_{prim}	Impedance (primary)
$\underline{Z}_{R,LE}$	Loop impedance line-to-ground at relay R
Z_{LV}	Impedance (secondary-side)

Abbreviations

AC	Alternating Current
AR	Auto Reclosure
BB	Busbar
DC	Direct Current
DTO	Definite Time Overcurrent
FACTS	Flexible Alternating Current Transmission Systems
HPF	High pass filter
ITO	Inverse Time Overcurrent
LPF	Low pass filter
MCM	Measuring-Circuit Monitoring
MMC	Modular Multilevel Converter
MOV	Metal oxide varistor
ProtHIL	Protection Hardware In the Loop
PST	Phase-Shifting transformer
RMS	Root Mean Square
RTS	Real-time simulator
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
SVC	Static Var Compensator
TCSC	Thyristor Controlled Series Compensator
THD	Total harmonic distortion
UPFC	Unified Power Flow Controller
SS	Substation
VSC	Voltage Source Converter

Table of Contents

1 Current Situation and Goal of this Thesis

As modern power systems evolve, integrating flexible AC transmission system (FACTS) devices, such as Static Synchronous Series Compensators (SSSCs), has become increasingly important for enhancing grid stability and flexibility. SSSCs are used to dynamically control power flows, improve system stability, and mitigate issues such as power oscillations. However, while SSSCs offer significant benefits for grid operation, they also enhance complexities, particularly in the behaviour of distance protection relays. The impact of SSSCs on these protection systems can challenge conventional fault detection methods, potentially affecting the accuracy and reliability of fault location, direction detection, and zone shifting.

This thesis aims to investigate the specific influence of SSSCs on distance protection relays. Understanding this interaction is crucial for ensuring that protection systems can operate accurately and reliably in the presence of SSSCs. The findings of this research will be applied to develop a protection concept that addresses these challenges, allowing for the effective integration of SSSCs into transmission grids. By analysing both static and dynamic behaviours, through theoretical analysis, simulation and Hardware In the Loop testing, this thesis seeks to provide comprehensive insights into mitigating protection issues associated with SSSCs.

The ultimate goal of this work is to propose reliable protection strategies that accommodate the unique operational characteristics of SSSCs, ensuring that distance protection systems maintain their effectiveness and selectivity even as grid configurations become more advanced.

2 Literature Review

This chapter summarises a literature review and acts as a foundation for the following sections.

Section 2.1 covers the basics of protection technology and commonly used protection functions for line protection, such as overcurrent time protection, distance protection, and differential protection.

Chapter 2.2 provides an overview of the topic Flexible AC Transmission Systems (FACTS) and discusses typical parallel-connected devices such as the Static Var Compensator (SVC) and Static Synchronous Compensator (STATCOM), as well as serial FACTS devices like the Thyristor Controlled Series Compensator (TCSC) and Static Synchronous Series Compensator (SSSC). It also includes a hybrid topology that combines parallel and serial FACTS technologies, the Unified Power Flow Controller (UPFC). This chapter, however, primarily focuses on serial devices and the control of active power flow in electrical power systems.

The basis for analysing the effects of SSSCs on conventional protection functions is provided by experience gained from securing TCSCs, as summarised in chapter 2.3. It also summarises previous studies that examine the impact of SSSCs on protection concepts. Findings from this section also serve as the foundation for the investigations and simulations conducted in this work.

2.1 Power System Protection

Protection systems and functions form an essential foundation for the safe and reliable operation of electrical power systems and, in this context, underpin the high level of supply security present in modern electrical systems. The requirements for a protection system can be described as follows [1]:

Reliability: Reliability implies that a protection system must distinguish between permissible operating conditions and fault conditions so that it only activates in the actual case of a fault.

Selectivity: Protection devices are responsible for safeguarding their primary protection zone. This guarantees that no more equipment than necessary is switched off in order to clear a fault. In addition, these devices can detect faults outside this primary zone, in what is called the overlap zone. This capability allows for the implementation of backup functions within a protection system. Coordination between protection devices must be such that an upstream device detecting a fault in the overlap zone does not activate before the device responsible for detecting the fault in its primary zone. This is referred to as selectivity, which can be achieved, for example, by exchanging teleprotection signals between protection devices and by setting time delays in the overlap zone.

Speed: The faster a protection system can detect a fault and initiate disconnection by a trip signal to the circuit breaker, the sooner fault locations and potentially defective equipment can be isolated. Ideally, this fault clearance should occur as quickly as possible. The speed of a protection system is fundamentally influenced by two factors: reliability and selectivity. The faster a protection system must

decide between normal operation and fault conditions, the less precise the decision may be, potentially leading to incorrect actions. Additionally, the staggered timing of protection functions to maintain selectivity may result in a non-negligible delay in fault clearance.

Simplicity: A guiding principle for protection systems is to keep them as simple as possible without sacrificing essential and required functionalities. Increasing the complexity of a protection system raises the potential for complications and, in the worst case, could even lead to the system's failure.

Economy: In terms of cost-effectiveness, protection systems should aim to provide all necessary protective functionalities at minimal financial cost. However, the cost of protection systems should be weighed against potential risks arising from system malfunction and the damage to protected equipment. Generally, more expensive protection systems are more reliable and can significantly reduce commissioning and operational expenses.

Definition: Pickup

The goal of protection systems is to reliably distinguish between fault conditions and normal operation. For this purpose, threshold or limit values are defined, which, when exceeded or fallen below, trigger the activation of a protective function. This activation is referred to as pickup [1,2,3]. Depending on the type of protection functions, different pickup mechanisms are commonly used, and these are explained in an application-oriented manner based on the respective protection functions in the following chapters.

Definition: Underfunction and Overfunction

The objective of protection technology is to detect faults reliably, quickly, and selectively. When these objectives are not met, there are two possible causes:

- Underfunction: In protection technology, an underfunction occurs when a fault within the primary protection zone of a protection device is not detected by the device itself, and backup protection equipment must take over fault clearance.
- Overfunction: An overfunction of a protection system occurs when a device is triggered even though the fault is not located within its primary protection zone. Overfunctions should be avoided, as they significantly reduce the supply security of the electrical power system.

Definition: Underreach and Overreach

Fault impedance measurements can be affected in such way that fault detection recognises a fault in zone where it is not actually located. Depending on the real fault location, this known as underreach or overreach.

- Overreach: If the fault is located above the reach of zone 1 of a distance protection relay and the relay detects the fault in zone 1, it is called overreach.
- Underreach: If the fault is located below the reach of zone 1 of a distance protection relay and the relay detects the fault in zone 2, it is called underreach.

2.1.1 Overcurrent Protection (ANSI Code 50, 51 und 67)

Overcurrent protection is a protection function used to detect short-circuits. The primary criterion for initiating and triggering overcurrent protection lies in the measurement and assessment of current. There are also methods where voltage and the short-circuit angle are used as additional fault criteria [1,2].

Overcurrent protection is categorized into three types:

- Instantaneous Overcurrent Protection (ANSI Code 50): Tripping occurs immediately upon exceeding the pickup threshold.
- Time-Delayed Overcurrent Protection (ANSI Code 51): Tripping occurs after a delay once the pickup threshold is exceeded.
- Directional Overcurrent Protection (ANSI Code 67): Tripping occurs after exceeding the pickup threshold and considering the directionality element, detecting faults in either the forward or reverse direction.

An exemplary integration of overcurrent protection is shown in Figure 1. Here, $\underline{I}_k$ and $\underline{U}_k$ represent the complex fundamental phasors of the short-circuit current $i_k(t)$ and the short-circuit voltage $u_k(t)$, which were measured via instrument transformers. The inclusion of voltage measurement is optional and depends on the requirements and specific conditions of the protection system.

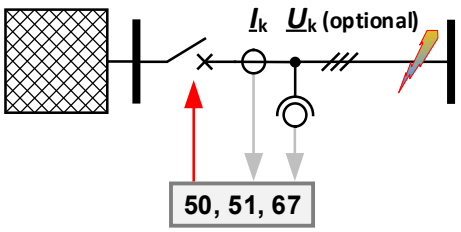


Figure 1: Integration of overcurrent protection

With regard to tripping characteristics, an additional distinction is made between independent definite-time overcurrent protection (DTO) and dependent (inverse) time overcurrent protection (ITO). The following chapters will focus exclusively on DTO.

2.1.1.1 Pickup- and Tripping-Criteria

For the pickup and tripping of DTOs, it is possible, depending on the protection device used, to configure multi-stage characteristics. A multi-stage tripping characteristic of a DTO can generally be set according to the following features:

- Threshold values for conductor current levels, negative-sequence current levels, or zero-sequence current levels, with corresponding individual time settings (delay times)
- Direction-dependent blocking of time stages
- Voltage-dependent blocking of time stages
- Blocking through additional binary signals

In the configuration, a distinction is made between the current pickup stage *I*> and the high-current stage *I*>>. The difference lies within the fact that exceeding the threshold *I*>> leads to an instantaneous tripping of the protection device, while exceeding *I*> initiates the respective time stage.

By additionally considering the voltage at the measuring point, both the fault direction and the voltage level at the time of tripping can be taken into account. Considering the voltage level is particularly useful when the minimum short-circuit current and the maximum load current are of similar magnitudes. The direction of a fault is determined by the phase angle between current and voltage. In this context, the allocation of measured quantities plays a crucial role. Depending on the detected fault loop, the phase relationships of different voltages (line-to-ground or line-to-line) to the fault current serve as directional criteria. Furthermore, the quality of the voltage signals is relevant for determining the direction. In cases of poor voltage signal quality, such as a relatively low amplitude during a close three-phase fault, a voltage memory can be used, containing the healthy pre-fault voltage. Limitations of the voltage memory may arise due to large frequency deviations, which make it unavailable.

Figure 2 shows an example of a multi-stage tripping characteristic of a DTO. The first three stages of the DTO are set to "forward," so a reverse-direction fault would not initiate the time stages in these levels. Stage 4 is non-directional, and stage 5 (*I*>>) is an instantaneous high-current stage without delay.

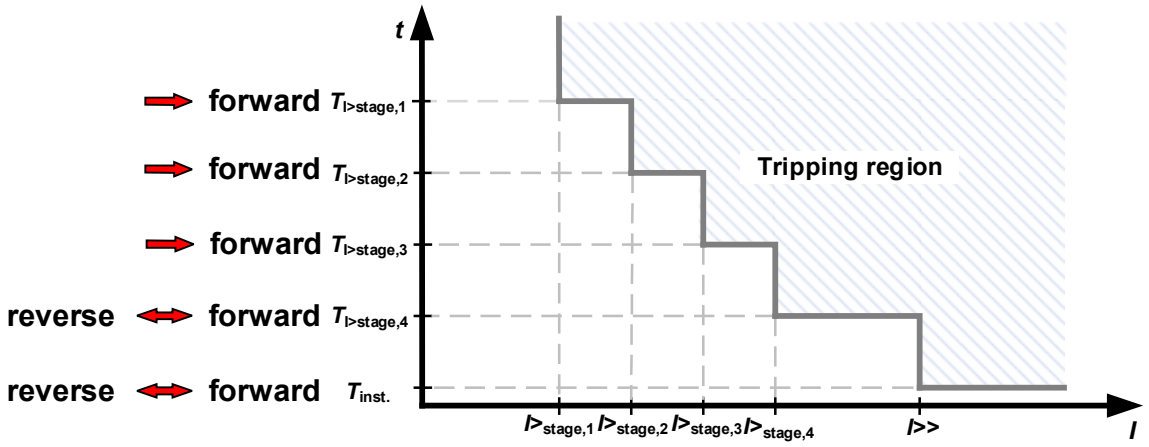


Figure 2: Example of a multi-stage DTO tripping characteristic with directional dependence and high-current stage (based on [2], page 126, Figure 4.7)

2.1.1.2 Setting Guidelines and Notes

Parameterization of Current Levels and Time Stages

When setting up the DTO, it is important to note that it is not intended as an overload protection for equipment. Therefore, thermal limits must be considered when configuring the DTO. The first stage of the DTO, $I>_{\mathrm{stage,1}}$ is typically set with a safety margin of 20 % (k_{s} = 1.2) relative to the maximum load current I_{load}, as shown in equation (1).

$$I >_{\mathrm{stage,1}} = I_{\mathrm{load}} \cdot k_{\mathrm{S}} \tag{1}$$

If additional stages or following protection devices are present, their settings should be coordinated with regard to selectivity.

During the configuration of a protection system, it may occur that selective setting of DTOs leads to exceeding the system's thermal short-circuit strength. In such cases, the high-current stage and its instantaneous tripping can be helpful. The high-current stage value, *I>>,* can be calculated based on equation (2), using the maximum short-circuit current of the downstream station $I_{k,max}$ and a safety factor k_s = 1.2 to 1.6.

$$I >> = I_{\mathrm{k,max}} \cdot k_{\mathrm{S}} \tag{2}$$

With regard to setting the time grading and the setpoints of individual time stages, the configuration is application-specific. The stage interval, or grading time, should be selected in the range of 300 to 400 ms [2].

Measuring Circuit Monitoring (MCM) and Blocking of Voltage-Dependent Functions

Measuring circuit monitoring is a supervision function in a fault-free state that detects asymmetries and missing measurements in current and voltage data. Once these irregularities are identified, it blocks protection functions to prevent malfunctions. In the event of a fault, MCM is deactivated. When MCM detects erroneous voltage measurements in overcurrent protection (DTO), it deactivates voltage-dependent functions in the DTO [5].

Emergency Overcurrent Protection

Distance protection relays (chapter 2.1.2) can only operate correctly if the measurements of voltages and currents are available. In the event of a voltage measurement failure, the MCM blocks the distance protection, and an emergency DTO protection is activated, which takes over the short-circuit protection based solely on the line currents, independent of the faulty voltage measurements.

2.1.2 Distance Protection (ANSI Code 21)

Distance protection is typically used as the primary protection function for transmission lines. Its operating principle is based on calculating the loop impedance at measurement points within a line branch. A schematic representation of the operating principle of distance protection is shown in Figure 3.

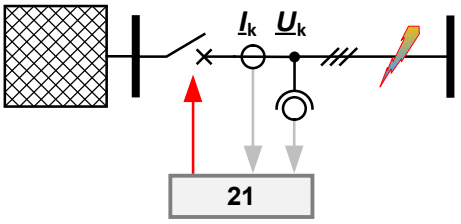


Figure 3: Integration of Distance Protection

$$\underline{Z}_k = \frac{\underline{U}_k}{\underline{I}_k} \tag{3}$$

$$u_k(t) = R_k \cdot i_k(t) + L_k \cdot \frac{di_k(t)}{dt} \tag{4}$$

Distance protection relays analyse six different fault loops (L1-G, L2-G, L3-G, L1-L2, L2-L3, L3-L1), with the selection of specific loops depending on the associated pickup signals [4,5,7].

Two methods are distinguished for analysing loop impedances. The analysis can be conducted either in the frequency domain using complex fundamental phasors (see Equation (3)) or in the time domain based on line differential equations (see Equation (4)). $\underline{U}_k$ and $\underline{I}_k$ represent the complex fundamental phasors of $i_k(t)$ and $u_k(t)$, R_k und L_k are the short-circuit resistance and inductance and $\underline{Z}_k$ is the complex short-circuit impedance.

In addition to calculating the six loops, the analysis of the measured quantities can also be performed by using symmetrical components. This additional approach is known as the “reactance method” [4]. Regardless of the chosen method, the determined impedances are ultimately compared with the line parameters. This enables the detection of faults and the determination of electrical distances to these faults. However, it should be noted that the resistive component of the measurable impedance is particularly influenced by the type of fault.

2.1.2.1 Pickup- and Tripping-Criteria

For distance protection, usually four pickup mechanisms can be used [4].

***I* – pickup / overcurrent pickup:** Figure 4 illustrates the basic operating principle of the overcurrent pickup function. For this pickup mechanism, the protection device picks up, as soon as a current is measured, that exceeds the pickup threshold I_{pickup}. In this context, the pickup reliability margin is an indicator of how reliably a short circuit is detected by the overcurrent pickup, and is equal to the distance between I_{pickup} and the minimal short-circuit current $I_{k,min}$. The space in between the max. thermal current of the conductors, I_{therm} and I_{pickup} is equal to a safety margin which ensures that a possible overload operation point will not trigger the overcurrent pickup mechanism.

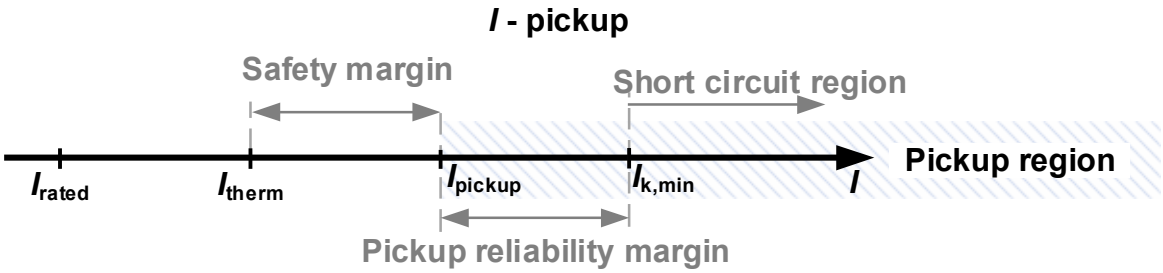


Figure 4: Overcurrent pickup for distance protection based on [4]

***U* / *I* – pickup:** If the current is not sufficient as the sole pickup criterion, the voltage dependent overcurrent pickup can be used. Its operation is schematically illustrated in Figure 5 (left). If a short-circuit current exceeds the upper pickup threshold *I*>>, the distance protection will pickup regardless of the measured voltage. For currents in between *I*>> and the lower pickup threshold *I*>, the protection device will only trigger if the voltage drops below the upper or lower voltage pickup threshold $U_{I>>}$ and $U_{I>}$. For currents below *I*>, the *U* / *I* – pickup will not trigger the distance protection.

***U* / *I* / *φ* - pickup:** The voltage-dependent overcurrent pickup mechanism can be advanced by additionally considering the angle φ between $\underline{U}$ and $\underline{I}$. This kind of pickup mechanism uses two different characteristic curves, *U(Iφ>) and U(I>>)*. Its characteristic is shown in Figure 5 (right). This mechanism uses the fact that typical values for load angles range between -30° to +30°, while line characteristic angles for high and extra-high voltage systems range from approximately 78° to 85° [4]. If a measured angle exceeds the load angle, the system can switch from the *U(I>>)*-characteristic to the more sensitive *U(Iφ>)*-characteristic.

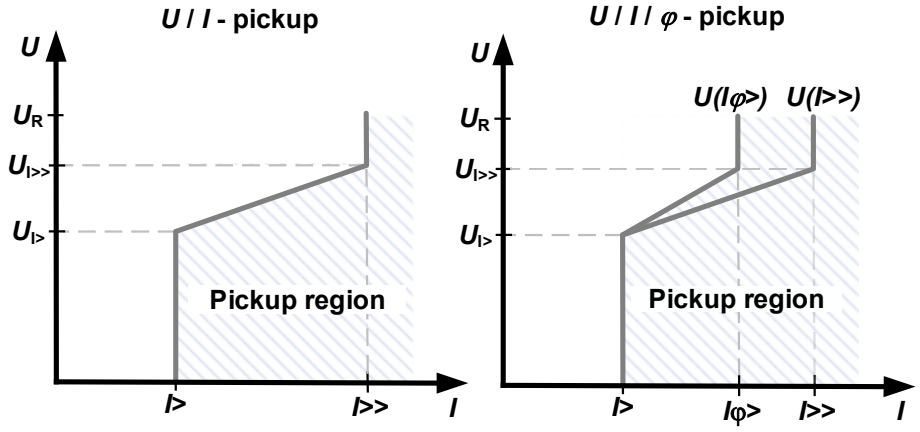


Figure 5: U / I – pickup (left) and U / I / φ – pickup (right) based on [4]

***Z* – pickup / impedance - pickup:** Two methods of the impedance pickup are shown in Figure 6. On the left, a shifted MHO characteristic is shown, while on the right, a polygon characteristic is depicted. When a protection device calculates an impedance that lies within the areas shown in the complex plane, a pickup by the protection relay occurs. In both figures, the line characteristic is also indicated, describing the *X/R* ratio of the protected line. For the impedance pickup, it is also possible to define a load area in the complex plane. This area lies within the pickup zone but blocks it to prevent tripping [5].

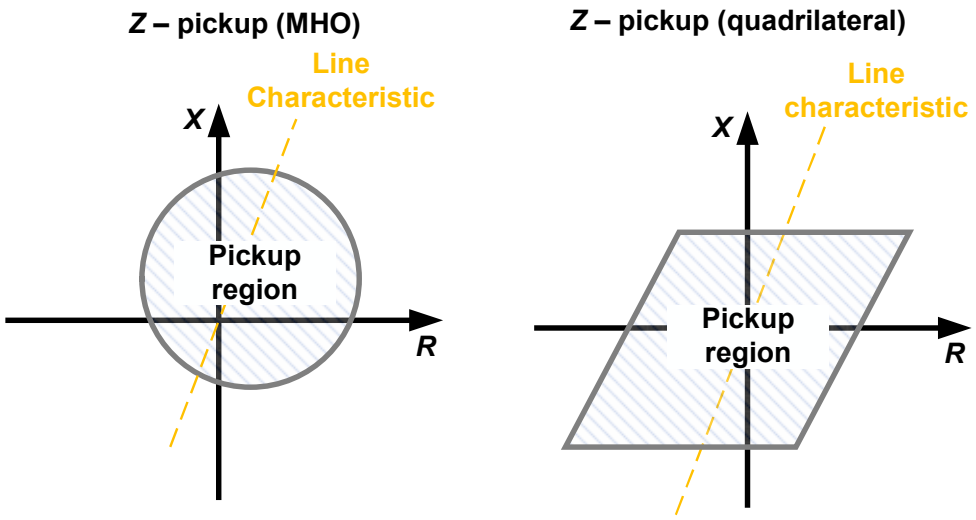


Figure 6: Z – Pickup with MHO- (left) and quadrilateral characteristics (right) based on [4]

Regardless of the type of pickup mechanism used, distance protection tripping operates based on impedance-time characteristics. This means that tripping occurs based on the measured impedance after a corresponding time delay. In this context, different tripping characteristics with various zones are introduced. The first zone is typically set for the protected object and trips faults without delay. Subsequent zones are then graded with the following protection devices in mind for selectivity. This grading will be explained in more detail in the following.

MHO Tripping Characteristic

In addition to the MHO or circular pickup characteristic (as in Figure 6), it is also possible for the tripping characteristics to be realised as MHO characteristic. However, this is less relevant for this work, and therefore it will not be elaborated on further here. Additional information on this topic can be found in [5, 7]. It should be noted, that the MHO characteristic historically represents the initial form of numerical distance protection devices and is still widely used today.

Quadrilateral Tripping Characteristic

In addition to the quadrilateral impedance pickup characteristic, it is also possible to implement a quadrilateral tripping characteristic. This provides very flexible adjustment options, as resistances and reactances can be set separately for the respective zones. The actual geometric configuration of the tripping polygons is fundamentally influenced by the specific protection device manufacturer and the parameters used in the configuration, as referenced in [5, 7]. An example of a quadrilateral tripping characteristic is illustrated in Figure 7. In this example, three zones, Z1, Z1B and Z2, are parameterized (depending on the manufacturer and application, more zones may also be configured). For the zone settings, the zone boundaries for the respective resistances (*R1*, *R1B* and *R2*) and reactances (*X1*, *X1B* and *X2*), as well as the associated tripping delays, are specified. An exception to the tripping delay is Z1B, which is the overlap zone. This zone does not operate with a time delay but is triggered by signals linked with additional functions such as the Automatic Reclosure (AR) function or teleprotection methods.

While the reactances *X1*, *X1B* and *X2* are based on the positive-sequence impedance of the line and the set distance of the respective zone, the resistances *R1*, *R1B* and *R2* consider the fault resistance R_f. Therefore, the line resistances are subject to the arc reserve R_{arc}. Additionally, different setting values for line-to-line and line-to-ground polygons are possible.

Also required are the characteristic values of the protected line. Typically, the positive-sequence and zero-sequence impedances ($\underline{Z}_1$, $\underline{Z}_0$ and $\varphi_{line} = \arctan\frac{\mathrm{Im}\{\underline{Z}_1\}}{\mathrm{Re}\{\underline{Z}_1\}}$) and the line length are needed for the fault locator. The fault locator is an additional function that calculates the distance of the fault based on measured impedances and the line characteristics. The angle α is necessary in cases where the fault is fed from multiple sides, which can lead to a distortion of the determined reactance. The directional decision is manufacturer-dependent and based on directional characteristics (indicated here by a straight line in the second and fourth quadrants).

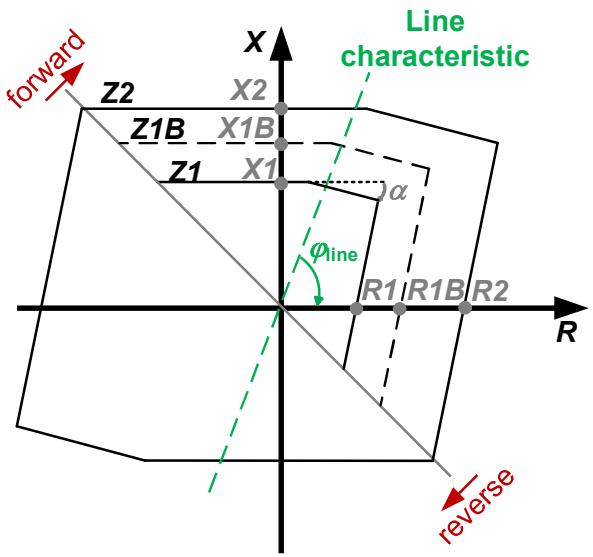


Figure 7: Example structure of a quadrilateral tripping characteristic based on [3,5]

Grading and Coordination of Multiple Zones and Relays

Figure 8 shows the grading plan for three exemplary protection devices Relay1, Relay2 und Relay3. Each device is connected in the branch of its associated lines, Line1, Line2, and Line3. To maintain selectivity when serially connecting distance protection devices, sufficient safety margins must be planned between the individual impedance zones. The staging plan outlines the impedance zone boundaries of the respective protection devices along with their associated time delays.

The first zone of each protection device ($Z1_{Relay1}$, $Z1_{Relay2}$ and $Z1_{Relay3}$) is to be set in such a way that 80 to 90 % of the associated line is tripped instantaneously ($T1$). The setting is not adjusted to the full 100 % of the line because the exact calculation of the fault distance is not possible due to load flow-related influences on the reactance measurement, inductive coupling in the zero-sequence system, inaccuracies of the measuring transformers, and line characteristics, which could lead to non-selective tripping.

Further settings for the second zones ($Z2_{Relay1}$ and $Z2_{Relay2}$) and the third zone ($Z3_{Relay1}$) are made based on the protection zones of the subsequent protection relays to ensure sufficient safety margins. Chapter 2.1.2.3 will provide a more detailed explanation of typical parametrisation values for distance protection. In addition to the grading of impedance zone boundaries, a time grading is also implemented. Typically, a spacing of Δt = 300 to 400 ms is chosen (e.g. $T_1 \approx 0$ ms, T_2 = 400 ms, T_3 = 800 ms) [4].

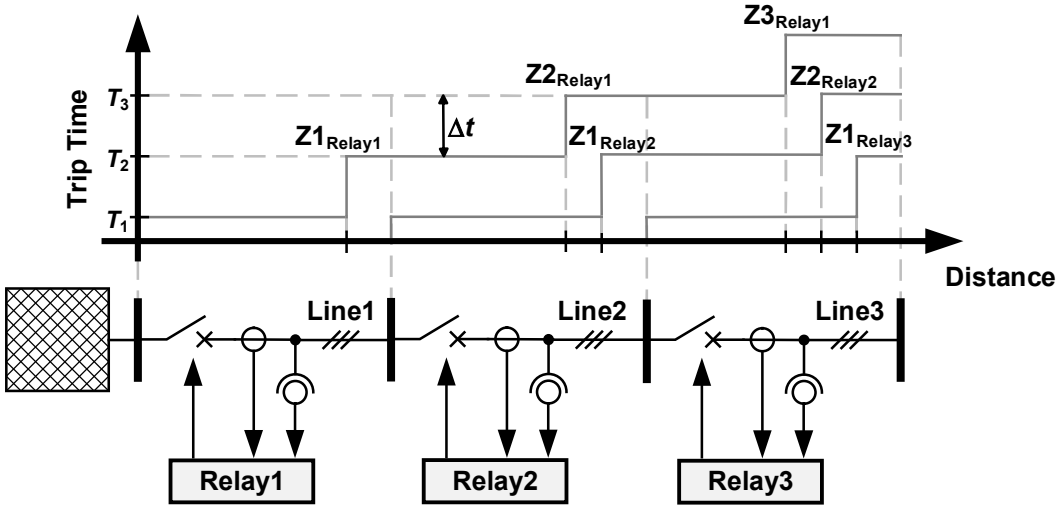


Figure 8: Grading plan of three distance protection devices Relay1, Relay2 and Relay3

2.1.2.2 Teleprotection Schemes for Distance Protection

In addition to parameterizing different independent zones, there is also the possibility of implementing a controlled zone, the overlap zone Z1B, with an associated communication channel to enable the interaction of protection devices [3,5]. These functions are based on data exchange between at least two opposite stations (in the case of a multi-terminal line, data exchange could also occur among more than two stations). The goal of these additional functions is to quickly disconnect faults that occur outside the first protection zone (80 to 90 % of the line length). The overlap zone is typically set to approximately 120% of the line length. Three methods are available for this purpose:

- Underreach schemes
- Overreach schemes
- Blocking schemes

An example topology that will be used to explain these methods is illustrated in Figure 9.

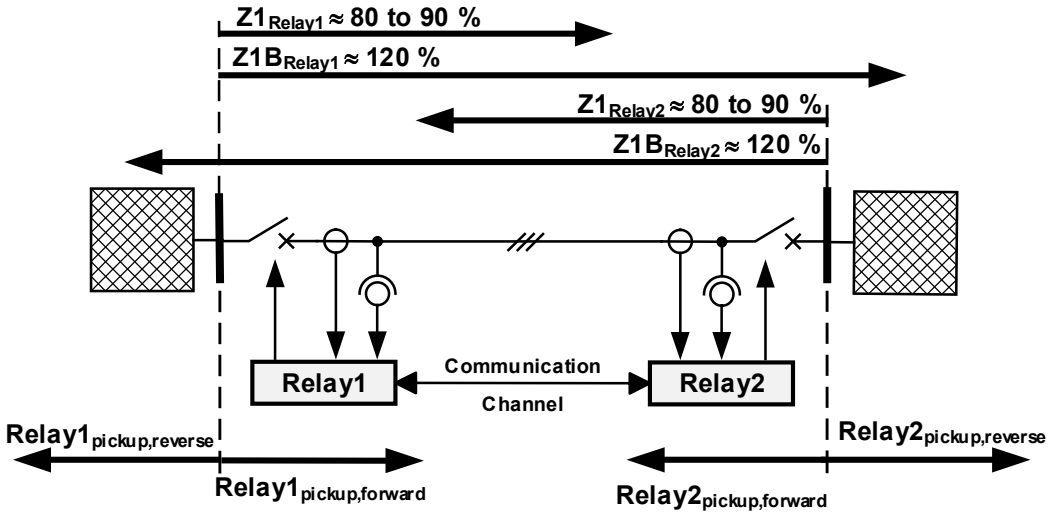


Figure 9: Teleprotection setup with two relays Relay1 and Relay2

Underreach schemes

- **Permissive underreach transfer trip:** If Relay1 trips in $Z1_{Relay1}$, a signal is sent to the remote device, Relay2. If Relay2 picked up in forward direction ($Relay2_{pickup,forward}$), the receiving signal from Relay1 leads to a trip of Relay2.
- **Permissive underreach transfer trip (PUTT) with overlap zone Z1B:** If Relay1 trips in zone $Z1_{Relay1}$, a signal is sent to the remote device, Relay2. This signal will enable the overlap zone $Z1B_{Relay2}$ and lead to a trip of Relay2, if the fault is detected in $Z1B_{Relay2}$.
- **Direct (underreach) transfer trip:** If Relay1 trips in $Z1_{Relay1}$, a signal is sent to the remote device, Relay2. This signal leads to a direct trip of Relay2.

Overreach schemes

- **Permissive overreach Transfer Trip (POTT):** If the fault is detected by Relay1 in $Z1B_{Relay1}$, a signal is sent to the remote device, Relay2. If Relay1 simultaneously receives an identical signal from Relay2, this will ultimately lead to the tripping of Relay1. Meanwhile, same condition applies to the tripping of Relay2. Therefore, the prerequisite for an instantaneous tripping is that both devices detect the fault in the overlap zone.
- **Directional Comparison:** This kind of overreach scheme can also be triggered by the direction of the pickup (directional comparison of Relay1 and Relay2). If Relay1 picks up in forward direction ($Relay1_{pickup,forward}$), a signal is sent to Relay2. If Relay2 also picks up in forward direction ($Relay2_{pickup,forward}$), while also receiving the direction comparison signal from Relay1, it will lead to the tripping of Relay2. On the pickup, Relay2 also sends a comparison signal to Relay1, which will also lead to a trip of Relay1.

Blocking schemes

- **Blocking of overreach Zone Z1B:** For this method, the detection of a fault in the overlap zone of Relay1, $Z1B_{Relay1}$, leads to a trip of Relay1, if no blocking signal is received by Relay2. A blocking signal is transmitted by Relay2, if it detects a fault in its reverse direction by a pickup of $Relay2_{pickup,reverse}$.
- **Reverse Interlocking:** The blocking of the controllable overlap zone can also be utilized as a method to implement a busbar protection system with radial connections [3].

2.1.2.3 Setting Guidelines and Notes

Zone Setting for Quadrilateral Characteristics

Table 1 summarises recommendations from [2] for setting the uncontrolled zones of distance protection devices as shown in Figure 8 – in this case for Relay1. The primary protection zone of the distance protection devices is set to 85 % of the directly associated line. However, these settings are merely guidelines. In practice, the sizing of the protection settings is carried out while considering the existing conditions. Furthermore, these setting recommendations primarily apply to the reactances of the respective zones, while additional guidelines need to be considered for the resistances. Regarding time grading, the individual zones are typically delayed between 300 and 400 ms.

Table 1: Setting recommendations based on [2]; *in which* $Z1_{Relay1}$, $Z2_{Relay1}$ *and* $Z3_{Relay1}$ *are the zone parameters and in which* $\underline{Z}_{Line1}$, $\underline{Z}_{Line2}$ *and* $\underline{Z}_{Line3}$ *are the line impedances based on Figure 8*

	Single line	**Double line**
$\mathbf{Z1_{Relay1}}$	$0.85 \cdot \underline{Z}_{Line1}$	$0.85 \cdot \underline{Z}_{Line1}$
$\mathbf{Z2_{Relay1}}$	$0.85 \cdot \underline{Z}_{Line1} + 0{,}72 \cdot \underline{Z}_{Line2}$	$0.85 \cdot \underline{Z}_{Line1} + 0.41 \cdot \underline{Z}_{Line2}$
$\mathbf{Z3_{Relay1}}$	$0.85 \cdot \underline{Z}_{Line1} + 0.72 \cdot \underline{Z}_{Line2} + 0.61 \cdot \underline{Z}_{Line3}$	$0.85 \cdot \underline{Z}_{Line1} + 0.41 \cdot \underline{Z}_{Line2} + 0.35 \cdot \underline{Z}_{Line3}$

Resistance / Arc Reserve R_{arc}

Considering the settings of the zones according to Table 1, it is advisable to incorporate additional safety margins regarding the resistances of the zone settings for overhead lines. These margins are typically adjustable separately for line-to-line and line-to-ground faults. The necessity for resistance reserve can be attributed to the occurrence of arcs and the transition resistances to the ground for ground faults, which is why these safety margins are also known as arc reserve. The resistance that is effective at the fault location is composed of the arc and associated transition resistances is referred to as the fault resistance R_f. Reference values for R_{arc} can be found in [3,6].

Ground Factor $\underline{k}_E$ and Parallel Compensation Factor $\underline{k}_M$

In the case of ground faults, it is necessary to calculate the line-to-ground loop impedance using the ground factor $\underline{k}_E$, which compensates for the contribution of the return conductor in the earth loop. $\underline{k}_E$ is calculated using the positive- and zero-sequence impedances $\underline{Z}_1$ and $\underline{Z}_0$, or alternatively by using the conductor impedance $\underline{Z}_L$ and the earth impedance $\underline{Z}_E$, according to equation (5) [3,4].

$$\underline{k}_{\mathrm{E}} = \frac{1}{3} \cdot \left(\frac{\underline{Z}_0}{\underline{Z}_1} - 1 \right) = \frac{\underline{Z}_{\mathrm{E}}}{\underline{Z}_{\mathrm{L}}} \tag{5}$$

Subsequently, $\underline{k}_{\mathrm{E}}$ can be incorporated into the equations for the calculation of the line-to-ground loop impedance. For a relay R, the line-to-ground loop impedance of any phase, $\underline{Z}_{\mathrm{R,LE}}$, is calculated by the line-to-ground voltage $\underline{U}_{\mathrm{R,LE}}$ the phase current $\underline{I}_{\mathrm{R,L}}$ the earth current of the considered branch, $\underline{I}_{\mathrm{E}}$, and the ground factor $\underline{k}_{\mathrm{E}}$ as shown in equation (6).

$$\underline{Z}_{\mathrm{R,LE}} = \frac{\underline{U}_{\mathrm{R,LE}}}{\underline{I}_{\mathrm{R,L}} + \underline{k}_{\mathrm{E}} \cdot \underline{I}_{\mathrm{E}}} \tag{6}$$

When considering double lines and line-to-ground faults, the mutual coupling of the zero-sequence system between the faulted and healthy system can influence the distance measurement for the faulty branch. In order to compensate this influence, the parallel compensation factor $\underline{k}_{\mathrm{M}}$ can be calculated with the positive- and mutual zero-sequence impedances $\underline{Z}_1$ and $\underline{Z}_{0\mathrm{M}}$ based on (7) and incorporated into the calculation of the line-to-ground loop impedance in (8). Here, $\underline{I}_{\mathrm{E1}}$ is the earth current of the faulty branch, while $\underline{I}_{\mathrm{E2}}$ is the earth current of the healthy parallel circuit [3].

$$\underline{k}_{\mathrm{M}} = \frac{1}{3} \cdot \left(\frac{\underline{Z}_{0\mathrm{M}}}{\underline{Z}_1} \right) \tag{7}$$

$$\underline{Z}_{\mathrm{R,LE}} = \frac{\underline{U}_{\mathrm{R,LE}}}{\underline{I}_{\mathrm{R,L}} + \underline{k}_{\mathrm{E}} \cdot \underline{I}_{\mathrm{E1}} + \underline{k}_{\mathrm{M}} \cdot \underline{I}_{\mathrm{E2}}} \tag{8}$$

Auto Reclosure Function (AR, ANSI Code 79)

A large number of arc short circuits on overhead lines extinguish automatically after disconnection by the protection system [1,2,3]. In this context, the Auto Reclosure (AR) function is used to reconnect lines to the network after a fault clearance. If the reconnection is successful and the fault has been cleared, it is referred to as a successful AR. If the fault is still present, it is termed an unsuccessful AR. The benefits of a double AR (AR after an initially unsuccessful reconnection) are also recognized in practice. Overall, the AR significantly contributes to enhancing the reliability of supply in electrical power systems [2]. Depending on the neutral point treatment of a network, either single-pole or three-pole ARs are performed. In solidly grounded networks, single-pole ARs are frequently used.

For the AR to be effective, it is crucial that a fault is quickly disconnected at all line ends. This allows the arc to extinguish as quickly as possible. In this regard, the overlap zone Z1B, which is typically set to about 120 % of the line length, trips quickly when the AR is available. It is also advisable to implement teleprotection procedures to prevent unselective tripping (even if these would be quickly resolved by an AR). In addition to the overlap zone, the time-staged impedance zones (Z1, Z2, etc.) operate independently of the AR status, meaning that if the AR is unavailable, a conventional trip according to the impedance-time characteristic will occur. Additional requirements for the availability of AR are also imposed by circuit breakers, as they must be designed for multiple consecutive switching cycles. Further information on AR can be found in [3,5,7].

Power Swing and Power Swing Detection

The rotor angle of generators can vary over time due to switching operations and faults, which inherently leads to power swings in the electrical power system [1,2,3,4]. These power swings have a direct impact on the measurable impedances in distance protection devices. A simplified network topology in the positive-sequence system is shown in Figure 10 to illustrate this.

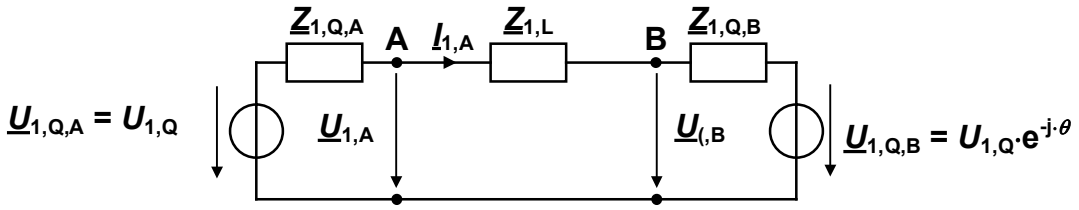


Figure 10: Simplified equivalent circuit for explaining power swings based on [4]

The voltages $\underline{U}_{1,Q,A}$ and $\underline{U}_{1,Q,B}$ represent the internal voltages of two rotating synchronous machines. For the following analysis, it is assumed that the magnitudes of both voltages share a common value $U_{1,Q}(t)$. Additionally, the following relationship for the transmission angle $\vartheta(t)$ applies based on the arguments of the phasors, as shown in equation (9).

$$\vartheta(t) = \arg\{\underline{U}_{1,Q,A}(t)\} - \arg\{\underline{U}_{1,Q,B}(t)\} \tag{9}$$

During power swings of the generators, the transmission angle $\vartheta(t)$ changes, as shown in *Equation* (10).

$$\frac{\mathrm{d}\vartheta(t)}{\mathrm{d}t} \neq 0 \tag{10}$$

The current $\underline{I}_{1,A}$ can be calculated based on (11).

$$\underline{I}_{1,A} = \frac{U_{1,Q}(t) \cdot (1 - e^{j\cdot\vartheta(t)})}{(\underline{Z}_{1,Q,A} + \underline{Z}_{1,L} + \underline{Z}_{1,Q,B})} \tag{11}$$

According to Figure 10 and based on equations (9), (10) and (11), the impedance from the perspective of node A can be described as shown in (12).

$$\underline{Z}_{1,A}(t) = \frac{\underline{U}_{1,A}(t)}{U_{1,Q}(t) \cdot (1 - e^{j\cdot\vartheta(t)})} \cdot (\underline{Z}_{1,Q,A} + \underline{Z}_{1,L} + \underline{Z}_{1,Q,B}) \tag{12}$$

Equation (12) shows that power oscillations affect the measurable impedances in line branches. A quantitative comparison of the temporal behaviour of the absolute values of the impedances during a fault and oscillation process is presented in Figure 11. It is evident, that the fault impedance changes rapidly, while the oscillation process occurs at a significantly slower rate. Furthermore, power oscillations can be identified based on additional criteria such as their periodicity or symmetry (no zero sequence). The oscillation blocking function is designed to detect power oscillations, thereby preventing erroneous tripping of the distance protection in the event of a power oscillation [2].

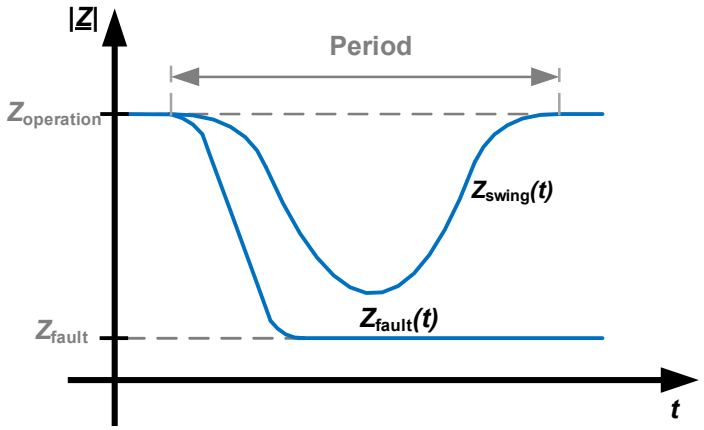


Figure 11: Quantitative progression of absolute impedance values during power swing and fault based on [2]

Measurement Circuit Monitoring (MCM) and Emergency Overcurrent Protection

The Measuring Circuit Monitoring (MCM) is a control function typically implemented in digital protection devices [7]. It monitors the plausibility of current and voltage transformer measurements and blocks affected protection functions in the event of a fault. If there is an error in the measurement input between the voltage transformers and the protection device, the MCM detects this fault. Since distance protection cannot function properly without voltage measurements, the next step is to block distance protection and activate the emergency overcurrent protection. This enables continued protection of equipment.

Voltage Memory

A voltage memory can be useful during a fault when the measured voltage values do not enable reliable fault detection. Low-quality voltage signals are often found in branches with weak infeed, such as converter-coupled generation plants. Furthermore, in series-compensated lines, the effect of voltage inversion can occur [3,7]. In this context, the voltage memory can provide a possible solution. However, the occurrence of an additional effect, current inversion, can negate the advantage of the voltage memory in series-compensated lines [3,5,7]. These situations are discussed in more detail in chapter 2.3.2.

End Time

In the case of distant faults, a scenario may occur where a distance protection device picks up, but no tripping occurs according to the impedance-time characteristic based on the set zones. In this context, end times can provide a solution [7]. These serve as backup protection functions that lead to tripping based on pending pickups after the expiration of time delays (which are set to be greater than the maximum grading times).

Additionally, a distinction can be made between directional and non-directional end times. In the case of directional end time, tripping occurs only after the set delay if the pickup detects a fault in the forward direction. The non-directional end time triggers independently of the direction after the delay has elapsed.

Transformation from primary- to secondary values for impedance configuration

The parametrization of the pickup and tripping parameters of the protection devices can be done in both high- ($\underline{U}_{HV}$, $\underline{I}_{HV}$), as well as in low-voltage quantities ($\underline{U}_{LV}$, $\underline{I}_{LV}$). For the transformation of impedances from high-voltage to low-voltage side, the transformer ratio of the voltage transformer t_U and the current transformer t_I are needed. The secondary impedance $\underline{Z}_{LV}$ can be calculated by following equation (13).

$$\underline{Z}_{LV} = \frac{\underline{U}_{LV}}{\underline{I}_{LV}} = \frac{\frac{\underline{U}_{HV}}{t_U}}{\frac{\underline{I}_{HV}}{t_I}} = \frac{\underline{U}_{HV}}{\underline{I}_{HV}} \cdot \frac{t_I}{t_U} \tag{13}$$

2.1.3 Differential Protection (ANSI 87)

The idea of differential protection is based on Kirchhoff's current law which states, that the geometric sum of one node has to be (ideally) zero at any moment. Differential protection devices compare current measurements by their amplitude differentiate between normal operation and a fault inside the protection zone / at the protected object. Differential relays are typically used for protecting transformers (87T), but can also be used for protecting overhead lines or cables (87L). Figure 12 illustrates the idea of differential protection for normal operation and for a faulty protected object.

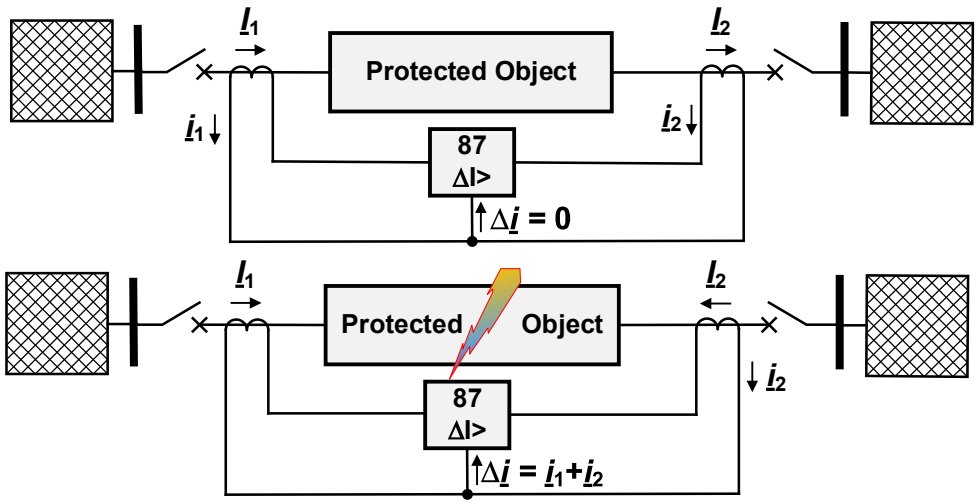


Figure 12: Basic topology for differential protection; above: normal operation; below: fault

In the example Figure 12 (above), the secondary currents $\underline{i}_1$ and $\underline{i}_2$ flow in opposite directions, which leads to a differential current $\Delta\underline{i}$ = 0 A. For the faulty example in Figure 12 (below), the geometric sum of $\underline{i}_1$ and $\underline{i}_2$ leads to a differential current, which, depending on threshold values, can lead to a trip if the differential protection function.

Figure 13 shows the pickup characteristic for a classic differential protection device. For the ideal short-circuit inside of the protected object, the differential current $\underline{I}_D$ is equal to the stabilisation current $\underline{I}_S$, which is why the ideal fault characteristic is along the abscissa. Due to measurement errors (also including current transformer saturation) and further deviations (for transformers as protected object:

tap changing, magnetization current), a relay characteristic is configured based on these expected differences between $\underline{I}_D$ and $\underline{I}_S$ for normal operation.

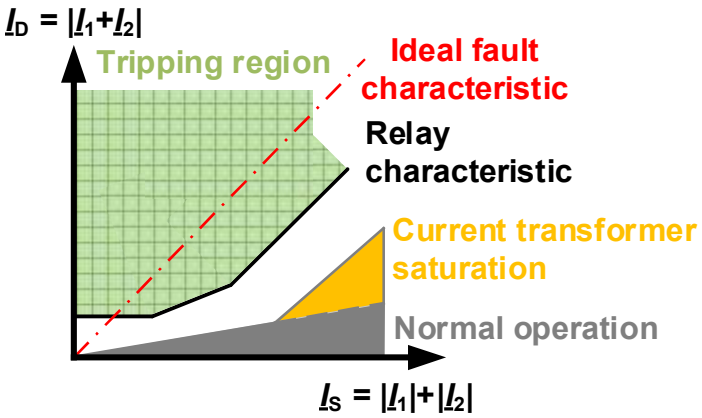


Figure 13: Relay characteristic of a differential protection device

The current measurements can be transmitted by wire connection or digitally decoded and transmitted by digital interfaces. This enables the possibility to transmit the current values over long-distance connections enabling the possibility of using differential protection as protection function for lines. Limitations occur regarding the dependency of auxiliary bus transfer, which does not allow using differential protection for lines (without additional measurements or by using a flexible communication based on e.g. IEC 61850).

The main idea of this chapter was to introduce the concept of differential protection. For the following chapters, it will not be further investigated. For further information on differential protection, [8] can be considered.

2.2 Flexible AC Transmission Systems (FACTS)

FACTS are semiconductor-based equipment used in electric networks that enable a more flexible operation of the power grid. They are to be connected in series or parallel (or a combination of both) to an electric grid and offer possibilities for optimising grid operation. This includes:

- Controlling the active power flow
- Controlling busbar voltages
- Reactive power compensation reducing power transfer losses
- Damping of power oscillations
- Increase transient stability margins

The following chapters will describe five different FACTS. This topic is mainly based on [9]. The main focus of this chapter lies on SSSCs.

2.2.1 Static Var Compensator (SVC)

SVCs are parallel connected FACTS that are based on capacitors and reactors controlled by thyristors. This kind of FACTS exchanges reactive power with the power grid allowing reactive power compensation or controlling busbar voltages.

Two simplified topologies of this kind of FACTS are shown in Figure 14. An SVC (left) consists of at least one Thyristor Controlled Reactor (TCR) and one Thyristor Switched Capacitor (TSC). In contrast, a simpler structure would be the Fixed Capacitor – Thyristor Controlled Reactor (FC-TCR; right). This device consists of a fixed capacitor (instead of a TSC) and a TCR. The advantage of the SVC over the FC-TCR lies in a smaller reactor rating for achieving an identical output reactive power, while reducing losses.

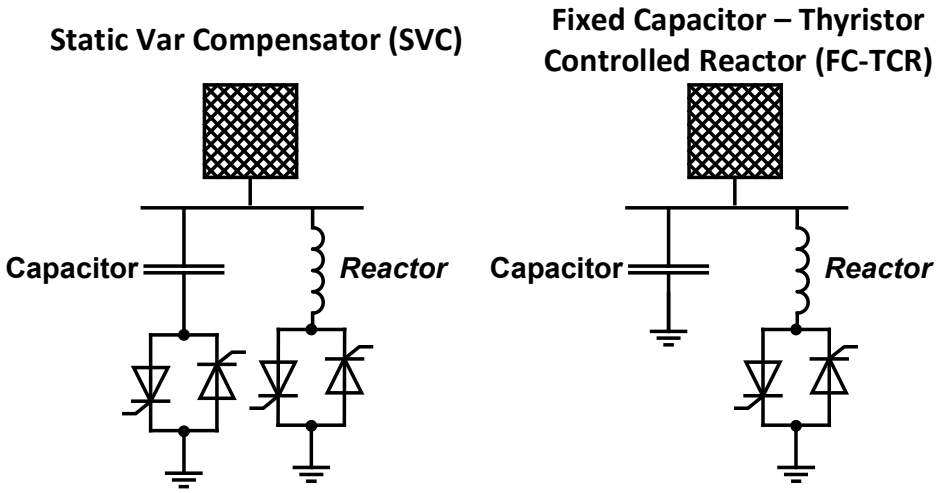


Figure 14: Static Var Compensator SVC and Fixed Capacitor - Thyristor Controlled Reactor FC-TCR, based on [9]

2.2.2 Static Synchronous Compensator (STATCOM)

STATCOMs are parallel FACTS that are based on Voltage Source Converters (VSC). This kind of FACTS topology is connected in parallel to the power grid and can exchange inductive and capacitive reactive power with the power grid. Based on a VSC, a STATCOM injects a reactive current into the power grid by controlling its modulated voltage considering its amplitude, phase and frequency. Due to its fast and precise injection capability, typical applications for STATCOM lie in dynamic voltage support for flicker mitigation, damping oscillations or could be used for improving transient stability margins [9].

A typical structure for a STATCOM is illustrated in Figure 15. The VSC consists of a DC link capacitor acting as an energy storage with a stable voltage, which is needed by the STATCOM to produce the required AC voltage waveform. For multilevel topologies, the DC link is distributed on the several modules. According to [4], STATCOMs are a typical application for modular multilevel converters (MMC). Essentially, a series inductor or coupling transformer is used for coupling the STATCOM to the power grid in order to limit current peaks in case that the DC link capacitor is shortened and discharges rapidly into the power grid [9].

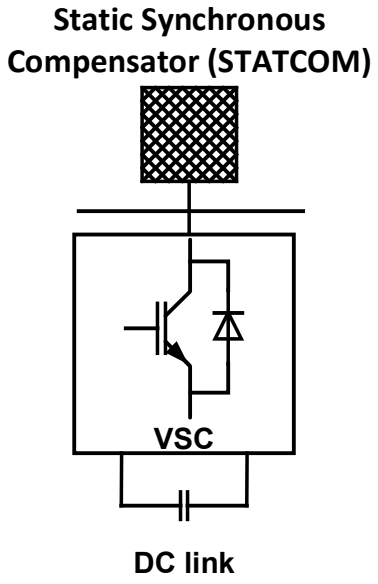


Figure 15: Static Synchronous Compensator (STATCOM) based on [9]

2.2.3 Thyristor Controlled Series Compensator (TCSC)

The principle of compensating long lines with a series capacitor is well known and widely applied in electrical power systems. The idea of series compensation is compensating the inductive line reactance enabling power transfer capabilities by increasing the maximum transmittable power P, as calculated in (14). Here, U_A and U_B correspond to the absolute values of the positive sequence phasors of the line-to-line voltages of two nodes A and B. δ is equal to the phase angle between the nodes and is also known as the transmission angle. X_{AB} is the inductive reactance connecting A and B and X_C is the capacitive reactance compensating X_{AB}.

$$P = \frac{U_A \cdot U_B}{X_{AB} - X_C} \cdot \sin \delta \tag{14}$$

For $X_C > 0$, P can be further increased, unlocking active power transmission capabilities. Series compensation therefore allows transmitting higher active power while maintaining a small transmission angle. By adding a TCR in parallel to a capacitance for series compensation, operational advantages for controlling the line reactance can be achieved, leading to the concept of TCSCs. The basic topology of a TSCS is shown in Figure 16.

The reactance of the TCSC can be controlled by the thyristor circuit which leads to the TSCS acting as a parallel tuned LC circuit. This unlocks the possibility of the TCSC behaving capacitive or inductive. Additionally, by approaching the resonance region of the parallel circuit, it is also possible to increase the effective capacitance of the TCSC above the actual value of the capacitance [9,10].

TSCSs are also equipped with protection equipment such as a voltage dependent resistor, a Metal Oxide Varistor (MOV), as well as a spark gap, that both protect the series capacitor from overvoltage. The additional bypass breaker of the TCSC is used for bypassing the TCSC during major fault events or when the compensation of the TCSC is not required.

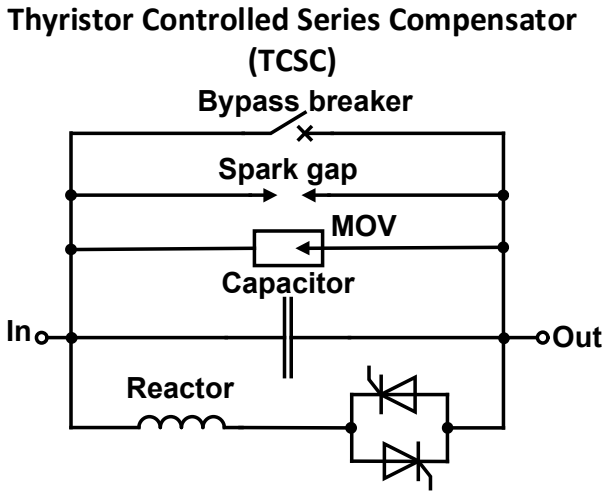


Figure 16: Thyristor Controlled Series Compensator (TCSC) based on [10]

2.2.4 Static Synchronous Series Compensator (SSSC)

The SSSC is a series FACTS device that controls the active power flow in a power grid. Its technology is based on VSC allowing operation in inductive and capacitive modes. The coupling of the VSC can be done by a series connected coupling transformer. Such a topology is illustrated in Figure 17. The VSC measures the current $\underline{I}$ and injects a voltage $\underline{U}_{inj}$ that is ±90° perpendicular to this current, acting inductive or capacitive. For this, the VSC needs to synchronise to the line current $\underline{I}$. This can be done by a PLL [12,13,17]. In order to protect the VSC from overcurrent, the SSSC is equipped with a bypass switch that activates during fault events. This protects the VSC from short circuit currents that could damage

its power electronics. The bypass can be both on the high and low voltage side of the transformer. Additionally, the bypass decisively reduces the influence of SSSC on distance protection [11,15,16,17].

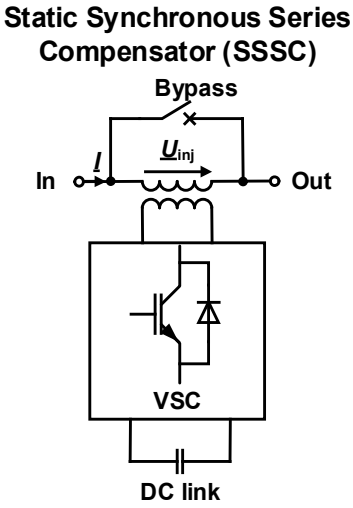


Figure 17: Static Synchronous Series Compensator (SSSC) based on [10]

Additional to SSSCs coupled by transformers, the SmartWires company developed a transformer-less and modular topology (m-SSSC) [16]. Its basic structure for one phase is shown in Figure 18. This kind of topology consists of High Pass Filters (HPF) and Low Pass Filters (LPF) as well as a MOV at the entry stage of the device. A thyristor-based Silicon Controlled Rectifier (SCR) allows the implementation of a fast acting bypass that protects the sub modules (SM) from short-circuit currents. This bypass can be triggered by the instantaneous value of $\underline{I}$ exceeding a threshold value. It is also activated for internal protection of the SMs. This example in Figure 18 consists of three SMs. An additional switch can be closed for monitoring mode of the m-SSSC (no capacitive or inductive voltage injection). During injection mode, the SCR is non-conducting and the switch is open. The current $\underline{I}$ therefore flows through the SMs.

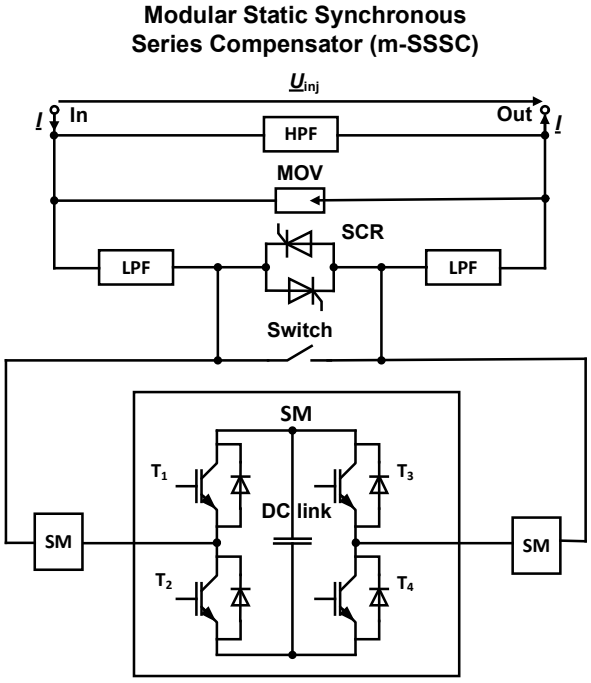


Figure 18: Modular Static Synchronous Series Compensator (m-SSSC) [11]

The SMs are built of full bridges with a DC link capacitor. Due to its modular concept, a m-SSSC contains multiple SMs leading to the distribution of the DC link voltage. This topology therefore has common characteristics with MMCs. For an ideal phase shift of ±90° between the injected voltage $\underline{U}_{inj}$ and the line current $\underline{I}$, no active power is exchanged between the DC link capacitor and the grid. This leads to a constant DC link capacitor voltage over a full period.

As soon as the phase shift is not at an absolute value of 90°, active power will be transmitted to or from the DC link capacitor, leading to a change in its mean voltage level. These voltage fluctuations have to be considered to balance out the DC link voltages of all SMs (since in a modular topology, not all SMs will be active at once). A possible approach for balancing the stress for each SM is introduced in [12]. Further control schemes for SSSC can be found in [13, 17].

The amplitude of $\underline{U}_{inj}$ can be controlled, depending on the operation mode. For constant reactance operation, the output voltage is controlled in dependency of the line current, so that the required reactance is injected. For constant voltage mode, the output voltage is kept constant, independent of the current. For both operation modes, the voltage is kept within operational limits. Limits are also set by the minimum and maximum line current boundaries, I_{min} and I_{max}. These are visualised in Figure 19.

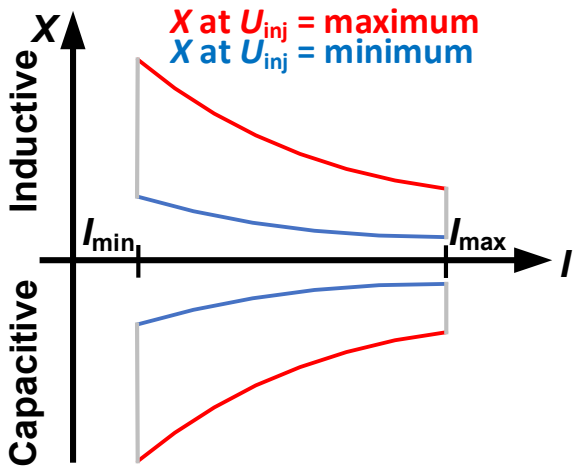


Figure 19: Operational diagram for a SSSC

In order to change the amplitude of $\underline{U}_{inj}$, the level of the DC link voltage needs to be adapted. This can be done by enabling an active power transfer, by choosing the reference angle a little off the ideal 90° phase shift, until the required voltage level is reached.

For ideal steady-state operation, the DC link voltages of all DC links can be assumed constant with an identical voltage level. The IGBTs of the SMs can then be controlled in such a way that the phasor of the fundamental of the injected voltage is perpendicular to the line current, while modulating the voltage waveform in such a way, that its Total Harmonic Distortion (THD) is minimal. In general, the THD decreases with the increasing number of submodules. More regarding the voltage output will be discussed in section 3.1.2.

Figure 20 shows the basic phasor diagram for the operation concept of SSSCs. Here, two voltage sources $\underline{U}_{1,A}$ and $\underline{U}_{1,B}$ are connected by a line impedance $\underline{Z}_{1,L}$ and a SSSC injecting the voltage $\underline{U}_{inj}$.

By the SSSC being capable of operating both capacitive ($-\underline{U}_{inj}$) and inductive ($+\underline{U}_{inj}$), different values for $\underline{Z}_{1,L}$ allow the same current to flow across the line.

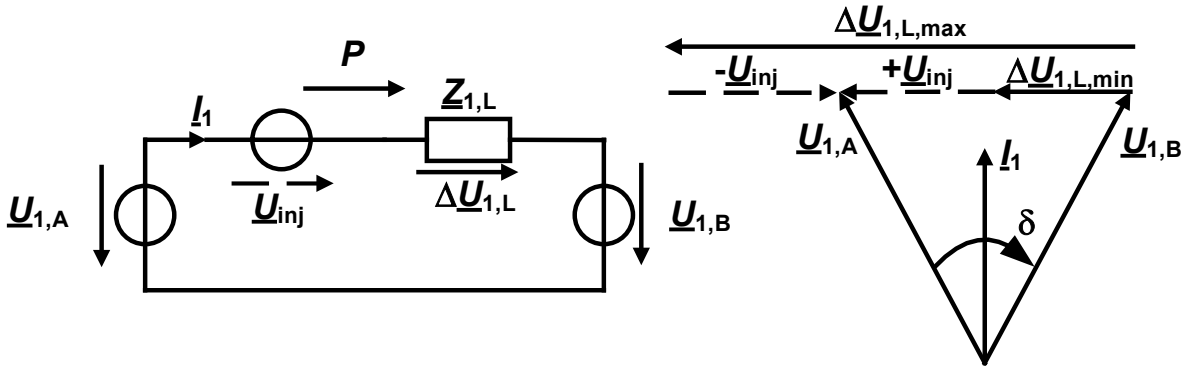


Figure 20: Phasor diagram for capacitive and inductive operation of a SSSC based on [9]

2.2.5 Unified Power Flow Controller (UPFC)

The UPFC is a combination of a STATCOM and a SSSC and is therefore both, a series and parallel FACTS device. It allows very flexible operation and can be used for several different applications. Its working principle is based on sections 2.2.2 and 2.2.4. It can be expanded due to the common DC link of this FACTS device. Its basic topology is illustrated in Figure 21. For further information regarding UPFCs, see [9].

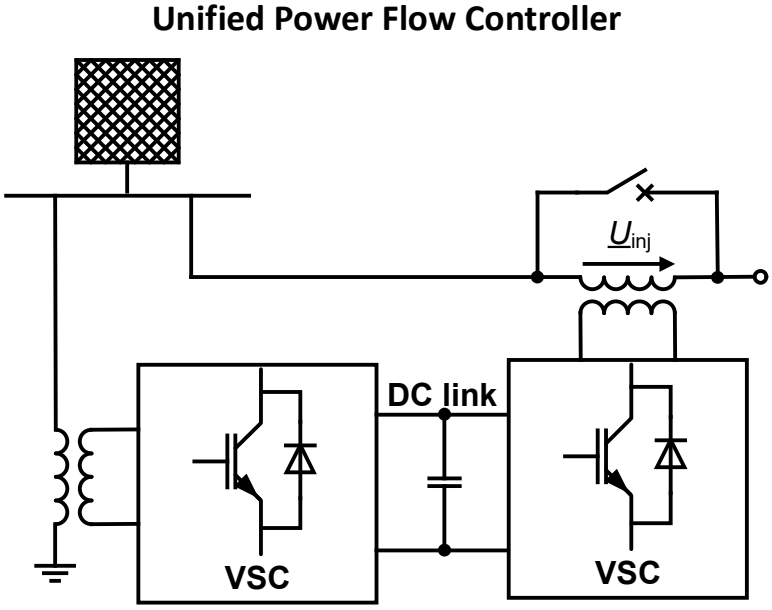


Figure 21: Unified Power Flow Controller (UPFC) based on [9]

2.3 Protection Schemes for Series-Compensated Lines

This section deals with preceding investigations regarding known effects that occur for compensated lines and practical and theoretical approaches for dealing with the influence of series compensation FACTS on distance protection. Additionally, the effects of voltage and current inversion are explained in the following sections.

2.3.1 Preceding Investigations regarding Lines operating with SSSCs

TCSCs and SSSCs can influence the measurement of distance protection relays. For TCSCs, an alternative approach for setting distance protection zones is proposed in [10]. Here, the major impact lies in the potential overreach caused by the capacitive operation mode. This challenge can be mitigated by using modified reactive zone settings according to the effective capacitance of the SSSC. Additionally, the overvoltage protection mechanisms (MOV and spark gap) influence the resistance of the fault loop impedance measured by distance protection relays. Therefore, modified resistive zone setting can improve the reliability of distance protection with TCSCs.

The main influence of SSSCs on distance protection is given by the impact of the SSSC on the measured voltage that is used by the distance protection relay for calculating the fault loop impedance. In contrast to TCSCs, this is due to the injected voltage of the SSSC (section 4.1). Depending on the operation mode (capacitive or inductive), over- and underreach can occur, leading to the possibility of unselective trips. In [14], a proposed method for dealing with the injected voltage of the SSSC is using adaptive parameter settings for the distance zones. By this, the influence of the SSSC is compensated due to adaptive zone settings, which depend on the operation mode of the SSSC. [15] proposes a solution for the influence of the SSSC by additionally considering the injected voltage for the fault loop impedance calculation. This demands an additional communication interface between the SSSC and the protection relays or voltage measurements.

Both, [14] and [15] did not consider a bypass of the SSSC during a fault event. This would be identical to faults with bypass failure. [16] and [17] deal with the impact of SmartWires Inc. m-SSSC on distance protection while considering both, faults with and without the activation of the SSSCs bypass. Here it is shown that the threshold for the activation of the bypass must be chosen delicately. For the m-SSSC, the threshold is based on an instantaneous current value. Based on [17], this threshold needs to be coordinated with the distance protection pickup threshold (for the *I* – pickup). It is additionally mentioned that in case of low-current short-circuits (high resistive faults), the internal protection of the m-SSSC can supplement the overcurrent criteria for the activation of the bypass. For ensuring reliable protection for the scenario of a bypass failure, it is recommended to adapt the reactive reach setting to mitigate the effect of unselective trips due to overreach [16]. The use of teleprotection schemes can also act as a solution for this. Regarding a functional fast-acting SCR bypass, it could be shown that this bypass ensures that the distance protection is not affected by SSSCs.

In this context, a research gap could be identified regarding the speed of the activation of the bypass. It will therefore be investigated in Protection Hardware In the Loop (ProtHIL) tests, how fast the bypass

must react to a short-circuit in order to not influence distance protection relays. The results of the ProtHIL tests are summarised in section 6.

2.3.2 Voltage- and Current Inversion

Voltage and current inversion can occur for the series compensation device operating in capacitive mode. In the following, the boundary conditions for these effects to occur are explained for a SSSC.

Voltage Inversion

The basic idea of voltage inversion is illustrated in Figure 22. A fault occurs at the end of Line2, with a relative fault distance *n,* calculated in (15)

$$n = \frac{n \cdot \underline{Z}_{\mathrm{Line2}}}{\underline{Z}_{\mathrm{Line2}}} = \frac{Fault\ distance\ in\ \mathrm{km}}{Length\ of\ line\ in\ \mathrm{km}} \tag{15}$$

The SSSC is operating in capacitive mode. For voltage inversion to occur, the following two criteria, (16) and (17), have to be fulfilled [3]. It can be seen in Figure 22 that the capacitive voltage of the SSSC leads to the inversion of the faulty voltage $\underline{U}_{\mathrm{Relay2}}$.

$$\left|\mathrm{Im}\{\underline{Z}_{\mathrm{Line1}} + n \cdot \underline{Z}_{\mathrm{Line2}}\}\right| > \left|\underline{X}_{\mathrm{SSSC}}\right| \tag{16}$$

$$\left|\mathrm{Im}\{n \cdot \underline{Z}_{\mathrm{Line2}}\}\right| < \left|\underline{X}_{\mathrm{SSSC}}\right| \tag{17}$$

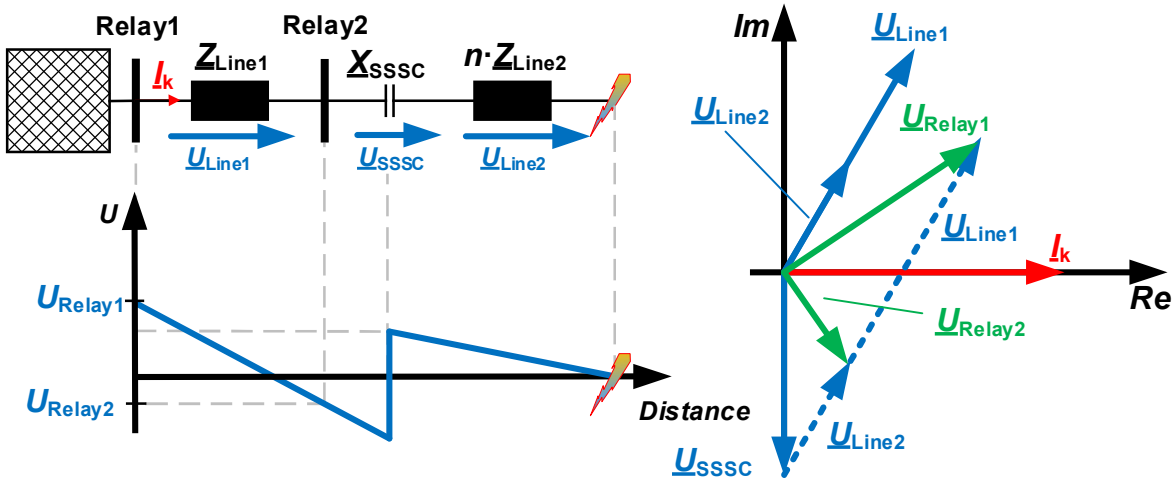


Figure 22: Voltage inversion based on [3,5]

During voltage inversion at Relay2, the phase relation between the faulty voltage $\underline{U}_{\mathrm{Relay2}}$ and the short-circuit current $\underline{I}_{\mathrm{k}}$ does not allow a reliable detection of the fault direction (measured impedance is in the fourth quadrant). Therefore, it is common practice to use unfaulted voltages or memorised voltages for the fault direction determination [5,7]. This effect is well known and typically occurs in case of series-compensated lines (e.g. TCSCs). As for the SSSC, as soon as the bypass of the SSSC is activated, the condition in (17) is not fulfilled anymore. A faster reacting bypass is therefore an improvement due to the fact that it shortens the time span voltage inversion can occur.

Current Inversion

Current inversion is an effect related to voltage inversion. A topology illustrating the functionality is shown in Figure 23. For this effect to occur, the SSSC must be operating in capacitive mode. If condition (18) is fulfilled, current inversion will occur.

$$\left|\mathrm{Im}\{\underline{Z}_{\mathrm{Line1}} + n \cdot \underline{Z}_{\mathrm{Line2}}\}\right| < \left|\underline{X}_{\mathrm{SSSC}}\right| \tag{18}$$

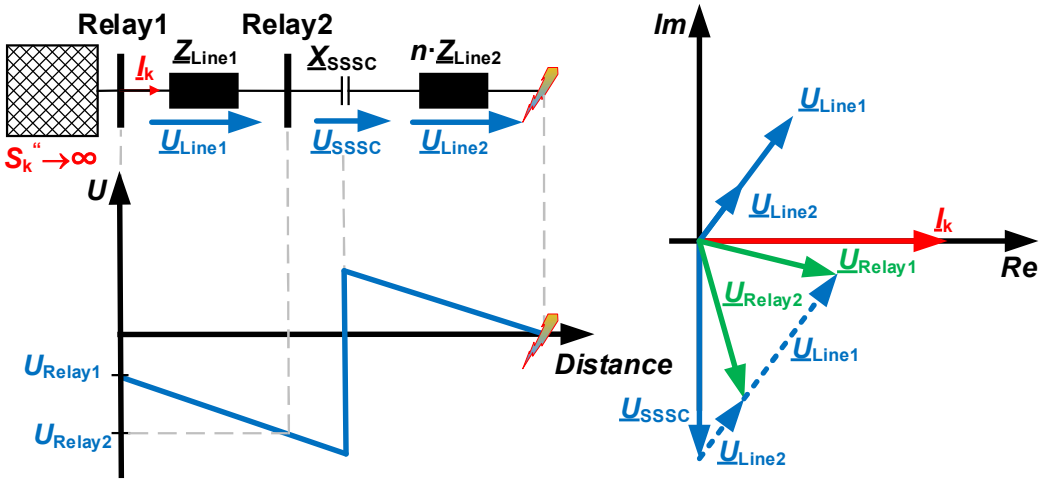


Figure 23: Current inversion based on [3,5]

Current inversion occurs as soon as the fault impedance from the feeding point of the grid to the fault point acts capacitive, leading to a capacitive fault current. This capacitive fault current leads to the absolute voltage increasing instead of decreasing along the lines Line1. For this case, the use of unfaulted voltages or memorised voltages does not aid in the correct determination of the fault direction, as the inverted current $\underline{I}_k$ will be leading a memorised or unfaulted voltage. The requirement for this effect in equation (18) is only fulfilled in very rare or special grid constellations, with the fault being directly at the terminal of the SSSC. With the activation of the bypass, condition (18) will not be fulfilled anymore.

3 Development of a SSSC Model

This chapter documents the development of a SSSC model for simulations in Matlab / Simulink. The modelling of the SSSC is limited to its relevant operational characteristics such as the injected voltage, operation mode (inductive or capacitive) or operational boundaries. The verification of the model is performed by investigating the model's behaviour during load operation and in case of short circuits. In addition to model verification, a controllable bypass delay is implemented, allowing to investigate the time dependency of the bypass on the reliability of distance protection devices.

The developed model will afterwards be used for offline simulations in Matlab / Simulink as well as for real-time simulation tests on a real-time simulator (RTS).

3.1.1 Topology

The topology for the model to be implemented is based on the m-SSSC as described in section 2.2.4. The realised m-SSSC has three SMs per phase with an overall rated maximum injected RMS of the fundamental U_{inj} = 1698 V. The rated current of the device is set with an RMS of 1800 A. For further investigations, even though the topology of the m-SSSC is used, only the term SSSC will be used as an abbreviation.

Each leg of the SSSC comprises three full-bridge SMs, as illustrated in Figure 24. The injected voltage u_{inj} is the sum of the voltages of each individual SM. This is illustrated in Figure 26. The converter design features a dedicated leg for each phase, resulting in electrically decoupled legs that can be analysed independently. For the real converter, the mean of each DC link voltage fluctuates in dependency of the phase shift between the line current *i* and the injected voltage of each SM. The use of full-bridges demands the implementation of a dedicated DC link voltage controller. Because the focus of this work is on the SSSC model functionality an ideal voltage controller is assumed, resulting in the use of controlled voltage sources instead of full-bridge SMs. This results in a constant DC link voltage which is chosen as described in 3.1.2. The DC link capacitor was still considered in order to simulate the hardware protection system of the SSSC, which would lead to a bypass activation due to over- or undervoltage in the DC-link. This is further described in sections 3.1.4 and 3.1.5.

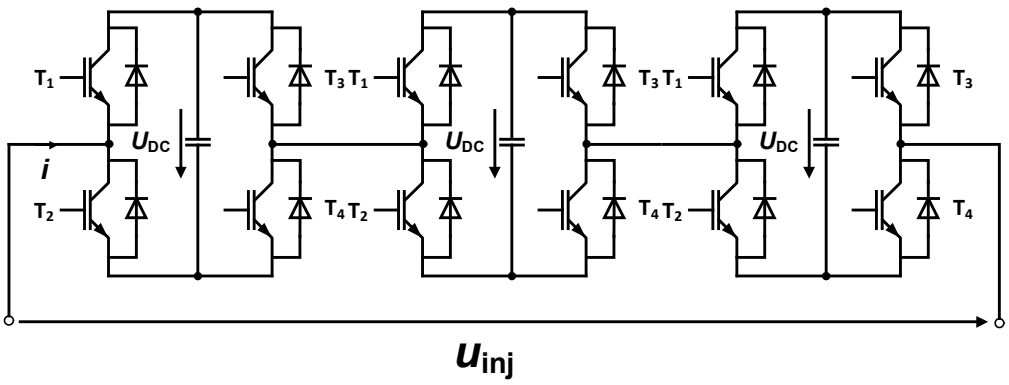


Figure 24: Three SMs for one leg of the SSSC (one phase)

3.1.2 Voltage Output

For the voltage output of each leg, only one instead of three controlled voltage sources will be used. The goal for the output voltage waveform is set as follows:

- The RMS of the injected rectangular-shaped voltage is set equal to the RMS of the fundamental of the reference voltage. The reference voltage is the ideal sinusoidal voltage waveform with an RMS of the fundamental $U_{inj,ref}$=1698 V, leading or lagging the line current by 90° (depending on operation mode).
- The THD of the resulting output voltage should be as small as possible for the number of SMs. For a larger number of SMs, the THD will decrease.

Regarding these requirements, a Matlab routine was designed in order to generate the injected voltage waveform by the SSSC. The following section documents the calculation of the height of the waveform, U_{DC} and the duration of turn-on, τ.

In a first step, the task was reduced to generating the voltage for a SSSC with just one SM. The result for this is shown in Figure 25. The reference RMS of the fundamental for this task was chosen with $U_{inj,ref}$ = 566 V. The first step of the routine is finding a solution for the optimal waveform of the rectangular-shaped signal by minimising the THD. The THD is calculated based on (19) with U_1 being the fundamental and U_n being harmonics of order n.

$$THD = \frac{\sqrt{\sum_{n=2}^{N} U_n{}^2}}{U_1} \tag{19}$$

The Matlab routine subsequently varies the pulse width τ_1 for the rectangular-shaped signal with [1:0.1:10] ms, and calculates its THD. The resolution for this interval was chosen with 100 µs due to the stimulation step of the subsequently used real-time simulator. Finally, the optimum solution for τ_1 is based on minimum value of the THD. For one SM, the optimal pulse width was calculated with τ_1 = 7.4 ms with an *THD* = 28.96 %.

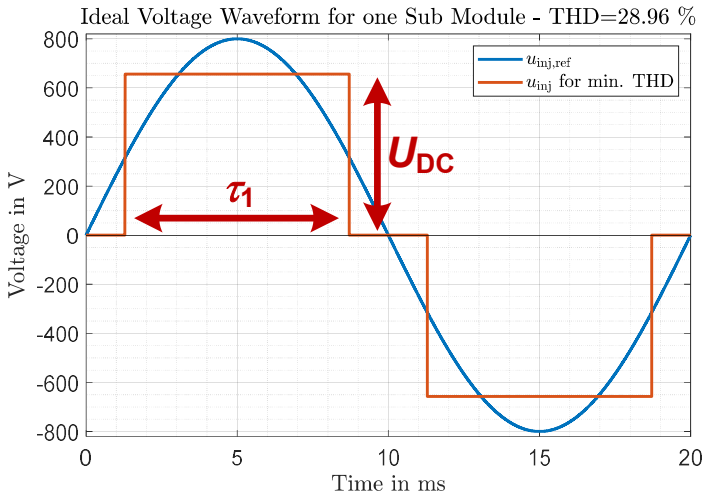


Figure 25: u_{inj} for one SM and minimum THD = 28.96 %

The absolute value of the rectangular-shaped signal, which would be equivalent to the mean value of the DC link voltage U_{DC} for generating an equivalent waveform, can be calculated by equation (20) by the RMS of a rectangular-shaped signal, $U_{inj,ref}$. This is done in the second step of the routine. With this successfully calculated, the task for a topology with one SM is fulfilled.

$$U_{DC} = \frac{U_{inj,ref}}{\sqrt{\frac{2 \cdot \tau_1}{T}}} = 657.96\ \text{V} \tag{20}$$

For the topology containing three SMs, the process for calculating the optimum pulse width is identical to the process of the single SM topology. The only difference is that three parameters, τ_1, τ_2 and τ_3, have to be calculated according to a minimal THD. Additionally, the RMS of the fundamental of the reference voltage signal is chosen with $U_{inj,ref}$ = 1698 V. The final waveform for the injected voltage while using three SMs is illustrated in Figure 26. This waveform results in a *THD* = 11.51 % with τ_1 = 9 ms, τ_2 = 7 ms and τ_3 =4.4 ms.

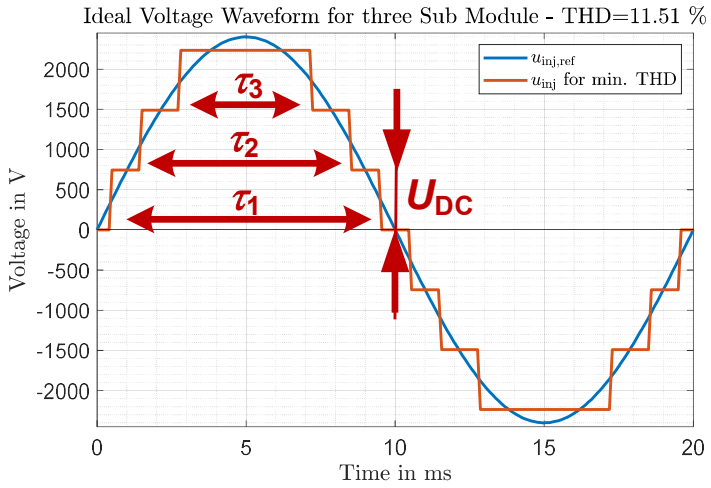


Figure 26: u_{inj} for three SMs and minimum THD = 11.51 %

The DC link voltage for a three SM topology, based on (20), can be calculated based on equation (21).

$$U_{DC} = \sqrt{\frac{{U_{inj,ref}}^2}{18 \cdot \frac{\tau_3}{T} + 8 \cdot \frac{\tau_2 - \tau_3}{T} + 2 \cdot \frac{\tau_1 - \tau_2}{T}}} = \sqrt{\frac{(1698\ \text{V})^2}{18 \cdot \frac{4.4\ \text{ms}}{20\ \text{ms}} + 8 \cdot \frac{2.6\ \text{ms}}{20\ \text{ms}} + 2 \cdot \frac{2\ \text{ms}}{20\ \text{ms}}}} = 744.21\ \text{V} \tag{21}$$

U_{DC} is calculated in dependency of $U_{inj,ref}$. The value for $U_{inj,ref}$ is chosen in dependency of the control mode. For const. *U* control, $U_{inj,ref}$ is chosen manually within operational boundaries. For const. *Z* control, the reference value for $U_{inj,ref}$ is chosen in dependency of the RMS of the measured line current. Both const. *U* and *Z* control were implemented, but only const. U was used. Its value was always chosen with the upper operational limits for obtaining the maximum impact by the SSSC.

Due to the better results achieved with the three SM topology, this topology was implemented Matlab / Simulink.

3.1.3 Synchronisation

The synchronisation process performed for each phase individually by a phase locked loop (PLL). For the following explanation, phase L1 will be considered. A flowchart for obtaining the reference angle of the current space vector of phase 1, θ_{L1}, is illustrated in Figure 27. Figure 28 visualises this process based on phasors. The instantaneous current i_{L1} is processed by a second-order generalised integrator (SOGI), which generates a second signal in addition to i_{L1}, which is 90° lagging the original signal. This results in the original signal, $i_{\beta,L1}$, and the lagging signal, $i_{\alpha,L1}$. Due to the constant frequency used in the simulation, also a fixed delay with 5 ms could have been used to generate the perpendicular signal. The perpendicular signal is mandatory, so that the dq-transform can be performed by the PLL.

The two signals $i_{\alpha,L1}$ and $i_{\beta,L1}$ can then be processed by the PLL. The PLL acquires the reference angle of the current space vector $\underline{i}_S = i_{\alpha,L1} + j \cdot i_{\alpha,L1}$. This is done by a PI controller with the parameters k_p and k_i. The output of the PLL controller is equal to the angular frequency of the grid and can additionally be added with a feed-forward signal, ω_{ff}. ω_{ff} is equal to the expected angular frequency of the grid. This reduces the time the PLL needs for locking to the correct angle. Finally, the signal is integrated and the modulo operator limits the value of the reference angle to $2 \cdot \pi$. With the angle of the current space vector acquired, the SSSC is controlled using a rotating reference frame with dq-components.

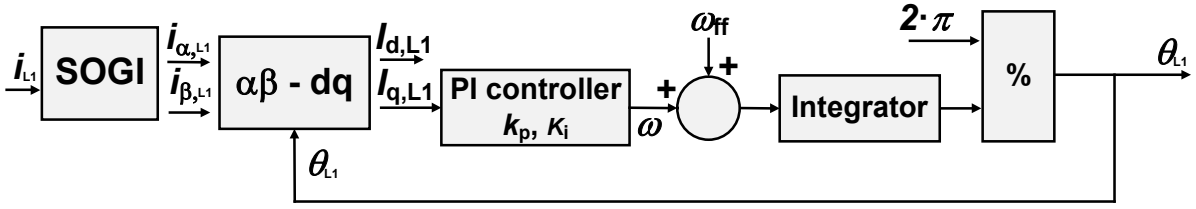


Figure 27: Flowchart for obtaining the reference angle θ_{L1}

It can be seen in Figure 28 that with the coordinate system locked to the current space vector, the phase of the injected voltage $\underline{U}_{inj,L1}$ is set relative to the d-axis. With $\underline{U}_{inj,L1}$ leading $\underline{I}_{d,L1}$ by 90°, the SSSC will operate inductive and for $\underline{U}_{inj,L1}$ lagging $\underline{I}_{d,L1}$ by 90°, the SSSC operates capacitive. This process is done simultaneously for each phase individually.

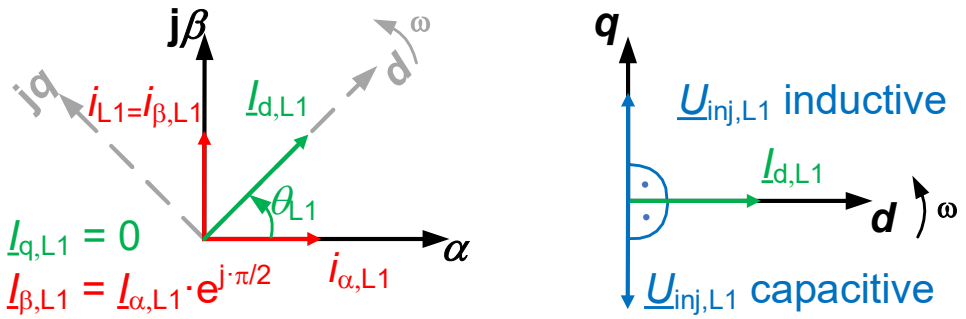


Figure 28: Phasor diagram for SOGI, PLL and rotating reference frame

3.1.4 Dimensioning the DC-link Capacitor

Even though the full bridge SMs are simplified to a controlled voltage source, a fictitious DC-link capacitor is dimensioned. This is needed to realise the voltage dependent DC link bypass control. The current of a capacitor i_C depends on the value of the capacitance C and u_C and can be calculated based on equation (22).

$$i_{\mathrm{C}} = C \cdot \frac{du_{\mathrm{C}}}{\mathrm{d}t} \tag{22}$$

Based on (22), equation (23) calculates the voltage of the capacitor.

$$u_{\mathrm{C}} = \frac{1}{C} \cdot \int i_{\mathrm{C}} \cdot \mathrm{d}t \tag{23}$$

During steady-state operation, the voltage of the capacity or has a ripple Δu_C that can be calculated based on equation (24).

$$\Delta u_C = \frac{1}{\mathrm{C}} \cdot \int_0^{\frac{\pi}{2}} i_{\mathrm{C}} \cdot \mathrm{d}t \tag{24}$$

For dimensioning the DC-link capacitor, it is chosen that the maximum ripple voltage $\Delta u_{C,max}$ for the maximum rated current of 1800 A is equal 10 % of the maximum DC-link voltage as calculated in equation (21). The capacitance of the DC-link capacitor is calculated in (25).

$$C = \frac{\hat{I}_{\mathrm{C}}}{\omega \cdot \Delta u_{\mathrm{C,max}}} = \frac{1800\ \mathrm{A} \cdot \sqrt{2}}{100 \cdot \pi\ \frac{1}{\mathrm{rad}} \cdot 74.4\ \mathrm{V}} = 108.9\ \mathrm{mF} \tag{25}$$

3.1.5 Automatic Bypass

The bypass of the SSSC is based on thyristors that activate during fault events. The automatic bypass can be triggered by two threshold values [11,16,17].

Instantaneous current threshold: In order to protect the SSSC from short-circuit currents, the device measures the instantaneous current of each converter leg. If one phase exceeds the threshold value I_{SC}, the bypass is activated. This can be done only in the faulty phase, or also for all phases. For this model, e.g. a line-to-ground fault will trigger the bypass in every phase. The threshold value needs to be chosen in dependency of the thermal current limit of the line and the pickup current value of the distance protection relay.

DC protection threshold: The energy stored in the fictitious capacitor is constantly monitored during fault events. For this, the lower voltage boundary U_{LB} and the upper voltage boundary U_{UB} for the DC-link voltage are defined. These are set based on the DC link voltage in equation (21), which depends on $U_{inj,ref}$.

$$75\ \% \cdot U_{\mathrm{DC}} = U_{\mathrm{LB}} \text{ and } 125\ \% \cdot U_{\mathrm{DC}} = U_{\mathrm{UB}} \tag{26}$$

Based on these voltage boundaries, a maximum energy intake or discharge of the DC link capacitors can be calculated, that would lead to exceeding the voltage limits based on equation (26).This is done in equation (27).

$$\Delta E_{\mathrm{LB}} = C \cdot \frac{{U_{\mathrm{LB}}}^2 - {U_{\mathrm{DC}}}^2}{2} \text{ and } \Delta E_{\mathrm{UB}} = C \cdot \frac{{U_{\mathrm{UB}}}^2 - {U_{\mathrm{DC}}}^2}{2} \tag{27}$$

As soon as a fault event occurs, the instantaneous power *p* of the SSSC leg is integrated in order to calculate the energy, *E,* that is absorbed by the three fictitious DC-link capacitors. This is shown in equation *(28*). The integration of the instantaneous current *i*, and the instantaneous injected voltage u_{inj}, starts with the short-circuit. Initial condition for *E* is set with *E*(0) = 0. The factor 1/3 compensates for the fact that the energy is distributed on three DC-link capacitors.

$$E = \frac{1}{3} \cdot \int p \cdot \mathrm{d}t = \frac{1}{3} \cdot \int i \cdot u_{\mathrm{inj}} \cdot \mathrm{d}t \tag{28}$$

Finally, the bypass condition for the DC protection can be summarised as shown in equation (29).

$$\text{Bypass activation due to DC protection threshold: } \Delta E_{\mathrm{LB}} \geq E \text{ and } \Delta E_{\mathrm{UB}} \leq E \tag{29}$$

This functionality is also implemented for each individual phase. The exceeding of these limits of any phase will trigger the bypass of all three phases.

Additionally to the automatic bypass, it is also possible to control the bypass manually. This is necessary for investigating the impact of the bypass delay on distance protection. Therefore, a bypass delay is set which is added to the time of the fault beginning.

3.1.6 Overview of the SSSC model

Figure 29 summarises and illustrates the functionality of the SSSC model.

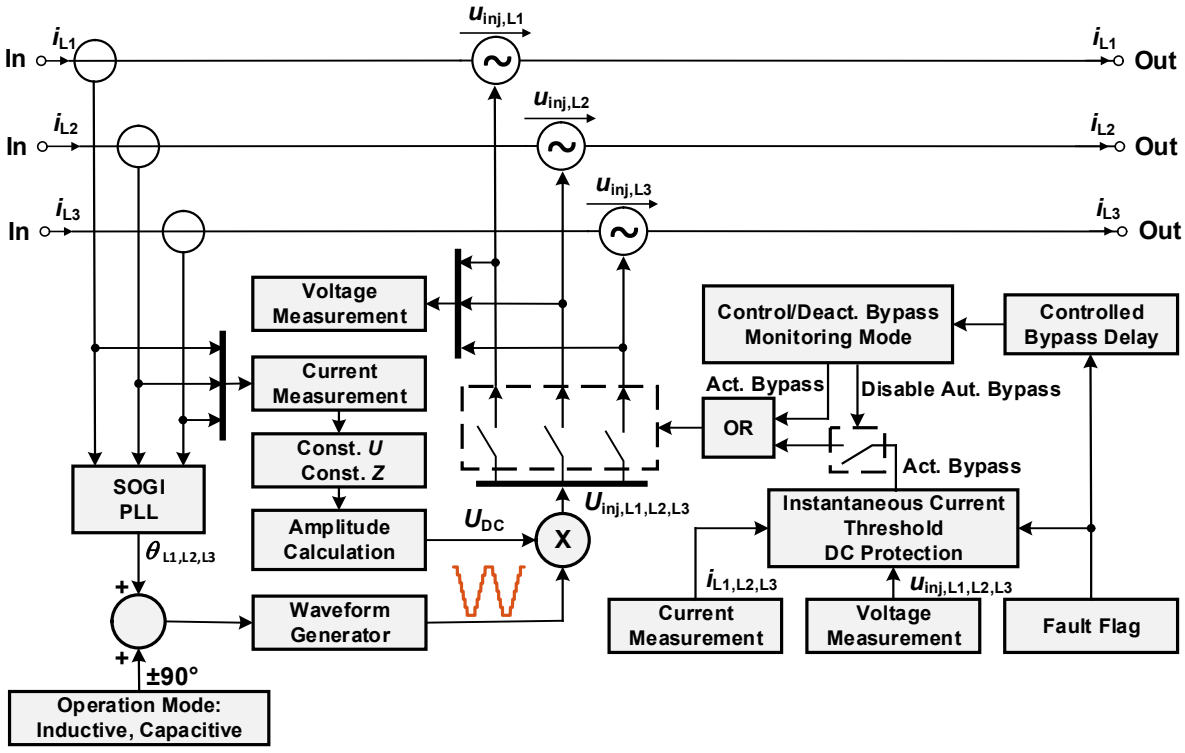


Figure 29: Topology of the SSSC model

3.1.7 Verification of the SSSC Model

For the verification process of the model, an offline simulation with Matlab / Simulink R2018b with the Simscape Specialized Power Systems Library was used. For the time-discrete solver, *Backward Euler* with a timestep of 100 µs was used.

Steady-State Operation with Inductive and Capacitive Mode

Figure 30 illustrates the instantaneous injected voltage $u_{inj,L1}$ and the corresponding current i_{L1} for inductive operation of the SSSC, Figure 31 shows identical quantities for capacitive operation. Both figures fulfil the expectancies for the phase relation of the current and the injected voltage, as well as the waveform of the injected voltage.

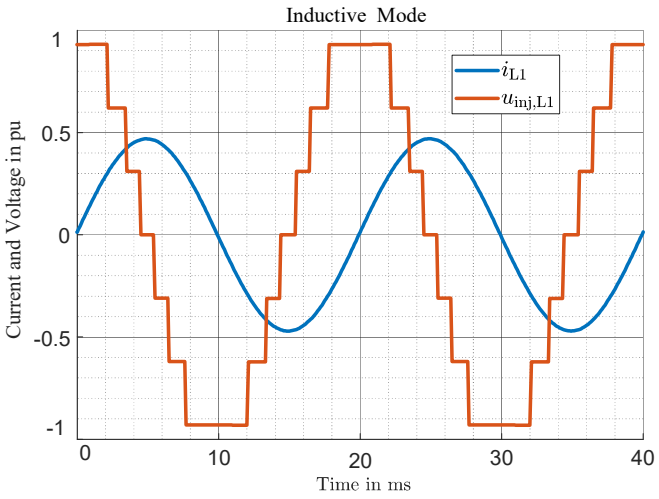


Figure 30: SSSC operating inductive

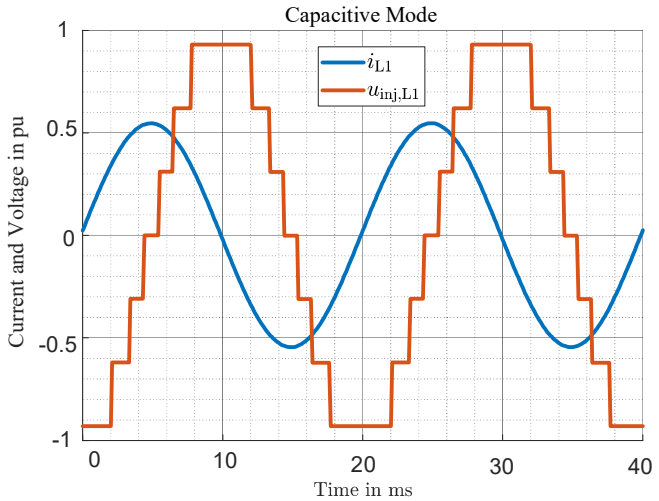


Figure 31: SSSC operating capacitive

Load Flow Simulation and Calculation

As a next verification step, the SSSC model is used for power flow simulations. Figure 32 illustrates the topology used for these simulations, which are verified by calculations based on (14). For the topology, two grids A and B were connected by a single line (losses neglected). Table 2 summarises the parameters used for simulation and calculation. Figure 33 shows the simulation results for the SSSC being used for controlling active power flow. The results of the calculation are summarised in Table 3. It can be seen that calculation and simulation lead to identical results, verifying the SSSC model for load flow simulation.

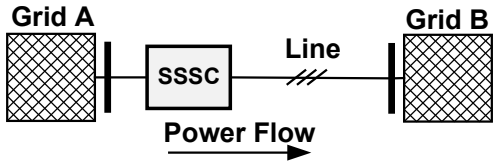


Figure 32: Topology for lossless power flow simulation and calculation

Table 2: Parameters of two grids A & B with phase shift δ, that are connected by a line with reactance X_{line} compensated by an SSSC

Grid and SSSC Parameter						
U_{GridA}	U_{GridB}	δ	U_{inj}	X_{line}	$X_{SSSC,ind}$	$X_{SSSC,cap}$
kV	kV	°	V	Ω	Ω	Ω
220	220	10	1698	56.18	4.4	-3.8

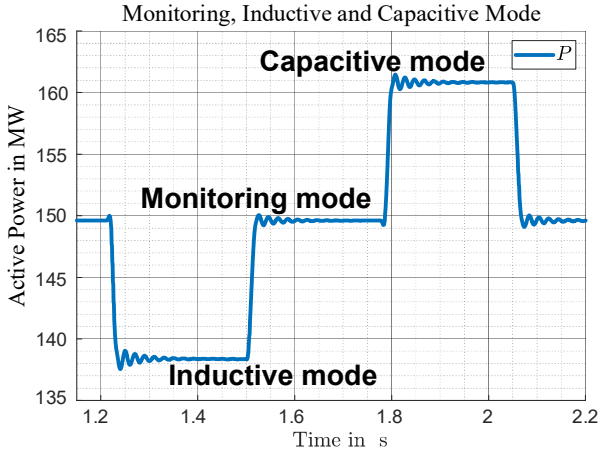


Figure 33: Load flow control by SSSC

Table 3: Results for calculated values of the load flow with the parameters of Table 2

Results for Steady-state load flow		
$P_{A\text{-}B,monitoring}$	$P_{A\text{-}B,inductive}$	$P_{A\text{-}B,capacitive}$
MW	MW	MW
149.6	138.7	160.4

Verification of the Bypass Mechanisms

For the verification of the bypass functionalities, a three-phase short-circuit was simulated and the response of the automatic bypass mechanisms was investigated. The instantaneous current threshold I_{SC} was chosen with 1.1 pu of the rated RMS current of the SSSC, the energy threshold was parametrised according to (27). Figure 34 illustrates the fault flag (start of the fault), the signal *SC* is equal to the bypass signal of the instantaneous current protection and *DC* is equal to the bypass signal of the DC protection mechanism. The overcurrent mechanism acted within 1.2 ms, the DC protection within 5.2 ms, relative to the fault start. For this test, the bypass was deactivated. Otherwise, the DC protection mechanism would not have been triggered because the bypass would already have been active due to the overcurrent protection. According to [16], the bypass triggers the SCR within 1 ms or less. Therefore, an additional delay is implemented, so that the SSSC is physically bypassed 1 ms after the bypass is activated. Regarding this additional delay, the automatic bypass would have therefore bypassed the SSSC within 2.2 ms.

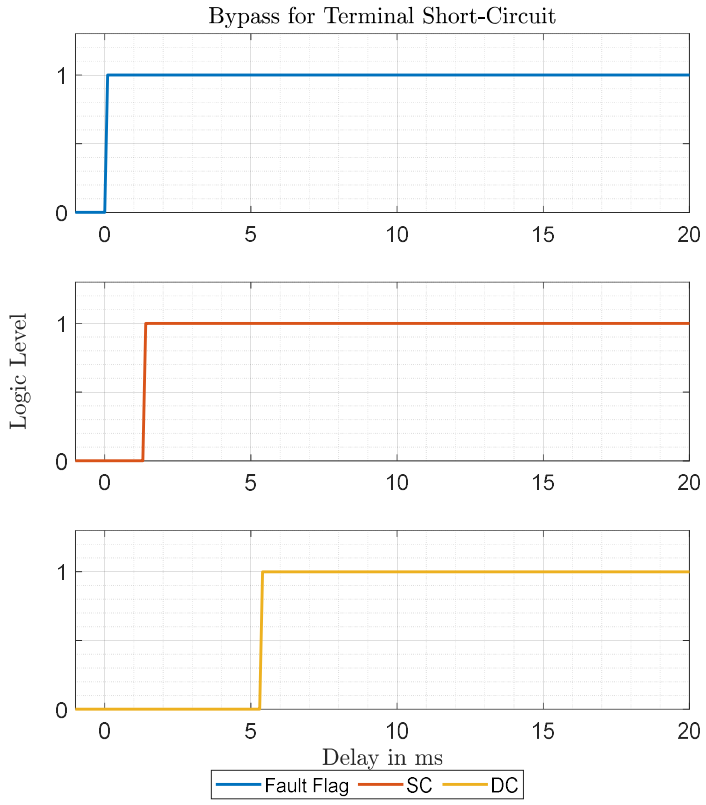


Figure 34: Response of the bypass to a three-phase short-circuit

Figure 35 illustrates the functionality of the instantaneous overcurrent bypass. The currents of the SSSC are set relative to $I_{SC.}$ It can be seen that as soon as the instantaneous current of phase L1 exceeds the threshold I_{SC}, the bypass is triggered by the instantaneous overcurrent mechanism.

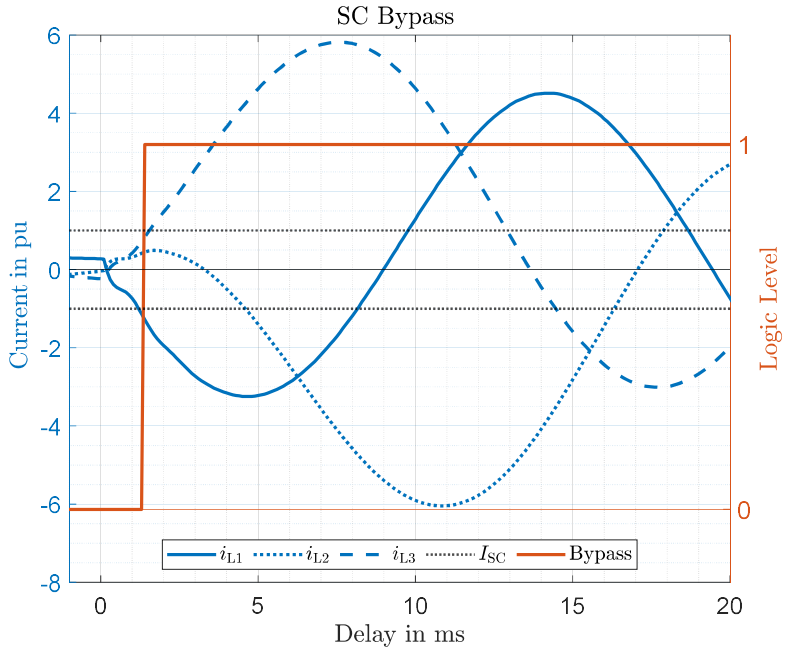


Figure 35: Instantaneous current protection for a three-phase short-circuit

Figure 36 illustrates the functionality of the DC protection bypass. The energy is calculated using the *cumtrapz* function of Matlab for each phase individually. The energy of each phase is plotted relative to ΔE_{LB}. It can be seen that, as soon as the energy of phase L1 exceeds the energy threshold, the bypass is triggered by the DC protection mechanism.

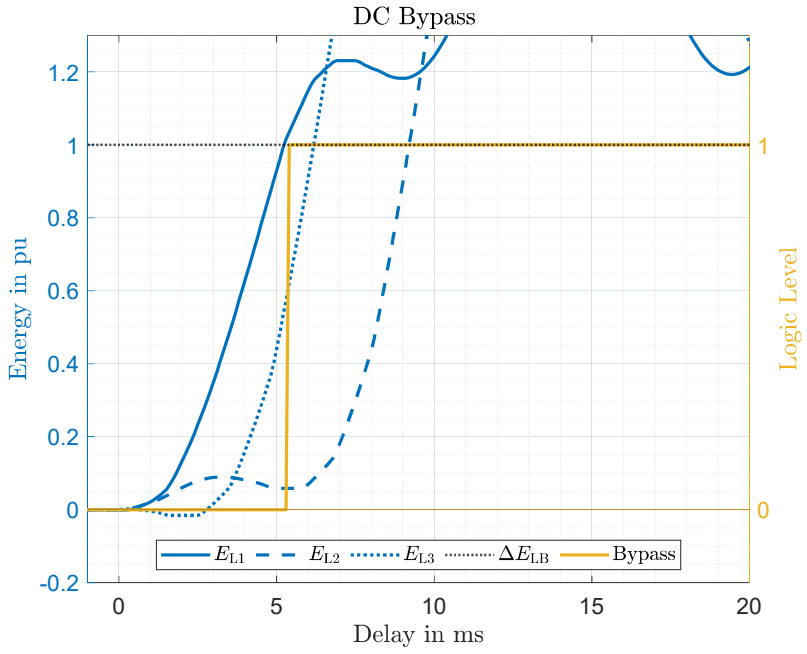


Figure 36: DC protection for a three-phase short-circuit

4 Investigation of the Influence of SSSCs on Distance Protection

4.1 Analytic Investigation of Four Different Topologies

The primary influence of SSSCs on distance protection devices and their reliable detection of faults is by its impact on the measured line reactance. SSSCs are equipped with a bypass, that activates in order to protect its power electronics. The activation of the bypass can occur when current thresholds are exceeded. High-impedance faults (e.g. a tree falling into a power line) as well as distant faults are possible scenarios where fault currents may not immediately lead to bypass activation. Another critical factor for accurately determining the fault distance is the time it takes for the bypass to activate after the fault begins.

In this context, this chapter aims to analyse network topologies and analytically determine the effects of an SSSC, while considering the scenario of a bypass failure. The investigation focuses on four different topologies. For each topology, the ideal three-phase short-circuit (without fault resistance R_f) as well as the one-phase short-circuit and the two-phase short-circuit without ground contact, considering fault resistance R_f and double feeding of the fault, will be examined. All further considerations of this chapter are based on a similar approach in [4].

4.1.1 Topology 1

Topology 1 is shown in Figure 37. Two grids are connected by Line1. The line is protected by two protection devices, Relay1A and Relay3. On the side of Relay1A, a SSSC in series to the line.

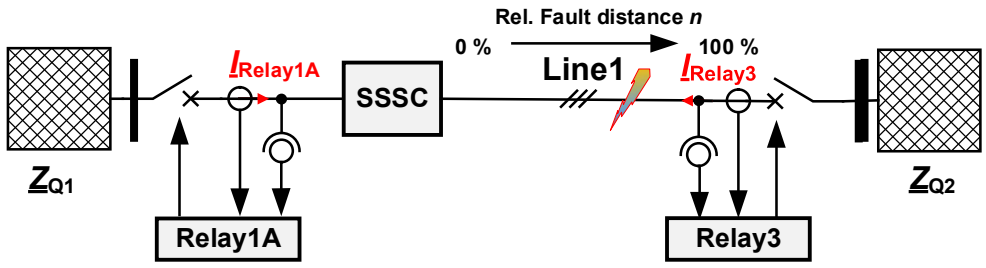


Figure 37: Topology 1

Three-Phase Fault with neglected Fault Resistance R_f

The three-phase fault without fault resistance R_f represents an idealised and simplified view of a symmetrical short circuit. Figure 38 illustrates an equivalent circuit diagram for this fault when considering the fault loop L1-L2.

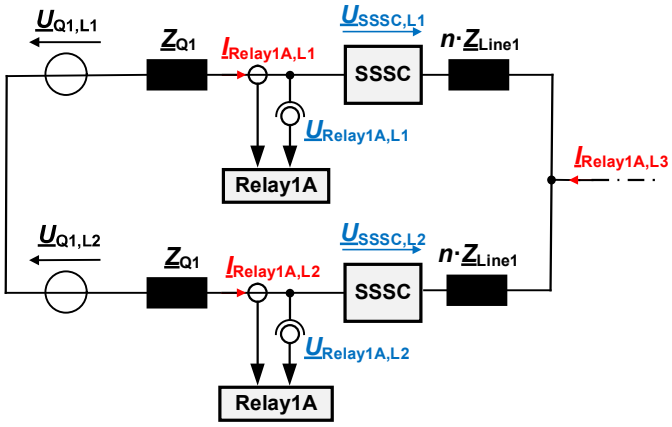


Figure 38: Equivalent circuit L1-L2 of a three-phase fault (L1-L2-L3), based on Figure 37 while neglecting the fault resistance R_f

For a symmetrical three phase fault, following relationship for the phase currents holds.

$$\underline{I}_{\text{Relay1A,L1}} = \underline{a} \cdot \underline{I}_{\text{Relay1A,L2}} = \underline{a}^2 \cdot \underline{I}_{\text{Relay1A,L3}} \text{ or } \underline{I}_{\text{Relay1A,L1}} + \underline{I}_{\text{Relay1A,L2}} + \underline{I}_{\text{Relay1A,L3}} = 0 \quad (30)$$

Based on the operating principle of the SSSC, equation (31*)* holds for the idealized behaviour of the injected SSSC voltages.

$$\underline{U}_{\text{SSSC,L1}} = \underline{a} \cdot \underline{U}_{\text{SSSC,L2}} = \underline{a}^2 \cdot \underline{U}_{\text{SSSC,L3}} \text{ or } \underline{U}_{\text{SSSC,L1}} + \underline{U}_{\text{SSSC,L2}} + \underline{U}_{\text{SSSC,L3}} = 0 \quad (31)$$

The voltage equation from the perspective of Relay1A can be formulated according to Figure 38 as follows. The factor *n* represents the relative fault distance (see *(15)*), based on the length of Line1.

$$\begin{aligned} \underline{U}_{\text{Relay1A,L1-L2}} &= \underline{U}_{\text{Relay1A,L1}} - \underline{U}_{\text{Relay1A,L2}} = \\ &= \underline{U}_{\text{SSSC,L1}} + \underline{I}_{\text{Relay1A,L1}} \cdot n \cdot \underline{Z}_{\text{Line1}} - \underline{I}_{\text{Relay1A,L2}} \cdot n \cdot \underline{Z}_{\text{Line1}} - \underline{U}_{\text{SSSC,L2}} \end{aligned} \quad (32)$$

The line-to-line fault loop impedance can be calculated as follows in (33).

$$\underline{Z}_{\text{Relay1A,L1-L2}} = \frac{\underline{U}_{\text{Relay1A,L1}} - \underline{U}_{\text{Relay1A,L2}}}{\underline{I}_{\text{Relay1A,L1}} - \underline{I}_{\text{Relay1A,L2}}} \quad (33)$$

Taking into account equations (30), (31), (32), and (33), the loop impedance of the L1-L2 loop can be calculated according to equation (34).

$$\underline{Z}_{\text{Relay1A,L1-L2}} = n \cdot \underline{Z}_{\text{Line1}} + \frac{\underline{U}_{\text{SSSC,L1}}}{\underline{I}_{\text{Relay1A,L1}}} \text{ or } \underline{Z}_{\text{Relay1A,L1-L2}} = n \cdot \underline{Z}_{\text{Line1}} + \frac{\underline{U}_{\text{SSSC,L2}}}{\underline{I}_{\text{Relay1A,L2}}} \quad (34)$$

It can be seen in equation (34) that the SSSC affects the measurable impedance from Relay1A's perspective. Assuming a phase shift of ± 90° between $\underline{U}_{\text{SSSC,L1}}$ and $\underline{U}_{\text{SSSC,L2}}$, and $\underline{I}_{\text{Relay1A,L1}}$ and $\underline{I}_{\text{Relay1A,L2}}$ the SSSC thus exclusively influences the measurable reactance. Depending on the operating point, it contributes to an increase (inductive) or a decrease (capacitive) of $\underline{Z}_{\text{Relay1A,L1-L2}}$.

Line-to-Ground Fault with Fault Resistance R_f and Double Feeding

Based on the outlined topology, the following equivalent circuit diagram in Figure 39 can be created for a line-to-ground fault. This represents a double-fed fault with fault resistance R_f .The specific faulty phase is not relevant for the following considerations.

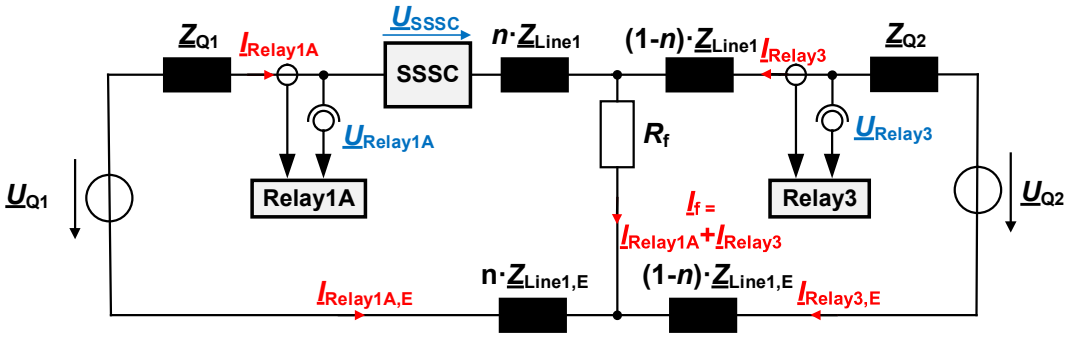


Figure 39: Equivalent circuit L-G of a one-phase fault (L-G), based on Figure 37 while considering the fault resistance R_f and double infeed

Following the impedance for the L-G fault is derived. This approach can be directly adopted for the following topologies. In a first step, the loop equation for Relay1A can be set up as following in (35). *n* again represents the relative location of the fault along the line.

$$\underline{U}_{\mathrm{Relay1A}} = \underline{I}_{\mathrm{Relay1A}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} - \underline{Z}_{\mathrm{Line1,E}} \cdot n \cdot \underline{I}_{\mathrm{Relay1A,E}} + \left(\underline{I}_{\mathrm{Relay1A}} + \underline{I}_{\mathrm{Relay3}}\right) \cdot R_{\mathrm{f}} + \underline{U}_{\mathrm{SSSC}} \tag{35}$$

By highlighting the term $\underline{I}_{\mathrm{Relay1A}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}}$, the voltage equation can be rewritten as formulated in (36).

$$\underline{U}_{\mathrm{Relay1A}} = \underline{I}_{\mathrm{Relay1A}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} \cdot \left(1 - \frac{\underline{Z}_{\mathrm{Line1,E}} \cdot \underline{I}_{\mathrm{Relay1A,E}}}{\underline{Z}_{\mathrm{Line1}} \cdot \underline{I}_{\mathrm{Relay1A}}}\right) + \left(\underline{I}_{\mathrm{Relay1A}} + \underline{I}_{\mathrm{Relay3}}\right) \cdot R_{\mathrm{f}} + \underline{U}_{\mathrm{SSSC}} \tag{36}$$

According to equation (6), the loop impedance for a line-to-ground fault can be calculated as shown in equation (37).

$$\underline{Z}_{\mathrm{Relay1A}} = \frac{\underline{I}_{\mathrm{Relay1A}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} \cdot \left(1 - \frac{\underline{Z}_{\mathrm{Line1,E}} \cdot \underline{I}_{\mathrm{Relay1A,E}}}{\underline{Z}_{\mathrm{Line1}} \cdot \underline{I}_{\mathrm{Relay1A}}}\right) + \left(\underline{I}_{\mathrm{Relay1A}} + \underline{I}_{\mathrm{Relay3}}\right) \cdot R_{\mathrm{f}} + \underline{U}_{\mathrm{SSSC}}}{\underline{I}_{\mathrm{Relay1A}} \cdot \left(1 - \underline{k}_{\mathrm{E}} \cdot \frac{\underline{I}_{\mathrm{Relay1A,E}}}{\underline{I}_{\mathrm{Relay1A}}}\right)} \tag{37}$$

With the simplification $\underline{I}_{\mathrm{Relay1}} = -\underline{I}_{\mathrm{Relay1,E}}$ (only one grounded neutral point) and using the definition of the ground factor $\underline{k}_{\mathrm{E}}$ according to equation (5), the loop impedance $\underline{Z}_{\mathrm{Relay1A}}$ can be expressed as shown in equation (38). Even though the simplification $\underline{I}_{\mathrm{Relay1}} = -\underline{I}_{\mathrm{Relay1,E}}$ does not reflect on boundary conditions in the field, it decisively simplifies (38), which is why this simplification was used.

$$\underline{Z}_{\mathrm{Relay1A}} = n \cdot \underline{Z}_{\mathrm{Line1}} + \frac{R_{\mathrm{f}}}{1 + \underline{k}_{\mathrm{E}}} + \frac{\frac{\underline{I}_{\mathrm{Relay3}}}{\underline{I}_{\mathrm{Relay1A}}} \cdot R_{\mathrm{f}}}{1 + \underline{k}_{\mathrm{E}}} + \frac{\underline{U}_{\mathrm{SSSC}}}{\underline{I}_{\mathrm{Relay1A}} \cdot (1 + \underline{k}_{\mathrm{E}})} \tag{38}$$

The loop impedance consists of four terms. The first term contains the actual distance information of the short circuit. The second and third terms result from considering a fault resistance R_f. The fourth term is caused by the injected voltage of the SSSC.

From the perspective of Relay3, the following voltage equation can be formulated according to equation (39).

$$\underline{U}_{\mathrm{Relay3}} = \underline{I}_{\mathrm{Relay3}} \cdot (1-n) \cdot \underline{Z}_{\mathrm{Line1}} \cdot \left(1 - \frac{\underline{Z}_{\mathrm{Line1,E}} \cdot \underline{I}_{\mathrm{Relay3,E}}}{\underline{Z}_{\mathrm{Line1}} \cdot \underline{I}_{\mathrm{Relay3}}}\right) + \left(\underline{I}_{\mathrm{Relay1A}} + \underline{I}_{\mathrm{Relay3}}\right) \cdot R_{\mathrm{f}} \tag{39}$$

In contrast to equation (36), it is clearly evident that the SSSC has no direct influence on the voltage equation of Relay2. The loop impedance from the perspective of Relay3 is then determined by (40), resulting in the following term with the previously made simplifications.

$$\underline{Z}_{\mathrm{Relay3}} = (1-n) \cdot \underline{Z}_{\mathrm{Line1}} + \frac{R_{\mathrm{f}}}{1+\underline{k}_{\mathrm{E}}} + \frac{\frac{\underline{I}_{\mathrm{Relay1A}}}{\underline{I}_{\mathrm{Relay3}}} \cdot R_{\mathrm{f}}}{1+\underline{k}_{\mathrm{E}}} \tag{40}$$

At Relay1A und Relay3, per equations (38) and (40), $\underline{Z}_{\mathrm{Relay1A}}$ and $\underline{Z}_{\mathrm{Relay3}}$ are distorted due to the consideration of the fault resistance R_{f}. This distortion depends on the argument of $\underline{k}_{\mathrm{E}}$, $\underline{I}_{\mathrm{Relay1A}}$ and $\underline{I}_{\mathrm{Relay3}}$ and affect both the real and imaginary parts of the determined impedances.

For $\underline{Z}_{\mathrm{Relay1A}}$, the voltage $\underline{U}_{\mathrm{SSSC}}$ causes an additional manipulation of the loop impedance. With an ideal phase relation of ±90 ° of $\underline{U}_{\mathrm{SSSC}}$ and $\underline{I}_{\mathrm{Relay1A}}$, the effect on the measured reactance depends on the argument of $\underline{k}_{\mathrm{E}}$. For rather small arguments of $\underline{k}_{\mathrm{E}}$, $\underline{U}_{\mathrm{SSSC}}$ mainly effects the loop reactance.

Line-to-Line Fault with Fault Resistance R_{f} and Double Infeed

For the two-phase fault in Scenario 1, the fault loop L1-L2 is examined. An equivalent circuit diagram for this is shown in Figure 40.

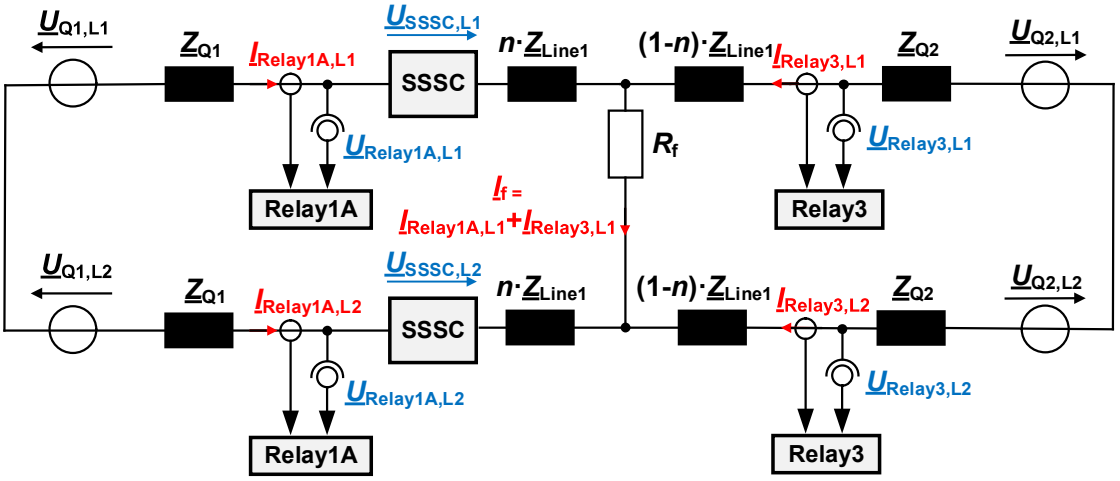


Figure 40: Equivalent circuit L1-L2 of a two-phase fault (L-L), based on Figure 37 while considering the fault resistance R_{f} and double infeed

Following the impedance for a L-L fault will be calculated. This approach can be adapted for the following topologies as well. Based on the equivalent circuit diagram, the voltage equation from the perspective of Relay1A can be formulated as shown in equation (41).

$$\begin{aligned} \underline{U}_{\mathrm{Relay1A,L1-L2}} &= \underline{U}_{\mathrm{Relay1A,L1}} - \underline{U}_{\mathrm{Relay1A,L2}} = \\ &= \underline{U}_{\mathrm{SSSC,L1}} + \underline{I}_{\mathrm{Relay1A,L1}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} + R_{\mathrm{f}} \cdot \left(\underline{I}_{\mathrm{Relay1A,L1}} + \underline{I}_{\mathrm{Relay3,L1}}\right) - \underline{I}_{\mathrm{Relay1A,L2}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} - \underline{U}_{\mathrm{SSSC,L2}} \end{aligned} \tag{41}$$

To evaluate the impedance of the loop L1-L2, calculation rule (33) is applied, where for a two-phase fault without ground contact, $\underline{I}_{\text{Relay1A,L2}} = -\underline{I}_{\text{RelayA1,L1}}$ holds. Therefore, the following calculation rule (42) applies based on equations (33) and (41).

$$\begin{aligned} \underline{Z}_{\text{Relay1A,L1-L2}} &= \frac{\underline{U}_{\text{Relay1A,L1}} - \underline{U}_{\text{Relay1A,L2}}}{\underline{I}_{\text{Relay1A,L1}} - \underline{I}_{\text{Relay1A,L2}}} = \\ &= \frac{\left(\underline{I}_{\text{Relay1A,L1}} - \underline{I}_{\text{Relay1A,L2}}\right) \cdot n \cdot \underline{Z}_{\text{Line1}} + \underline{U}_{\text{SSSC,L1}} - \underline{U}_{\text{SSSC,L2}} + R_{\text{f}} \cdot \left(\underline{I}_{\text{Relay1A,L1}} + \underline{I}_{\text{Relay3,L1}}\right)}{\underline{I}_{\text{Relay1A,L1}} - \underline{I}_{\text{Relay1A,L2}}} = \\ &= n \cdot \underline{Z}_{\text{Line1}} + \frac{\underline{U}_{\text{SSSC,L1}} - \underline{U}_{\text{SSSC,L2}}}{2 \cdot \underline{I}_{\text{Relay1A,L1}}} + \frac{R_{\text{f}}}{2} \cdot \left(1 + \frac{\underline{I}_{\text{Relay3,L1}}}{\underline{I}_{\text{Relay1A,L1}}}\right) \end{aligned} \tag{42}$$

Ideally, due to the condition $\underline{I}_{\text{Relay1A,L2}} = -\underline{I}_{\text{RelayA1,L1}}$, it follows that $\underline{U}_{\text{SSSC,L2}} = -\underline{U}_{\text{SSSC,L1}}$. This ultimately results in equation (43).

$$\underline{Z}_{\text{Relay1A,L1-L2}} = n \cdot \underline{Z}_{\text{Line1}} + \frac{\underline{U}_{\text{SSSC,L1}}}{\underline{I}_{\text{Relay1A,L1}}} + \frac{R_{\text{f}}}{2} \cdot \left(1 + \frac{\underline{I}_{\text{Relay3,L1}}}{\underline{I}_{\text{Relay1A,L1}}}\right) \tag{43}$$

From equation (43), a dependency of the measured impedance on the fault resistance, the double infeed, and the SSSC can once again be observed.

4.1.2 Topology 2

The topology for Scenario 2 is shown in Figure 41. Based on Scenario 1, an additional protection device, Relay1B, is included in Scenario 2. The influence of the SSSC on this protection device, Relay1B, will be examined. In this topology, it is also possible to implement a differential protection system using Relay1A and Relay1B for the SSSC, providing additional protection for the equipment.

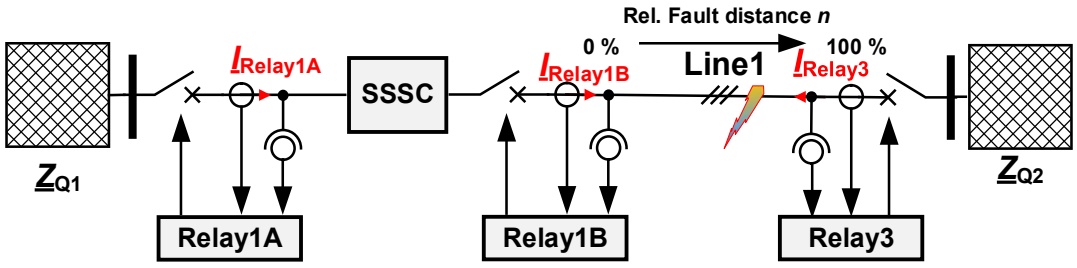


Figure 41: Topology 2

Three-Phase Fault with neglected the Fault Resistance R_f

Figure 42 graphically depicts the fault loop for a three-phase fault for topology 2. For this symmetrical fault, the simplifications from equations (30) and (31) can again be assumed. For the protection device Relay1A, the results from the preliminary analysis in chapter 4.1.1 can be directly applied. The following section will examine the influence of the SSSC on the device Relay1B.

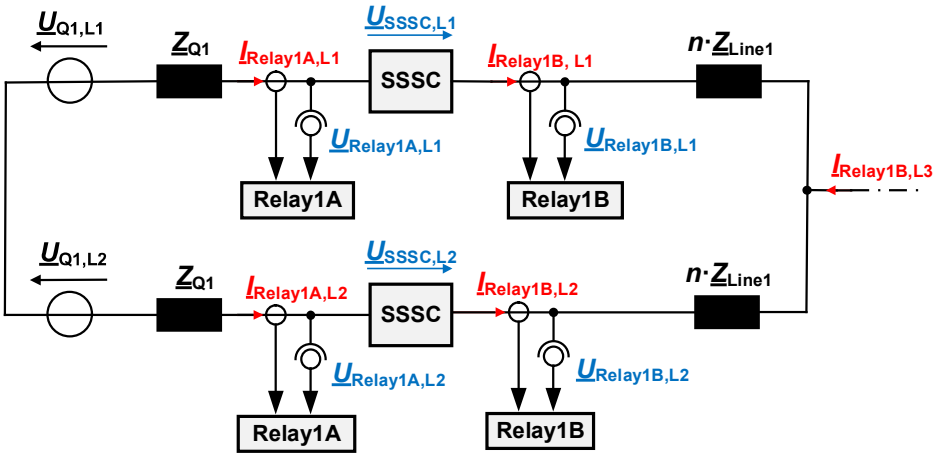


Figure 42: Equivalent circuit L1-L2 of a three-phase fault (L1-L2-L3), based on Figure 41 while neglecting the fault resistance R_f

For the device Relay1B, the following voltage equation is obtained according to Figure 42.

$$\underline{U}_{\text{Relay1B,L1}} - \underline{U}_{\text{Relay1B,L2}} = \underline{I}_{\text{Relay1B,L1}} \cdot n \cdot \underline{Z}_{\text{Line1}} - \underline{I}_{\text{Relay1B,L2}} \cdot n \cdot \underline{Z}_{\text{Line1}} \tag{44}$$

According to calculation rule (33), the following term for the loop impedance L1-L2 for Relay1B is obtained.

$$\underline{Z}_{\text{Relay1B,L1-L2}} = n \cdot \underline{Z}_{\text{Line1}} \tag{45}$$

From equation (45), it follows that, under ideal and symmetrical conditions in topology 2, the protection device Relay1B is not directly influenced by the SSSC when determining the fault loop impedance L1-L2.

Line-to-Ground Fault with Fault Resistance R_f and Double Infeed

Figure 43 graphically represents the equivalent circuit diagram for topology 2 in the case of a single-phase fault with double feeding, considering the fault resistance R_f.

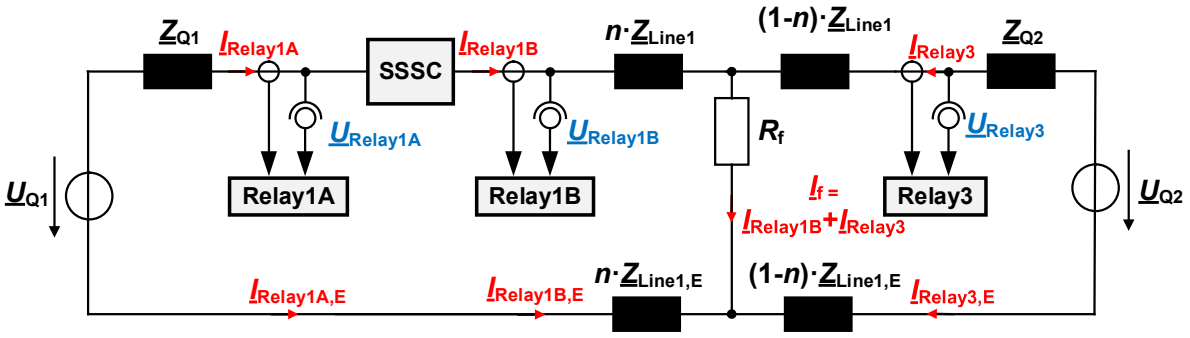


Figure 43: Equivalent circuit L-G of a one-phase fault (L-G), based on Figure 41 while considering the fault resistance R_f and double infeed

The impedance calculations from the perspective of Relay1A and Relay3 for this topology can be referenced from chapter 4.1.1. For the relay Relay1B, the following calculation rule (46) is derived for the voltage equation according to Figure 43 and the calculation steps in section 4.1.1.

$$\underline{U}_{\mathrm{Relay1B}} = \underline{I}_{\mathrm{Relay1B}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} \cdot \left(1 - \frac{\underline{Z}_{\mathrm{Line1,E}} \cdot \underline{I}_{\mathrm{Relay1B,E}}}{\underline{Z}_{\mathrm{Line1}} \cdot \underline{I}_{\mathrm{Relay1B}}}\right) + \left(\underline{I}_{\mathrm{Relay1B}} + \underline{I}_{\mathrm{Relay3}}\right) \cdot R_{\mathrm{f}} \tag{46}$$

When equation (6) is applied to equation (46), the impedance from the perspective of Relay1B in topology 2 is obtained, as shown in equation (47).

$$\underline{Z}_{\mathrm{Relay1B}} = n \cdot \underline{Z}_{\mathrm{Line1}} + \frac{R_{\mathrm{f}}}{1 + \underline{k}_{\mathrm{E}}} + \frac{\frac{\underline{I}_{\mathrm{Relay3}}}{\underline{I}_{\mathrm{Relay1B}}} \cdot R_{\mathrm{f}}}{1 + \underline{k}_{\mathrm{E}}} \tag{47}$$

Equation (47) clearly shows that positioning the protection device Relay1B after the SSSC proves advantageous for determining the loop impedance. Since the SSSC is not included in the fault loop, direct interference with the impedance calculation is thus avoided.

Line-to-Line Fault with Fault Resistance R_f and Double Infeed

Figure 44 presents the equivalent circuit diagram for the two-phase fault in Scenario 2. The results for the devices Relay1A and Relay3 can again be referenced from chapter 4.1.1. The following section analyses the effects of the SSSC on the device Relay1B during a two-phase fault.

The voltage equation for the device Relay1B is derived according to the following calculation rule.

$$\begin{aligned} \underline{U}_{\mathrm{Relay1A,L1-L2}} &= \underline{U}_{\mathrm{Relay1A,L1}} - \underline{U}_{\mathrm{Relay1A,L2}} = \\ &= \underline{I}_{\mathrm{Relay1A,L1}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} + R_{\mathrm{f}} \cdot \left(\underline{I}_{\mathrm{Relay1B,L1}} + \underline{I}_{\mathrm{Relay3,L1}}\right) - \underline{I}_{\mathrm{Relay1A,L2}} \cdot n \cdot \underline{Z}_{\mathrm{Line1}} \end{aligned} \tag{48}$$

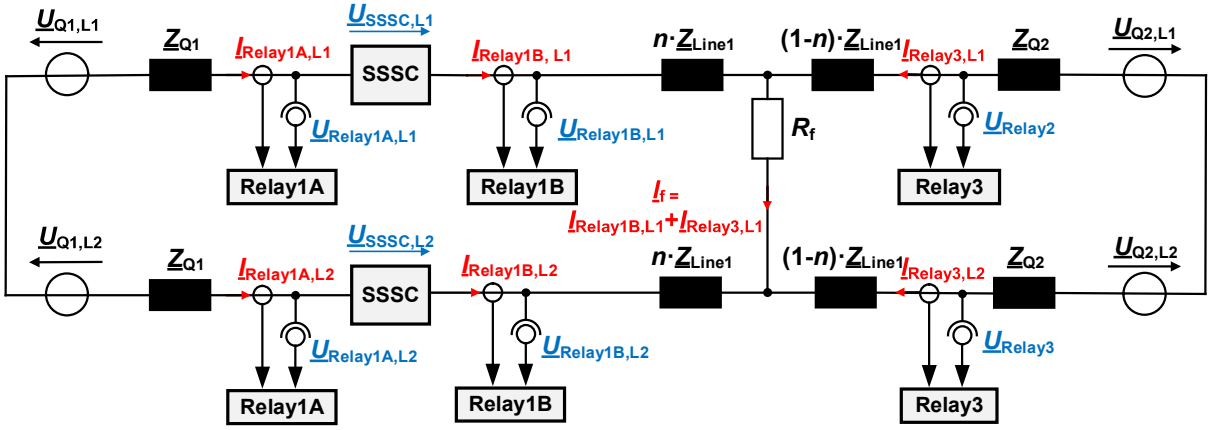


Figure 44: Equivalent circuit L1-L2 of a two-phase fault (L-L), based on Figure 41 while considering the fault resistance R_f and double infeed

Following the same procedure for forming the loop impedance as in equation (42), the loop impedance L1-L2 for the device Relay1B in the two-phase fault case can be calculated as follows (see 4.1.1 for more detailed calculation steps).

$$\underline{Z}_{\mathrm{Relay1A,L1-L2}} = n \cdot \underline{Z}_{\mathrm{Line1}} + \frac{R_{\mathrm{f}}}{2} \cdot \left(1 + \frac{\underline{I}_{\mathrm{Relay3,L1}}}{\underline{I}_{\mathrm{Relay1A,L1}}}\right) \tag{49}$$

This demonstrates that, even in this scenario, the SSSC has no direct influence on the loop impedance.

4.1.3 Topology 3

Topology 3 illustrates the effects of voltage and current reversal at the measurement points of the protection devices due to the SSSC. The critical criterion for the occurrence of these effects is the capacitive operating mode of the SSSC and the absolute values of the inductive line reactance. The conditions for the occurrence of these effects are summarised in section 2.3.2.This scenario also examines the extent to which an SSSC can impact the coordination of the protection devices.

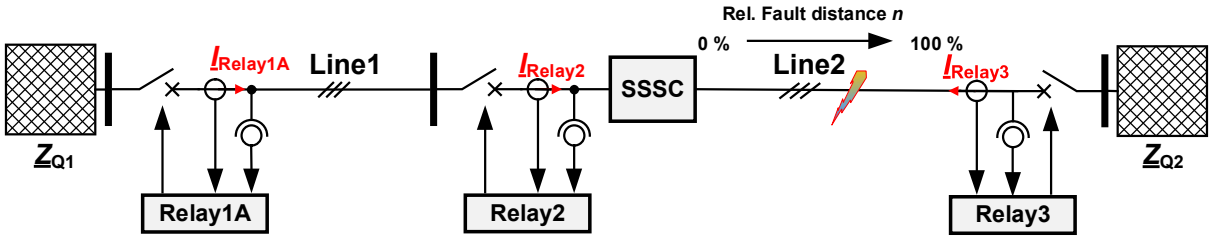


Figure 45: Topology 3

Three-Phase Fault with neglected the Fault Resistance R_f

Figure 46 graphically represents the equivalent circuit diagram for a three-phase fault in Scenario 3. In this case, neither the fault resistance R_f nor double feeding is considered.

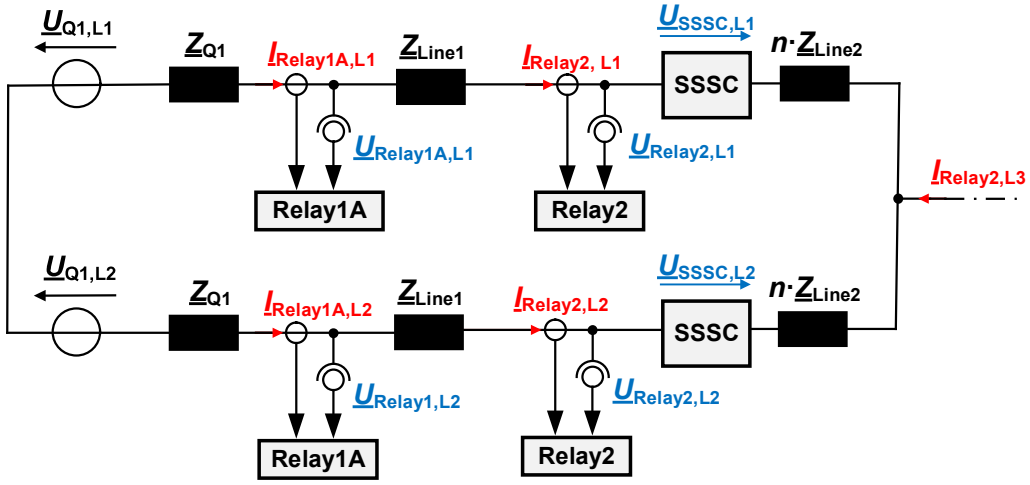


Figure 46: Equivalent circuit L1-L2 of a three-phase fault (L1-L2-L3), based on Figure 45 while neglecting the fault resistance R_f

The calculation of the fault loop impedance for the protection device Relay2 can be derived analogously to the considerations in chapter 4.1.1. The following section will first set up the voltage equation from the perspective of protection device Relay1A.

$$\underline{U}_{\mathrm{Relay1A,L1-L2}} = \underline{U}_{\mathrm{Relay1A,L1}} - \underline{U}_{\mathrm{Relay1A,L2}} =$$
$$= \underline{I}_{\mathrm{Relay1A,L1}} \cdot \underline{Z}_{\mathrm{Line1}} + \underline{U}_{\mathrm{SSSC,L1}} + \underline{I}_{\mathrm{Relay2,L1}} \cdot n \cdot \underline{Z}_{\mathrm{Line2}} - \underline{I}_{\mathrm{Relay2,L2}} \cdot n \cdot \underline{Z}_{\mathrm{Line2}} - \underline{U}_{\mathrm{SSSC,L2}} - \underline{I}_{\mathrm{Relay1A,L2}} \cdot \underline{Z}_{\mathrm{Line1}} \quad (50)$$

By applying $\underline{I}_{\mathrm{R1A,L1}} = \underline{I}_{\mathrm{R2,L1}}$ and $\underline{I}_{\mathrm{R1A,L2}} = \underline{I}_{\mathrm{R2,L2}}$ along with (30), (31) and (33), the loop fault impedance for L1-L2 for device R1A ultimately derived as shown in (51).

$$\underline{Z}_{\text{Relay1A,L1-L2}} = \underline{Z}_{\text{Line1}} + n \cdot \underline{Z}_{\text{Line2}} + \frac{\underline{U}_{\text{SSSC,L1}}}{\underline{I}_{\text{Relay1A,L1}}} \text{ bzw. } \underline{Z}_{\text{Relay1A,L1-L2}} = \underline{Z}_{\text{Line1}} + n \cdot \underline{Z}_{\text{Line2}} + \frac{\underline{U}_{\text{SSSC,L2}}}{\underline{I}_{\text{Relay1A,L2}}} \quad (51)$$

The SSSC thus directly distorts the loop impedance of the protection device Relay1A. Depending on the operating point, this can lead to an increase or decrease in the loop reactance, potentially impacting the coordination between devices Relay1 and Relay2. Meanwhile, the influence on reactance measured by Relay1A and Relay2 by the SSSC is identical.

Line-to-Ground Fault with Fault Resistance R_f and Double Infeed

Figure 47 represents the equivalent circuit for a single-phase fault with double feeding, also considering the fault resistance R_f. The following section examines the impedances of the protection devices Relay1A, Relay2, and Relay3. The impedances for Relay2 and Relay3 can be referenced from the results for Relay1A and Relay3 in Chapter 4.1.1.

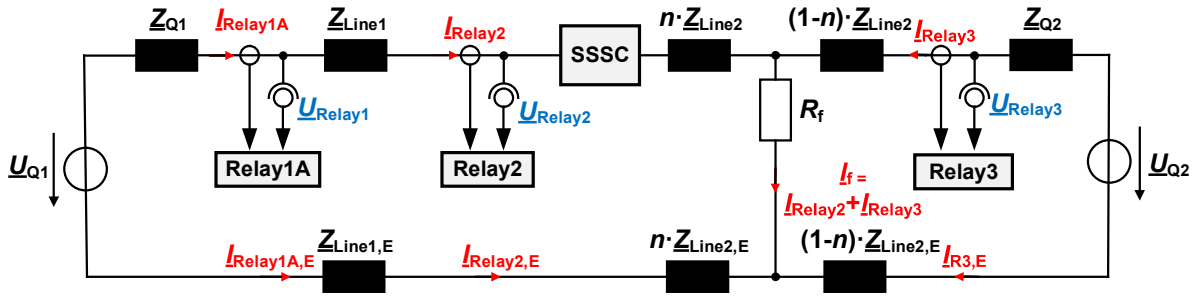


Figure 47: Equivalent circuit L-G of a one-phase fault (L-G), based on von Figure 45 while considering the fault resistance R_f and double infeed

In this scenario, the coordination between protection devices Relay1A and Relay2 is carried out. The setting of the ground impedance adjustment factors is done according to equation (5), with Relay1A configured as per equation (52) and Relay2 and Relay3 as per equation (53).

$$\underline{k}_{\text{E1}} = \frac{1}{3} \cdot \left(\frac{\underline{Z}_{0,\text{Line1}}}{\underline{Z}_{1,\text{Line1}}} - 1 \right) = \frac{\underline{Z}_{\text{Line1,E}}}{\underline{Z}_{\text{Line1}}} \quad (52)$$

$$\underline{k}_{\text{E2}} = \frac{1}{3} \cdot \left(\frac{\underline{Z}_{0,\text{Line2}}}{\underline{Z}_{1,\text{Line2}}} - 1 \right) = \frac{\underline{Z}_{\text{Line2,E}}}{\underline{Z}_{\text{Line2}}} \quad (53)$$

The loop equation for Relay1A is shown in (54).

$$\underline{U}_{\text{Relay1A}} = \underline{I}_{\text{Relay1A}} \cdot \underline{Z}_{\text{Line1}} \cdot \left(1 - \frac{\underline{Z}_{\text{Line1,E}} \cdot \underline{I}_{\text{R1A,E}}}{\underline{Z}_{\text{Line1}} \cdot \underline{I}_{\text{Relay1A}}} \right) + \underline{I}_{\text{Relay2}} \cdot n \cdot \underline{Z}_{\text{Line2}} \cdot \left(1 - \frac{\underline{Z}_{\text{Line2,E}} \cdot \underline{I}_{\text{R2,E}}}{\underline{Z}_{\text{Line2}} \cdot \underline{I}_{\text{Relay2}}} \right) + \\ + (\underline{I}_{\text{Relay2}} + \underline{I}_{\text{Relay3}}) \cdot R_f + \underline{U}_{\text{SSSC}} \quad (54)$$

With the simplifications $\underline{I}_{\text{Relay1A}} = -\underline{I}_{\text{Relay1A,E}}$, $\underline{I}_{\text{Relay2}} = -\underline{I}_{\text{Relay2,E}}$, $\underline{k}_{\text{E1}} = \underline{k}_{\text{E2}} = \underline{k}_{\text{E}}$ and $\underline{I}_{\text{Relay1A}} = \underline{I}_{\text{Relay2}}$ the impedance from the perspective of Relay1 is determined according to equation (6), resulting in (55). Even though the simplifications do not represent the field conditions, they decisively simplify (55).

$$\underline{Z}_{\text{Relay1A}} = \underline{Z}_{\text{Line1}} + n \cdot \underline{Z}_{\text{Line2}} + \frac{R_f}{1 + \underline{k}_{\text{E}}} + \frac{\frac{\underline{I}_{\text{Relay3}}}{\underline{I}_{\text{Relay1A}}} \cdot R_f}{1 + \underline{k}_{\text{E}}} + \frac{\underline{U}_{\text{SSSC}}}{\underline{I}_{\text{Relay1A}} \cdot (1 + \underline{k}_{\text{E}})} \quad (55)$$

By comparing equations (38) and (55), it can be seen that only an additional fifth term appears due to the previous simplifications, which includes the impedance of Line1. For relays Relay2 and Relay3, analogous results from Scenario 1 can be applied: equation (38) for Relay2 and equation (40) for Relay3.

Line-to-Line Fault with Fault Resistance R_f and Double Infeed

Figure 48 represents the equivalent circuit diagram for topology 3 in the case of a two-phase fault without ground contact, considering the fault resistance R_f and dual-sided fault feeding. The loop impedances of the respective protection devices are analysed again. The corresponding results for devices Relay2 and Relay3 can be referenced analogously from Chapter 4.1.1. The following section determines the loop impedance from the perspective of protection device Relay1A.

$$\underline{U}_{\mathrm{Relay1A,L1-L2}} = \underline{U}_{\mathrm{Relay1A,L1}} - \underline{U}_{\mathrm{Relay1A,L2}} =$$
$$= \underline{I}_{\mathrm{Relay1A,L1}} \cdot \underline{Z}_{\mathrm{Line1}} + \underline{U}_{\mathrm{SSSC,L1}} + \underline{I}_{\mathrm{Relay2,L1}} \cdot n \cdot \underline{Z}_{\mathrm{Line2}} + R_{\mathrm{f}} \cdot \left(\underline{I}_{\mathrm{Relay2,L1}} + \underline{I}_{\mathrm{Relay3,L1}}\right) - \underline{I}_{\mathrm{Relay2,L2}} \cdot n \cdot \underline{Z}_{\mathrm{Line2}} - \quad (56)$$
$$- \underline{U}_{\mathrm{SSSC,L2}} - \underline{I}_{\mathrm{Relay1A,L2}} \cdot \underline{Z}_{\mathrm{Line1}}$$

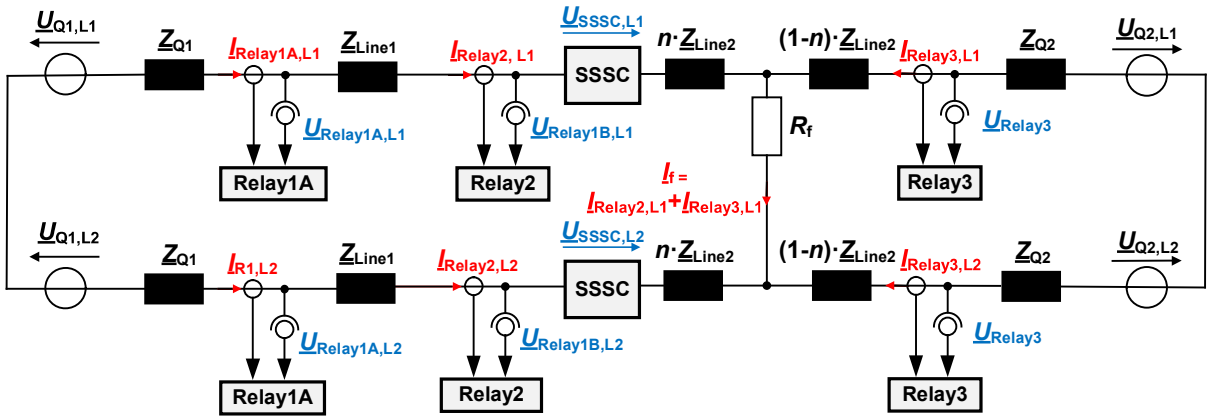


Figure 48: Equivalent circuit L1-L2 of a two-phase fault (L-L), based on Figure 45 while considering the fault resistance R_f and double infeed

For two-phase faults without ground contact, $\underline{I}_{\mathrm{Relay1A,L2}} = -\underline{I}_{\mathrm{Relay1A,L1}}$ also applies, which allows $\underline{U}_{\mathrm{SSSC,L2}} = -\underline{U}_{\mathrm{SSSC,L1}}$ as well. Based on $\underline{I}_{\mathrm{Relay1A,L1}} = \underline{I}_{\mathrm{Relay2,L1}}$ and $\underline{I}_{\mathrm{Relay1A,L2}} = \underline{I}_{\mathrm{Relay2,L2}}$ as well as equations (33) and (56), the following terms can ultimately be formulated. For more detailed calculation steps, see section 4.1.1.

$$\underline{Z}_{\mathrm{Relay1A,L1-L2}} = \underline{Z}_{\mathrm{Line1}} + \frac{\underline{U}_{\mathrm{SSSC,L1}}}{\underline{I}_{\mathrm{Relay1A,L1}}} + n \cdot \underline{Z}_{\mathrm{Line2}} + \frac{R_{\mathrm{f}}}{2} \cdot \left(1 + \frac{\underline{I}_{\mathrm{Relay3,L1}}}{\underline{I}_{\mathrm{Relay1A,L1}}}\right) \quad (57)$$

$$\underline{Z}_{\mathrm{Relay1A,L1-L2}} = \underline{Z}_{\mathrm{Line1}} + \frac{\underline{U}_{\mathrm{SSSC,L2}}}{\underline{I}_{\mathrm{Relay1A,L2}}} + n \cdot \underline{Z}_{\mathrm{Line2}} + \frac{R_{\mathrm{f}}}{2} \cdot \left(1 + \frac{\underline{I}_{\mathrm{Relay3,L1}}}{\underline{I}_{\mathrm{Relay1A,L1}}}\right) \quad (58)$$

The influence of the SSSC thus affects both Relay1A and Relay2 according to equations (43), (57) and (58) must therefore be considered in the coordination of the protection devices.

4.1.4 Topology 4

Figure 49 graphically represents the topology 4. This topology is similar to that in section 4.1.3, with the difference that the SSSC is now connected in the branch of Line 1. Consequently, based on the prior findings from Chapters 4.1.1 and 4.1.2, the protection devices Relay2 and Relay3 remain indirectly unaffected by the SSSC.

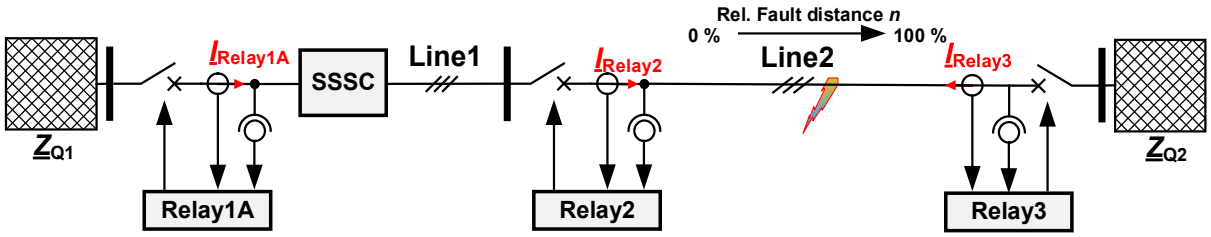


Figure 49: Topology 4

Three-Phase Fault with neglected the Fault Resistance R_f

Figure 50 graphically depicts an equivalent circuit diagram for an ideal three-phase fault, showing the fault loop L1-L2. According to the fault, the symmetry properties in equations (30) and (31) can be used to calculate the impedances. The calculation of the loop impedance for protection device Relay2 can be referenced from the calculation for device Relay1B in section 4.1.2.

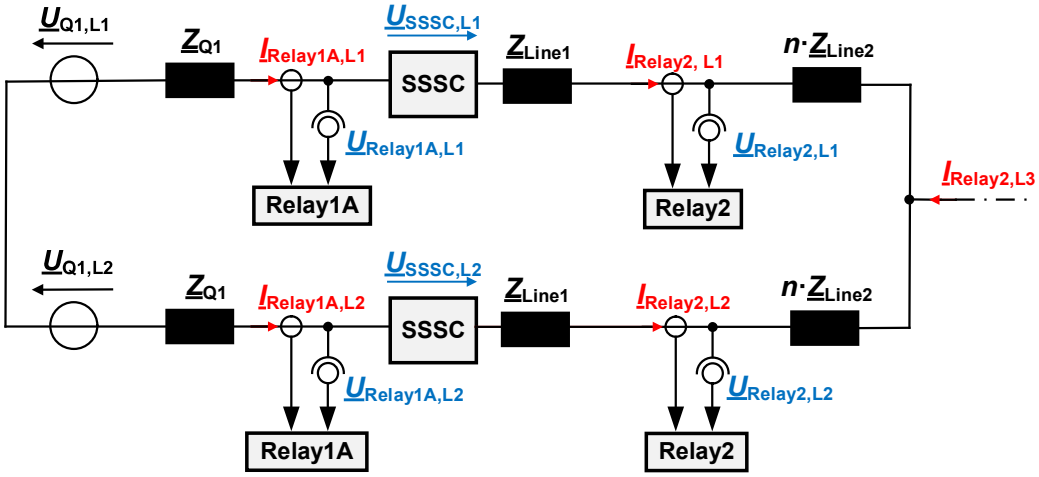


Figure 50: Equivalent circuit L1-L2 of a three-phase fault (L1-L2-L3), based on Figure 49 while neglecting the fault resistance R_f

The term for the impedance from the perspective of Relay1A, $\underline{Z}_{Relay1A,L1\text{-}L2}$, is identical to the calculations for topology 3, as in (51). The difference between topology 3 and 4 is that Relay1A continues to be influenced by the SSSC, while the SSSC is not present in the fault loop of Relay2. This results in additional requirements for the coordination of the protection devices Relay1A and Relay2.

Line-to-Ground Fault with Fault Resistance R_f and Double Infeed

Figure 51 represents the equivalent circuit diagram for a single-phase fault, considering the fault resistance R_f and double feeding. The impedances from the perspectives of the protection devices

Relay2 and Relay3 can be derived analogously from the calculations for devices Relay1B and Relay3 in Chapter 4.1.2.

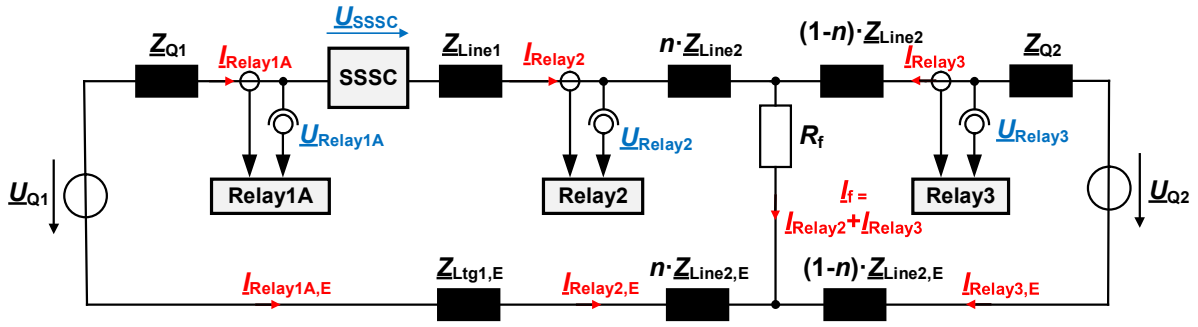


Figure 51: Equivalent circuit L-G of a one-phase fault (L-G), based on von Figure 49 while considering the fault resistance R_f and double infeed

The impedance term for protection device Relay1A corresponds to the term from topology 3 according to equation *(55)* and is thus influenced by the SSSC in determining the impedance. In contrast, the SSSC is not included in the fault loop of Relay2, allowing it to measure the unaffected impedance of the fault loop. This situation increases the requirements for the configuration of the protection devices to maintain the selectivity of devices Relay1A and Relay2.

Line-to-Line Fault with Fault Resistance R_f and Double Infeed

Figure 52 illustrates the equivalent circuit for the two-phase fault without ground and with double feeding for topology 4. The impedances from the perspectives of protection devices Relay2 and Relay3 can be derived analogously from the calculations for devices Relay1B and Relay3 in Chapter 4.1.2.

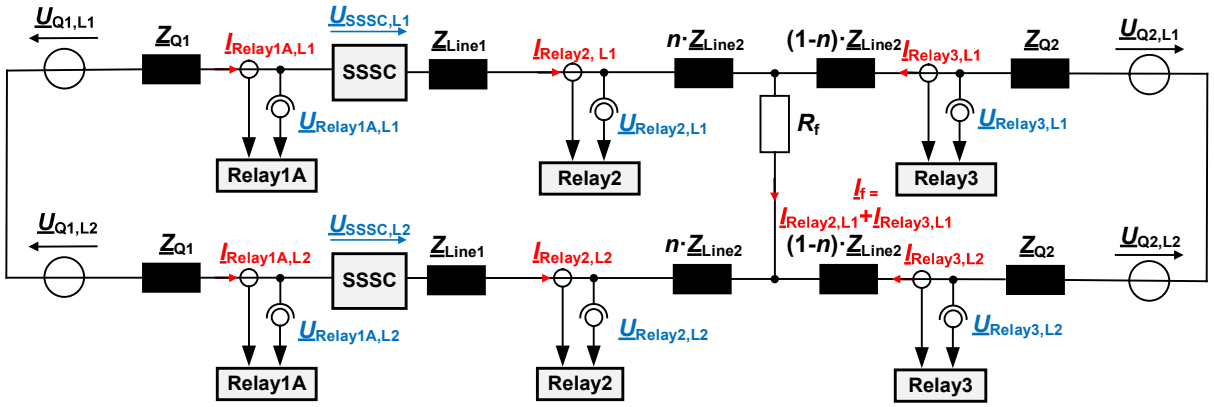


Figure 52: Equivalent circuit L1-L2 of a two-phase fault (L-L), based on Figure 49 while considering the fault resistance R_f and double infeed

Regarding the impedance of Relay1A, results for this case are identical to (57) and (58). Therefore, the SSSC influences the measured impedance of this device. Meanwhile, Relay2 and Relay3 are not influenced by the SSSC.

4.1.5 Summary of the Investigation of the 4 Topologies

A general summary of these investigations is given in section 8.1.

Summary Topology 1

For topology 1, it was demonstrated that the protection device Relay1A is influenced by the SSSC when calculating the fault loop impedance. Depending on the operating point of the SSSC, this influence can either increase or decrease the measured reactance. Additionally, the effects of voltage- or current-inversion could occur for Relay1A.The fault loop of the protection device Relay3 is not directly affected by the SSSC. However, there is an indirect influence where the SSSC can affect the short-circuit current, causing variations in the distortion of reactance due to the fault resistance $R_{f.}$

In this scenario, it proves advantageous that the protection device Relay3 communicates with device Relay1A via a communication channel, and the controlled overlap zone (see 2.1.2.2) is used to enable instantaneous tripping, even with fault loop impedance of Relay1A being influenced by the SSSC.

Summary Topology 2

Topology 2 demonstrated the benefit of placing a second protection device in the branch of the SSSC. Protection devices Relay1A and Relay3 yielded identical results to those observed in Scenario 1. By incorporating an additional device, Relay1B, this device is able to determine the impedance of the fault loop towards Line1 without influence, allowing for an accurate measurement of the line's reactance. The placement of an additional measurement point in the branch also enables the SSSC to be protected through differential protection.

Summary Topology 3 and 4

In topology 3, two protection devices, Relay1A and Relay2, are used in a graded configuration. Given the placement of the devices, both are influenced by the SSSC during impedance determination.

Topology 4 results in similar conclusions as topology 3. For this case, the grading of Relay1A and Relay2 can again be influenced by the SSSC, with only Relay1A being directly influenced by the SSSC. Depending on the topology, whether Relay1A or Relay2 can also be directly influenced by the SSSC due to the effects of voltage- or current-inversion.

4.2 Estimating the Influence of the SSSC on Distance Protection

Given the results of chapter 4.1.5, the following investigation aims to analyse the impact of the SSSC on the grading of two relays. This assessment is based on ideal three-phase short circuit calculations based on Figure 53. This topology is equivalent to the topology 3 in section 4.1.3. Here, the measured fault loop impedances of Relay1 and Relay2 are investigated for variable lengths of Line1 and Line2. Additionally to variable line lengths, also the short circuit power of the feeding grid is varied. The SSSC is operating in capacitive as well as in inductive operation mode.

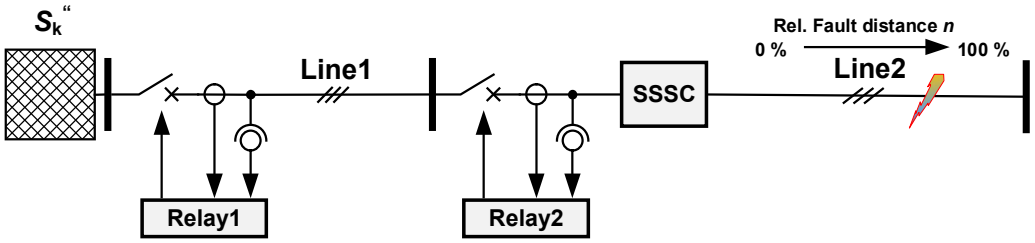


Figure 53: Grid topology for the assessment of the impact of the SSSC on the relay's grading and the occurrence of voltage- and current inversion

The following tables summarise the grid and device parameters and settings used for the investigation. The line impedances were chosen in dependency of the reactance of the SSSC for its rated current I_{SSSC} and maximum injected voltage U_{SSSC}. With these parameters, an ideal three-phase short-circuit calculation was performed (losses neglected). Subsequently, in the SSSCs operation point was considered inductive in 4.2.1, and capacitive in 4.2.2. For the solution of the calculation, an iterative Matlab routine was used, that considered the impact of the SSSC on the resulting short-circuit current, as well as on the voltages of the protection devices. Finally, the fault loop impedances of the protection devices, influenced by the SSSC, are calculated. This influence leads to the shifting of the zone boundaries. This is further explained in section 4.2.1.

For capacitive operation, the condition boundary for voltage inversion based on (13) and (16) were calculated as well.

Table 4: SSSC parameter for calculations based on Figure 53

Static Synchronous Series Compensator		
U_{SSSC}	I_{SSSC}	$X_{SSSC} = U_{SSSC} / I_{SSSC}$
V	A	Ω
1698	1800	0.943

Table 5: Line and grid parameter

Line Parameter		
X_{Line}	X_{Line1} / X_{SSSC}	X_{Line2} / X_{SSSC}
Ω	1	1
0.94	1	1
1.89	2	2
4.72	5	5
9.43	10	10
18.86	20	20
47.15	50	50

Grid Parameter
S_k"
GVA
1
2
5
10

Table 6: Protection relay settings for zone 1 (Z1) and zone 2 (Z2) of Relay1 & Relay2 in Figure 53

	Protection Relay Setting	
	Zone Z1	Zone Z2
Relay1	$0.85 \cdot X_{Line1}$	$X_{Line1} + 0.57 \cdot X_{Line2}$
Relay2	$0.85 \cdot X_{Line2}$	-

4.2.1 SSSC Operating in Inductive Mode and Ideal Three-Phase Short-Circuit

For inductive operation of the SSSC, Figure 54 and Figure 55 visualise the calculation results. Figure 54 illustrates the relative fault distance on Line2, for the SSSC shifting the fault from $Z1_{Relay2}$ to $Z2_{Relay2}$. Figure 55 shows this boundary for the SSSC shifting the fault from $Z2_{Relay1}$ to $Z3_{Relay1}$. $Z3_{Relay1}$ starts at the zone boundary of $Z2_{Relay1}$ at 57 % of Line2.

The diagrams can be interpreted as follows: The number in the heatmap is equal to the actual fault distance that leads to a detection of the fault in the corresponding zone. In Figure 54 in the top left plot, for $X_{Line1}/X_{SSSC} = X_{Line2}/X_{SSSC} = 1$, the fault distance for a zone shift of Relay2 from $Z1_{Relay2}$ to $Z2_{Relay2}$ is equal to 14 %. This means that, if the factual fault is located at 14 % of Line2, it is already recognised in $Z2_{Relay2}$.

$Z1_{Relay2}$ is set with a relative distance of 85 % of Relay1. With the SSSC operating inductive it is expected that the boundary for the transition from Z1 to Z2 will decrease. This can be observed in Figure 54. The worst case for the zone shifts of Relay2 is reached for $X_{Line2}/X_{SSSC} = 1$. The situation is improved for X_{Line2}/X_{SSSC} increasing. It can also be seen that the impact of the SSSC on the distance measurement increases both, for an increasing ratio X_{Line1}/X_{SSSC}, as well as for a decreasing short-circuit power. This is because, with a decreasing short-circuit power, the short-circuit current will also decrease while the injected voltage is kept constant, which is leading to an increase of the injected reactance by the SSSC.

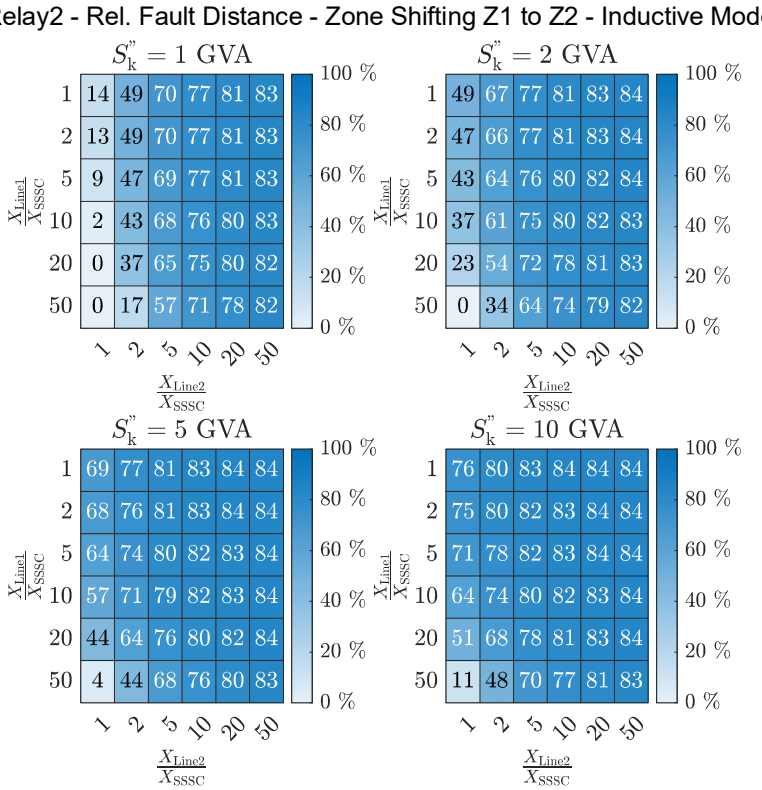


Figure 54:Zone shifting Z1 to Z2 for Relay 2 for inductive operation mode of SSSC; ideal = 85 %

The transition from $Z2_{Relay1}$ to $Z3_{Relay1}$ is set with a relative fault distance on Line2 of 57 %. For this investigation, it is again expected that the transition boundary will decrease due to the inductive operation mode of the SSSC.

As before, the worst case is given by $X_{Line2}/X_{SSSC} = 1$. The impact of the SSSC is again decreasing with this ratio X_{Line2}/X_{SSSC} rising. This also holds true with the short-circuit power increasing.

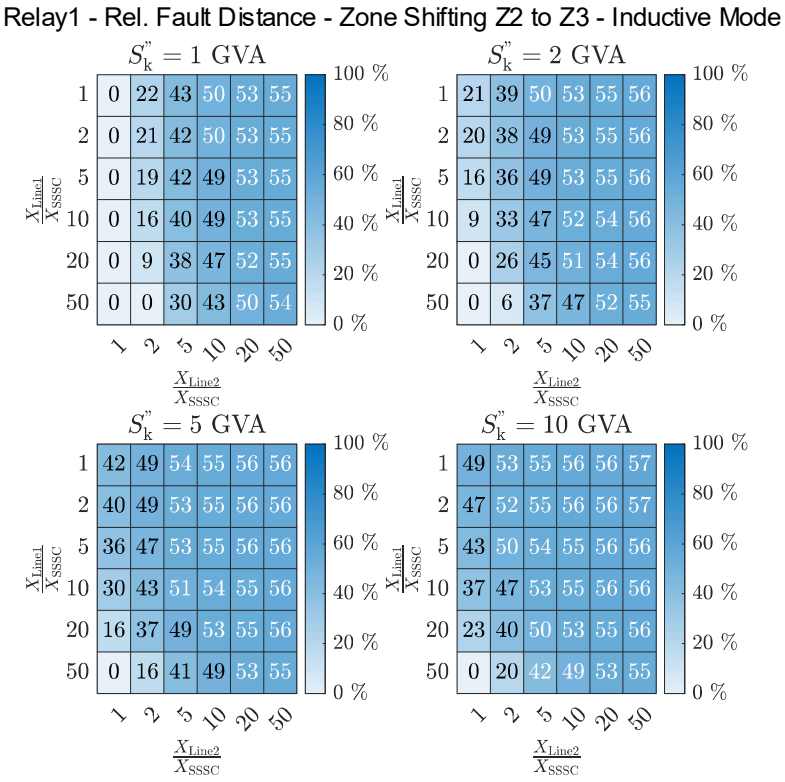


Figure 55: Zone shifting Z2 to Z3 for Relay1 for inductive operation mode of SSSC; ideal = 57 %

4.2.2 SSSC Operating Capacitive and Ideal Three-Phase Short-Circuit

For the following diagrams, the SSSC is operating in capacitive mode. Figure 56 illustrates the zone shifting boundary for shifting the fault from $Z2_{Relay2}$ to $Z1_{Relay2}$. Figure 57 summarises the relative fault distance on Line2 for shifting the fault from $Z3_{Relay1}$ to $Z2_{Relay1}$ and Figure 58 shows the results for shifting the fault from $Z2_{Relay1}$ to $Z1_{Relay1}$.

$Z1_{Relay2}$ is set with 85 % of Line2. With the SSSC operating capacitive, it is expected that the zone boundary between $Z1_{Relay2}$ and $Z2_{Relay2}$ will be increased due to the negative reactance injection. In Figure 56 it can be seen that $X_{Line2}/X_{SSSC} = 1$ or 2 is equal to the worst case for zone shifting. The fault could be at 100 % of Line2 (or beyond), and it would still be detected as a short-circuit in $Z1_{Relay2}$. As before, the impact of the SSSC once again decreases for a shorter Line1 or a higher short-circuit power.

The transition boundary for $Z2_{Relay1}$ to $Z3_{Relay1}$ is set as before with a relative fault distance on Line2 of 57 %. It is again expected that the transition boundary will be increased due to the inductive operation mode of the SSSC. This can be seen in Figure 57. For $X_{Line2}/X_{SSSC} = 1$ or 2, a fault in $Z3_{Relay1}$ is likely to be shifted into $Z2_{Relay1}$ which would directly influence the grading of the protection devices Relay1 and Relay2.

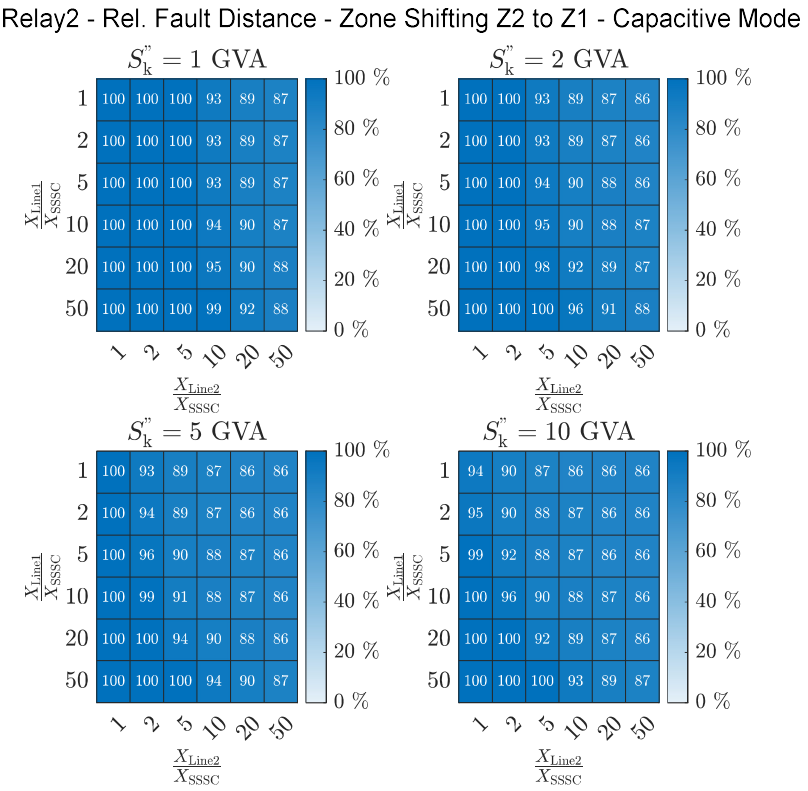


Figure 56: Zone shifting Z2 to Z1 for Relay2 for capacitive operation mode of SSSC; ideal = 85 %

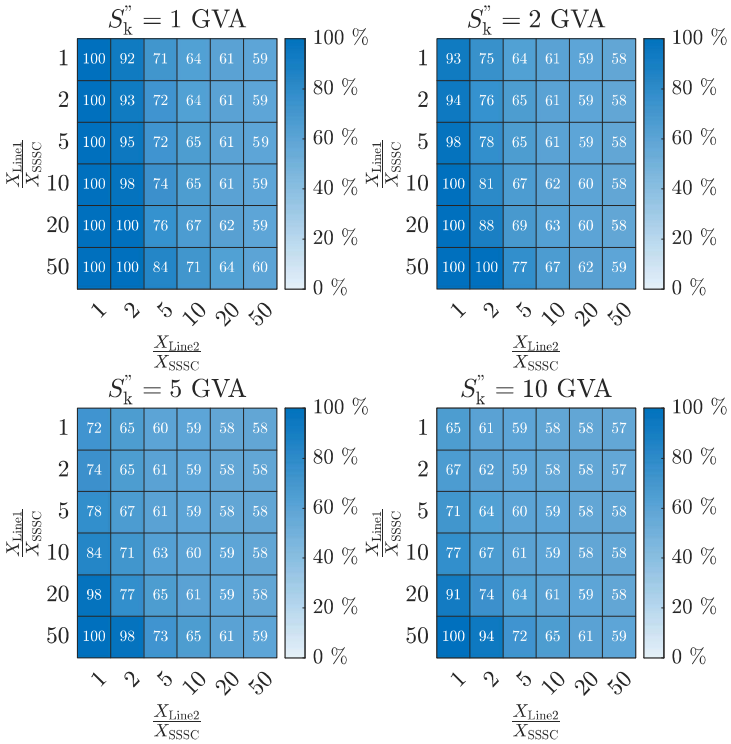


Figure 57: Zone shifting Z3 to Z2 for Relay1 for capacitive operation mode of SSSC; ideal = 57 %

Additionally, an unselective trip would also occur, if a fault on Line2 led to a Zone 1 trip for Relay1 in $Z1_{Relay1}$. Figure 58 illustrates the calculation result. For the given configuration it can be seen that is a

very unlikely scenario. Only for S_k'' = 1 or 2 GVA and X_{Line1}/X_{SSSC} = 1 or 2 it is possible, that this scenario could occur. A zero in this plot means that the fault cannot be shifted into $Z1_{Relay1}$.

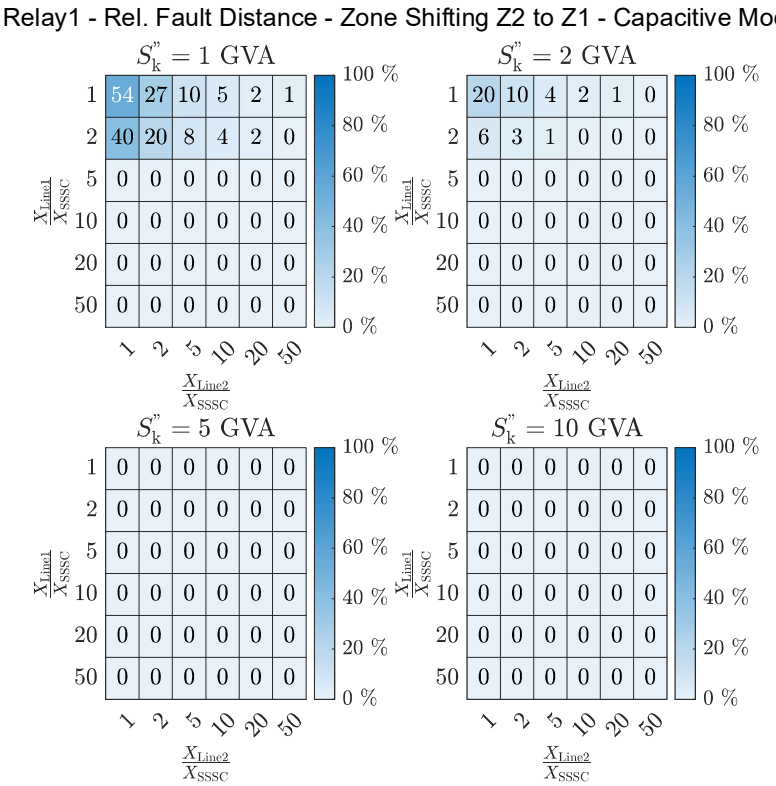


Figure 58: Zone shifting Z2 to Z1 for Relay1 for capacitive operation mode of SSSC; ideal = 0 %

Voltage inversion occurs, as soon as the conditions in (13) and (16) are fulfilled. Figure 59 displays the boundary for the effect to occur. It can be seen that a short Line1 leads to the worst results. If the relative fault distance reaches a value of 0 %, this means that voltage inversion only occurs for terminal short circuits.

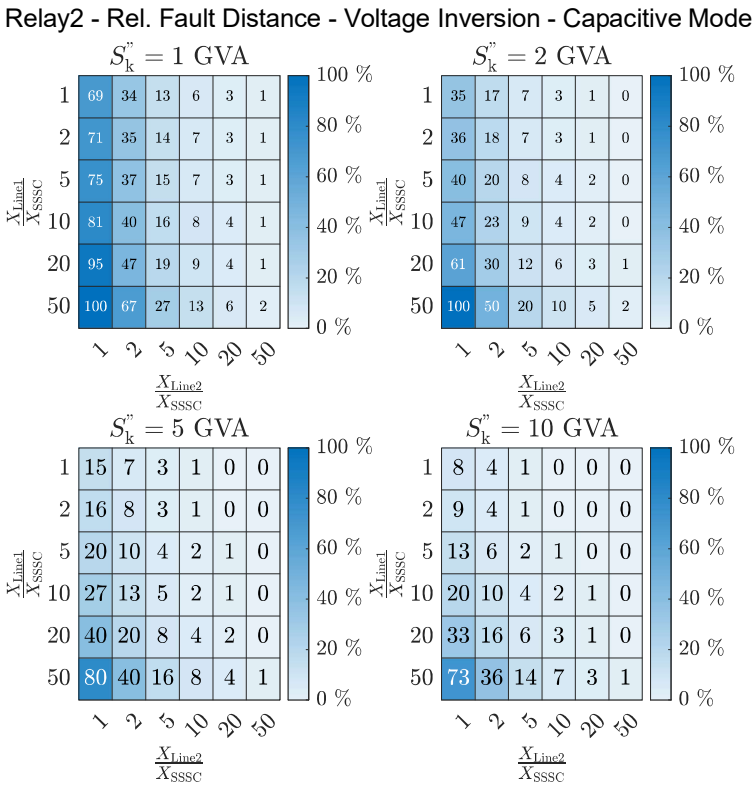


Figure 59: Voltage inversion for Relay 2 for capacitive operation mode of SSSC; ideal = 0 %

For a more detailed investigation of the voltage inversion boundary, the following topology in Figure 60 was used. Here, Relay1 and Line1 were spared, while the short-circuit power S_k'' was varied in such way that voltage inversion would occur for Relay2. Current inversion was not further investigated because its mandatory condition as described in (18) could not be fulfilled for this scenario.

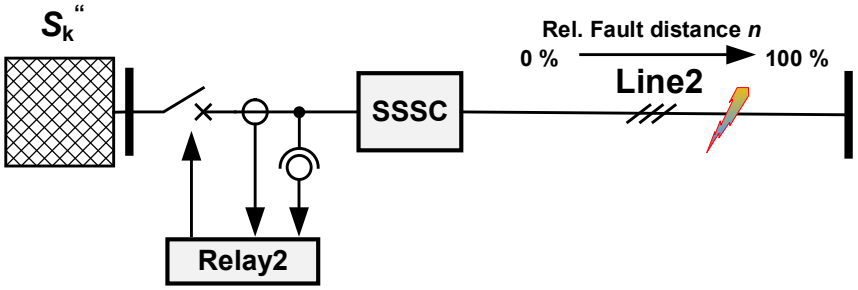


Figure 60: Topology for investigation the voltage inversion boundary for multiple values of X_{Line2}/X_{SSSC}

The result of this calculation is shown in Figure 61. It can be seen that the minimal short-circuit power for voltage inversion to occur increases for a shorter Line2. For X_{Line2}/X_{SSSC} = 1 or 2, voltage inversion is likely to occur even for faults being at 20 % of line length. For $X_{Line2}/X_{SSSC} \geq 5$ and considering S_k'' = 10 GVA, voltage inversion will only occur for (almost) terminal short-circuits.

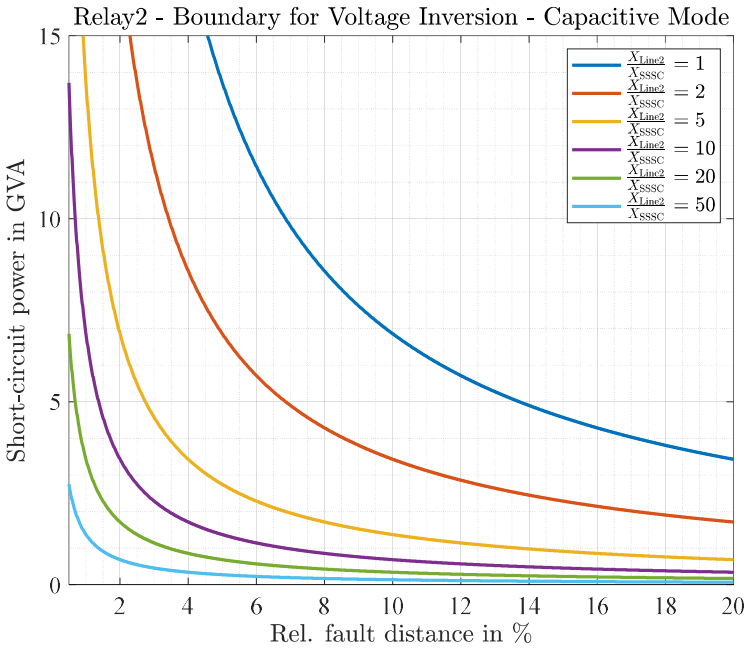


Figure 61: Voltage inversion boundary for multiple values of X_{Line2}/X_{SSSC}

4.2.3 Summary and Conclusion

Considering the results from chapters 4.2.1 and 4.2.2, the following conclusions can be made:

- The impact of the SSSC on the distance measurement of a protection device decreases for higher short-circuit powers (short-circuit currents).
- For the given topology in Figure 53, the worst case is given for a weak grid (S_k'' = 1 GVA) that is connected by a long line (X_{Line1}/X_{SSSC} = 50) to a short line, or a line with a strong SSSC used for compensation (X_{Line2}/X_{SSSC} = 1).
- Zone shifting (overreach and underreach) can occur, but the impact of the SSSC is limited for the ratio $X_{Line2}/X_{SSSC} \geq 10$.
- Voltage inversion can be a problem for very short lines and low short-circuit powers. For $X_{Line2}/X_{SSSC} \geq 5$, voltage inversion will only occur for faults very close to the SSSCs terminals.

4.3 Use Case Scenario

For the next step, a SSSC will be implemented into a use case scenario and its impact on protection devices will be studied using simulations in Matlab / Simulink and real-time simulations tests with protection devices (see section 6). Figure 62 illustrates the investigated 220-kV-topology. Two grids, A and D, are connected by three double lines, Line AB, Line BC and Line CD. There are four substations (SS), A, B, C and D. The branches are named based on their start and end SS, the additional number gives information about the considered three-phase circuit.

The SSSC is connected at the end of Line BC at branch CB1. All parameters are listed in Table 7, Table 8 and Table 9. For additional explanations on the SSSC parameters, see section 3.

The line model is realised as a T-equivalent circuit. Additionally, the inductive coupling of the two three-phase systems in the zero-sequence system is considered. For the reduction of the calculation effort, and also for saving hardware resources on the real-time simulator (see section 5.2), the capacitive coupling of the two circuits is neglected (due to no decisive impact results).

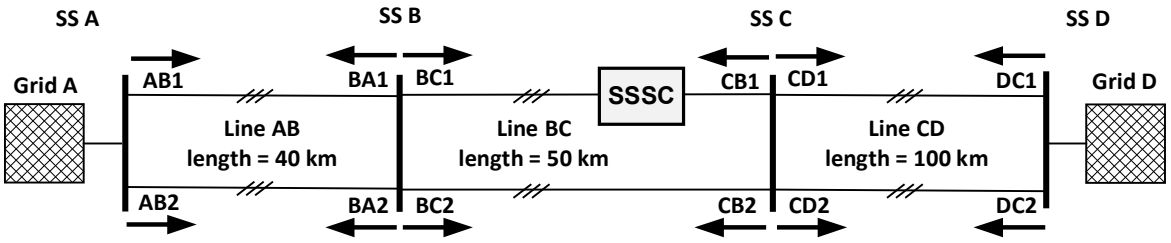


Figure 62: Grid topology of the investigated use case scenario

Table 7: Line parameters

Line	length	R_1'	R_0'	R_{0m}'	X_1'	X_0'	X_{0M}'	φ	X_1/R_1	X_0/R_0	C_1'	C_0'
-	km	Ω	Ω	Ω	Ω	Ω	Ω	°	1	1	nF	nF
AB	40	0.03	0.1	0.09	0.3	0.7	0.3	84.3	10	7.1	13	7
BC	50	0.08	0.2	0.15	0.4	1	0.5	78.7	5	5	9	6
CD	100	0.08	0.2	0.15	0.4	1	0.5	78.7	5	5	9	6

Table 8: Grid parameters

U_N = 220 kV	R_1	R_0	X_1	X_0	$S_k''_{3ph}$	$S_k''_{1ph}$	δ
-	Ω	Ω	Ω	Ω	GVA	GVA	°
A	0.8	2.1	6.3	17	7.6	1.6	0
D	0.8	1.5	5	12	9.6	2.2	-15

Table 9: SSSC parameters

C_{DC}	U_{SSSC}	I_{SSSC}	I_{SC}	U_{DC}	U_{LB}	U_{UB}	$k_{P,PLL}$	$k_{I,PLL}$
mF	V	A	pu	V	pu	pu	1	1/s
108.9	1698	1800	1.1	744	1.25	0.75	15	90

4.3.1 Grid Verification using Short-Circuit Simulations and Numerical Short-Circuit Calculations using Matlab / Simulink

For the verification process of the given grid topology, short-circuit simulations were performed and compared with short-circuit calculations using a Matlab model. Due to the high effort required for solving the short-circuits analytically, it was decided to solve them numerically using Matlab / Simulink in an iterative procedure.

Subsequently, one-, two- and three-phase short-circuits on Line AB, Line BC and Line CD at 30 % of the line lengths were examined with the SSSC operating inductive, capacitive or while being in monitoring mode. To evaluate the impact of the SSSC on the short circuit currents, the bypass was deactivated for this verification process.

To consider the SSSC in the numerical solution, the ideal behaviour of the SSSC (injected voltage is 90° perpendicular to current for steady-state) was assumed. This behaviour could be directly applied for calculations in symmetrical components.

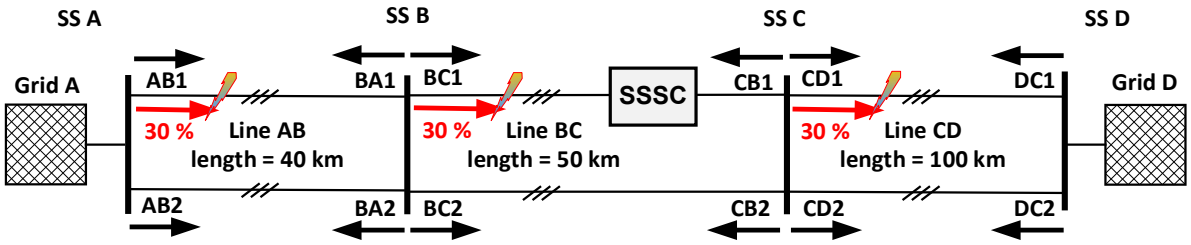


Figure 63: Grid topology for one-, two- and three-phase short-circuit calculations with the SSSC operating inductive, capacitive or being deactivated and the fault location 30% of line length

The model introduced passed this verification process. The results of the short-circuit simulations and calculations are summarised in section 8.2. The maximum relative error for the fault current for all scenarios is equal to about 0.66 %. Additional derivations between the results are explained by the neglection of the capacitances for the short-circuit calculation.

4.3.2 Short-Circuit Simulations and Investigations on the Impact of the SSSC with Bypass Failure on Fault Loop Impedances with faults in Line BC

In the following chapter, the impact of the SSSC on fault impedances is investigated. The bypass of the SSSC is deactivated for this analysis. One, two and three phase faults are simulated on line BC. Regarding the given topology in Figure 62, the following reactance ratios can be calculated for X_{SSSC} = 0.943 Ω.

Table 10: Reactance ratios for use-case

Line AB: $X_{1,AB}$ / X_{SSSC} = 12.73 Line BC: $X_{1,BC}$ / X_{SSSC} = 21.21 Line CD: $X_{1,CD}$ / X_{SSSC} = 42.42

Considering the results of section 4.2, it is therefore expected that the influence of the SSSC will not be severe on the measured fault distance. For the following simulations, a fault resistance R_f of approx. 0 Ω, 5 Ω and 10 Ω is considered. The fault distance varies between 1 % and 99 % while the SSSC is either in monitoring, capacitive or inductive mode. For the analysis, a steady-state short-circuit window of 1 s is used. This is shown in Figure 64.

For this window, a Fast Fourier Transform (FFT) is performed and the phasors of the fundamental are then used for calculating the fault impedance of the investigated branch. Table 11 summarises the simulated fault cases for the following results. For the SSSC in monitoring mode, these fault simulations acted as a reference scenario for calculating the error of impedance calculation for when the SSSC operated inductive or capacitive. The relative error is then given related to the positive line reactance of line BC for branch BC1 and CB2, line AB for branch AB1 or AB2 and line CD for branch DC1 or DC2.

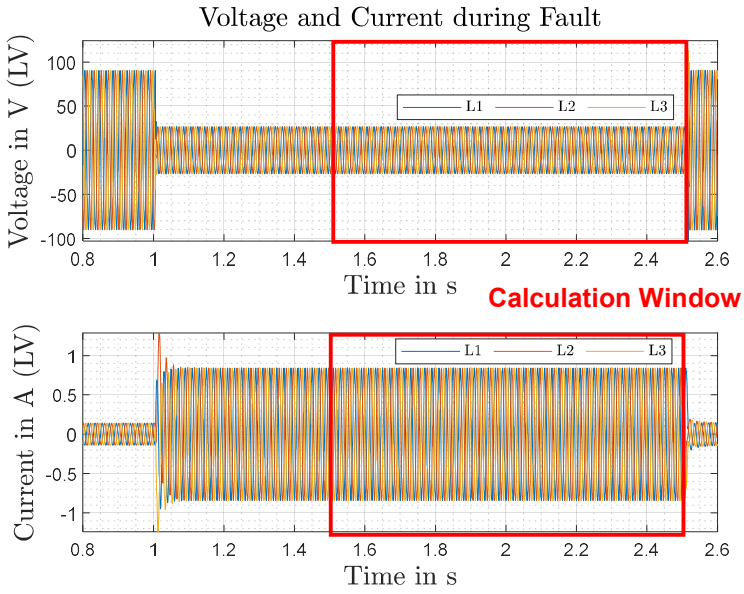


Figure 64: Steady-state short circuit window for impedance calculation

Table 11: Summary of simulated fault cases for faults on line BC

Fault Distance	Fault	R_f	SSSC Mode
%	-	Ω	-
1	L-G	≈ 0	Monitoring
[5:5:95]	L-L	5	Inductive
99	L-L-L	10	Capacitive

In the following section, the investigated fictitious relays are named after their corresponding branch. The measurement error of the relays displayed by the relative error in % and is calculated in (59).

$$\text{Rel. Error } \varepsilon = \frac{\text{Reactance with SSSC active } - \text{Reactance with SSSC deactivated}}{\text{Corresponding Line Reactance}} \cdot 100\,\% \qquad (59)$$

Influence of the SSSC on Branch CB1

Following, the impact of the SSSC on a fictitious distance protection relay in branch CB1 (Figure 62) is investigated. For the calculation of the fault impedance, equation (8) for L-G loops and equation (33) for L-L loops is used. According to equations (5) and (7), the ground factor is calculated with $\underline{k}_E$ = 0.4477 - j·0.033 and the mutual coupling compensation factor with $\underline{k}_M$ = 0.3399 - j·0.066. Figure 65, Figure 66 and Figure 67 illustrate the impact of the SSSC on the fault impedance in branch CB1 for a L-G, L-L and three-phase fault. The relative error based on (59) is used as an indication of impact. It is calculated based on the difference between the fault impedance while the SSSC is in monitoring mode and when the SSSC operates inductive or capacitive, related to the line reactance of line BC, as in (59).

Regarding the L-G fault scenarios in Figure 65, it can be seen that the impact of the SSSC on the impedance measurement increases for the fault resistance R_f also increasing. This is because the short-circuit current decreases for increasing values of R_f, leading to a higher impact of the SSSC, as also illustrated in Figure 19.

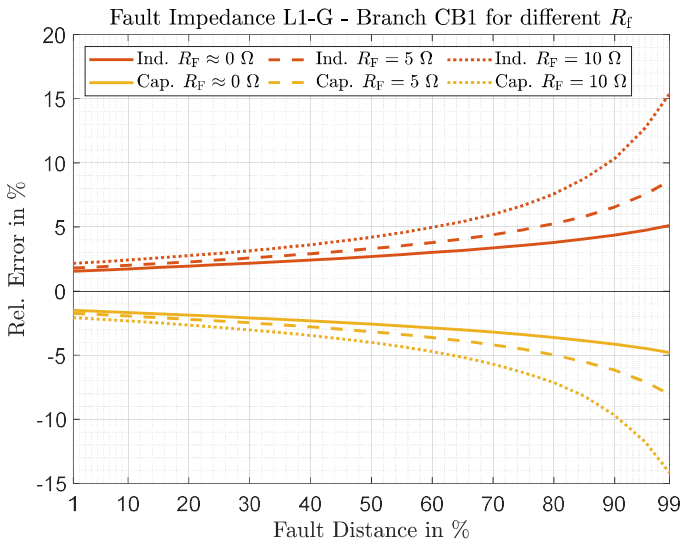


Figure 65: Relative measurement error in branch CB1 for L-G fault, for the inductive and capacitive operation of the SSSC and different R_f

Additionally, the impact of the SSSC also increases for increasing fault distance. This is due to the short-circuit current decreasing for more distant faults. Figure 66 illustrates the impact of the SSSC on fault impedances for L-L faults. It can be seen that the impact of the SSSC is decreased for R_f = 5 Ω and 10 Ω, compared to corresponding L-G faults. Meanwhile, the impact for $R_f \approx 0\ \Omega$ is almost identical to the L-G fault scenarios. It can also be noted that the impact for inductive operation is slightly higher than for capacitive operation, which can again be explained by the impact of the operation mode on the current amplitude.

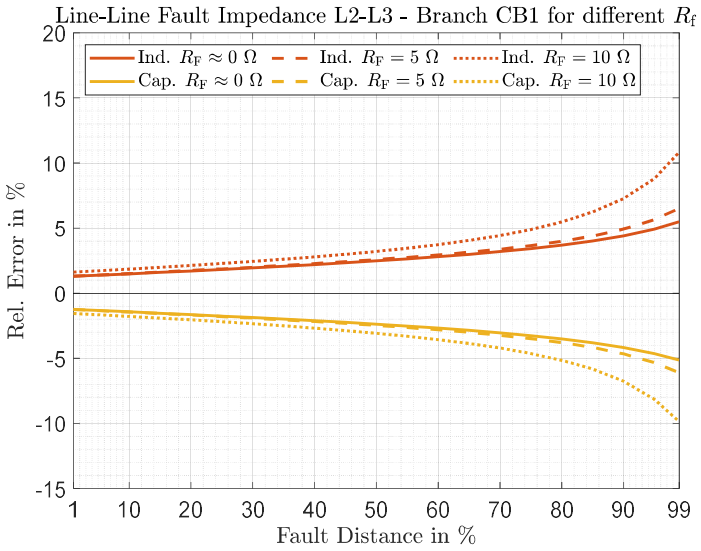


Figure 66: Relative measurement error in branch CB1 for L-L fault, for inductive and capacitive operation of the SSSC and different R_f

For the three-phase fault results, illustrated in Figure 67, the impact of the SSSC on the impedance measurement is the least. Regarding the effect of voltage inversion, it can occur for the absolute negative error being bigger than the fault distance. It can be seen in Figure 65, Figure 66 and Figure 67 that voltage inversion would only occur for a maximum fault distance of 1 to 2 %. The results discussed

show that the impact of the SSSC is given, but not severe for the fault location detection. This is further explained in Figure 68, Figure 69 and Figure 70, which display the calculated fault distance by the fictitious distance relay for L-L faults with different values of R_f.

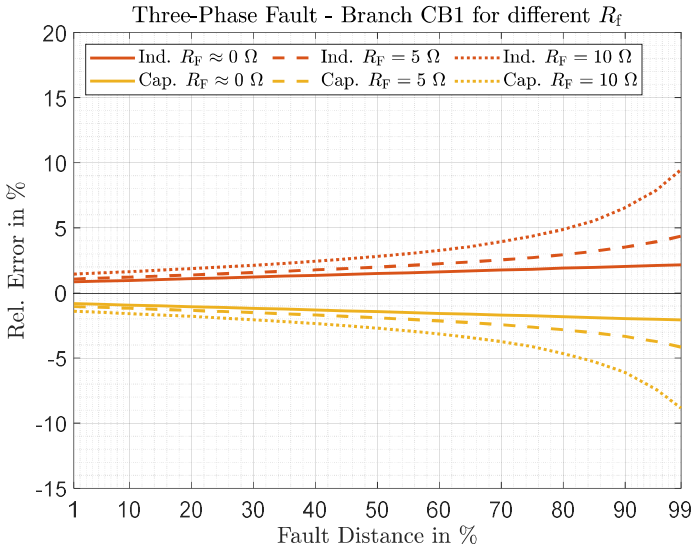


Figure 67: Relative measurement error in branch CB1 for three-phase fault, for inductive and capacitive operation of the SSSC and different R_f

Figure 68 illustrates the case for $R_f \approx 0\ \Omega$. As shown in Figure 66, the calculated fault distance varies by up to ± 6 %.

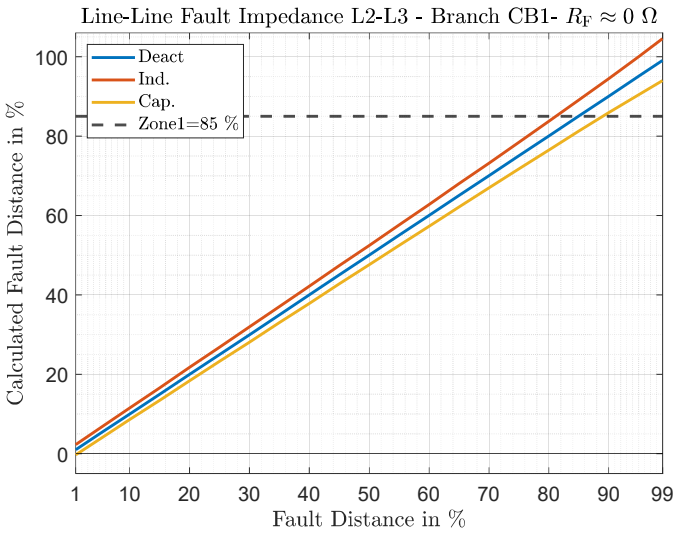


Figure 68: Rel. calculated fault distance for L-L fault for inductive and capacitive operation of the SSSC and $R_f \approx 0\ \Omega$

Figure 69 and Figure 70 represent the results of the L-L fault with $R_f = 5\ \Omega$ and $R_f = 10\ \Omega$. As shown in Figure 66, the impact of the SSSC increases with R_f. Nevertheless, the error of distance measurement for these scenarios is mainly caused by the underreach, occurring due to the pre-fault load flow and the presence of the fault resistance [3]. Comparing the results of Figure 69 and Figure 70 with Figure 68, it can be seen that the impact of the fault resistance on the fault distance detection is a lot stronger than

the impact of the SSSC. The maximum difference of the measured fault distance for the SSSC monitoring and for R_f = 5 Ω is about 20 %, for R_f = 10 Ω is about 33%, compared to $R_f \approx 0$ Ω.

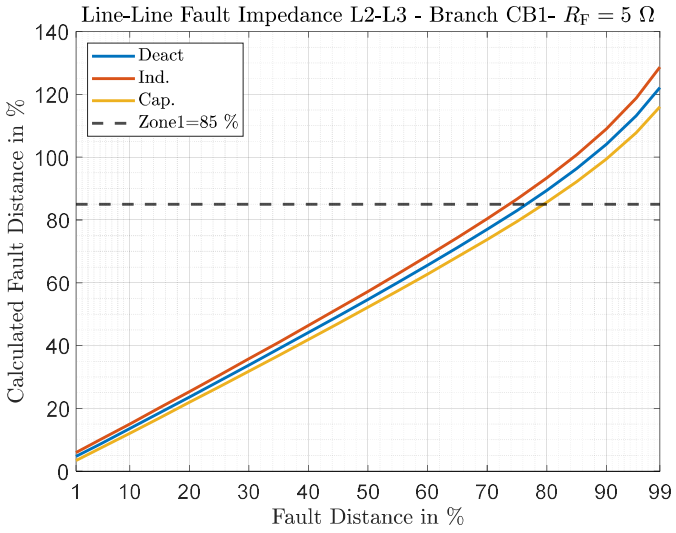


Figure 69: Rel. calculated fault distance for L-L fault for inductive and capacitive operation of the SSSC and R_f = 5 Ω

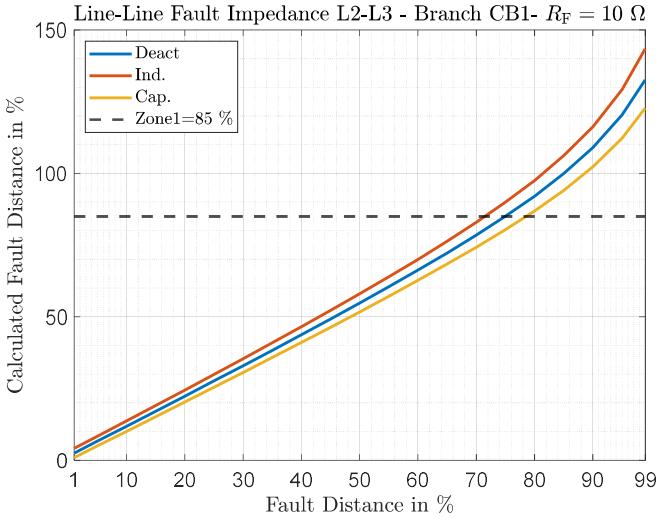


Figure 70: Rel. calculated fault distance for L-L fault for inductive and capacitive operation of the SSSC and R_f = 10 Ω

Figure 71 illustrates the impact of the mutual coupling compensation factor $\underline{k}_M$ for the fault distance calculation for a L-G fault with $R_f \approx 0$ Ω. It can be seen that not considering $\underline{k}_M$ (as in equation (6)) leads to severe underreach for faults in the end of the line.

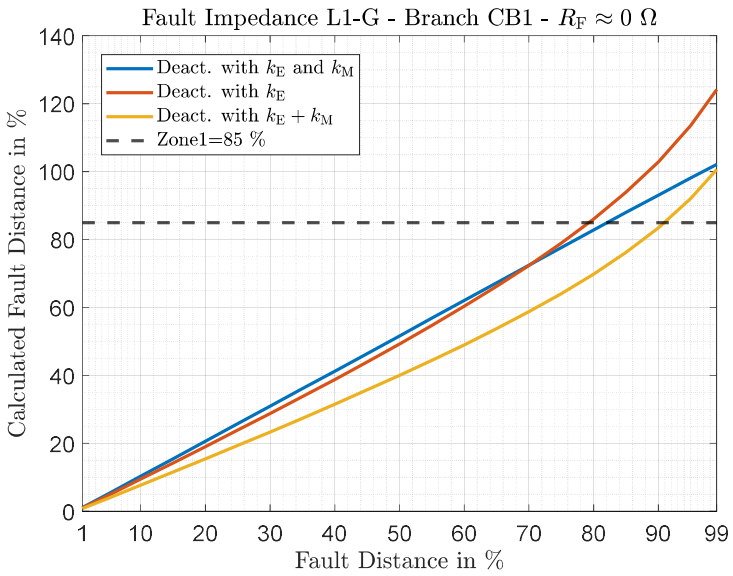


Figure 71: Rel. calculated fault distance for L-G fault for monitoring mode of the SSSC and $R_f \approx 0\ \Omega$; analysis of the impact of $\underline{k}_M$

Regarding the ProtHIL tests following in section 6, the used distance protection relays do not have the functionality of mutual coupling compensation. As a work-around, it would have also been possible to combine $\underline{k}_E$ and $\underline{k}_M$ as shown in (60).

$$\underline{Z}_{R,LE} = \frac{\underline{U}_{R,LE}}{\underline{I}_{R,L} + \underline{I}_{E1} \cdot (\underline{k}_E + \underline{k}_M)} \tag{60}$$

This led to severe overreach, as illustrated in Figure 71. Therefore, it was decided to use L-L faults for the ProtHIL tests, since a similar impact of the SSSC on L-L faults is expected as for L-G faults, as shown in Figure 66.

Influence of the SSSC on Branch BC1

Figure 72, Figure 73 and Figure 74 illustrate the summarised impact on the measured fault impedances of branch BC1 (Figure 62). It can be seen that the impact of the SSSC is minimal, with a maximum influence of about 0.45 % for a three-phase fault with R_f = 10 Ω. This directly fulfils the expectancies, as derived before for Relay3 in section 4.1.1. Using the opposite branch of the SSSC for reliable fault detection can therefore turn out as an advantage.

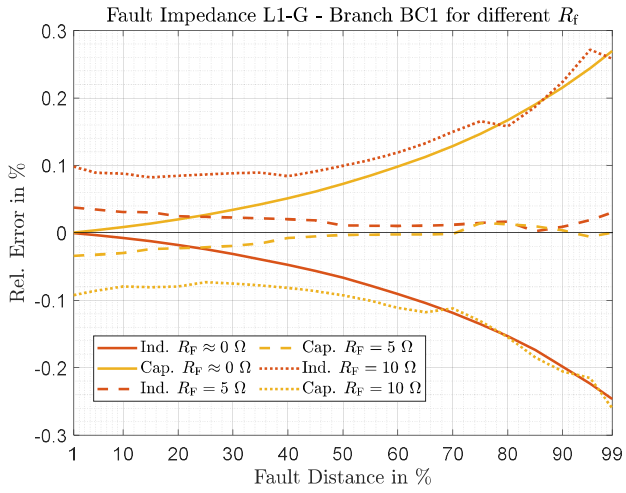


Figure 72: Relative measurement error in branch BC1 for L-G fault, for inductive and capacitive operation of the SSSC and different R_f

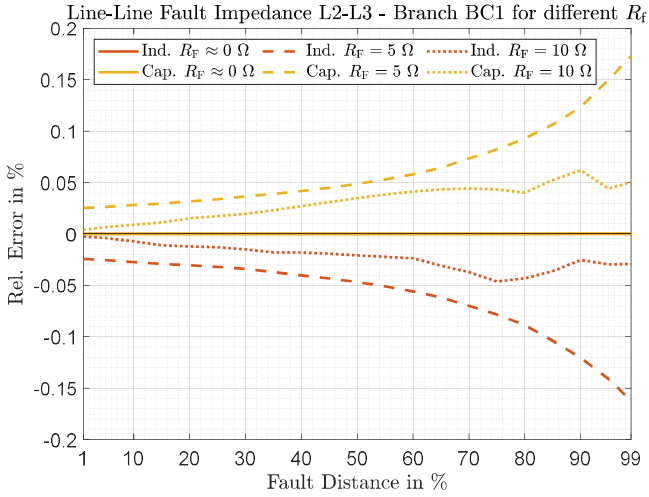


Figure 73: Relative measurement error in branch BC1 for L-L fault, for inductive and capacitive operation of the SSSC and different R_f

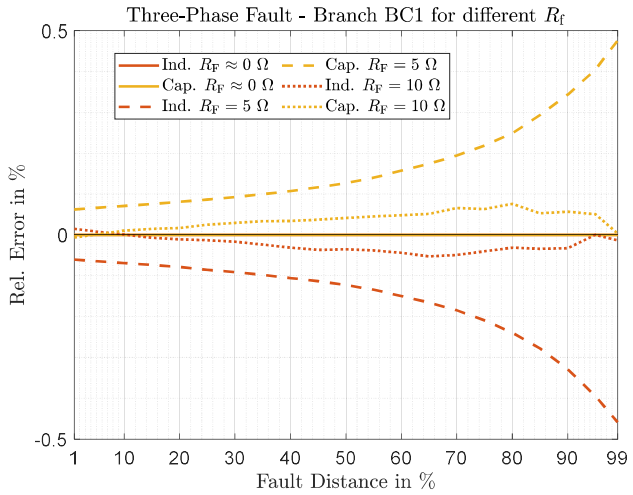


Figure 74: Relative measurement error in branch BC1 for three-phase fault, for inductive and capacitive operation of the SSSC and different R_f

Influence of the SSSC on Branch AB and DC

Figure 75 illustrates the impact of the SSSC on the distance measurement error for branch DC1 or DC2 and AB1 or AB2 (identical results for branch 1 and branch 2) for L-L faults (Figure 62). It can be seen that the maximum absolute influence for DC is around ±3.2 % (relative to line reactance DC), while for AB it is around 3 % (relative to line reactance AB). Regarding the large distance of the branches to the fault and typical measurement errors due to several effects (impact of R_f and load flow, additional infeed, multi terminal lines [3], inhomogeneous values for zero-sequence systems leading to measurement errors due to $\underline{k}_E$ and $\underline{k}_M$), this impact is categorized as not severe.

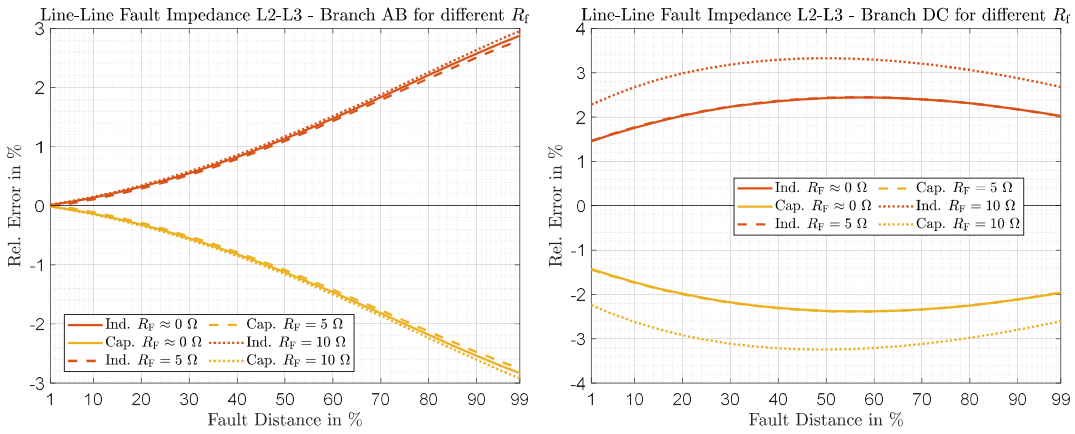


Figure 75: Relative measurement error in branch CD1 or CD2 and AB1 and AB2 for L-L fault, for inductive and capacitive operation of the SSSC and different R_f

4.3.3 Key Findings for the Impact of the SSSC in Case of Bypass Failure

The key findings of the simulations used for assessing the impact of the SSSC on a fictitious distance protection relays are summarised as following.

- **Impact of the fault resistance R_f:** The influence of the SSSC increases with the fault resistance R_f. Nevertheless, the measurement error for the fault distance due to pre-fault load flow and the consideration of R_f is usually a lot more decisive for this use case.

- **Impact of the SSSC on branch BC1:** A severe influence of the SSSC on the measurable fault distance in branch BC1 is not given. As expected, since the SSSC is not in the fault loop measured by the relay, the impact is minimal leading to the reliable detection of the fault distance by a protection device in branch BC1. This fact can be used for implementing teleprotection schemes that enable reliable protection in case of a bypass failure.

- **Impact of the SSSC on branch CB1:** Branch CB1 is, as expected, influenced the most by the SSSC. The maximum influence occurs for L-G fault with a high fault resistance. The least influence is given by three-phase short circuits. The maximum relative error of the SSSC is given for the L-G fault with R_f = 10 Ω, with about ±15 %.

- **Impact of the SSSC on branches AB and DC:** An impact on the measured fault impedance by the branches in SS A and SS D is given with a maximum of about ±3 to 3.2 %. This is not assessed severe, due to the long distance between the impedance measurement and the actual fault location.

- **Impact of the SSSCs operation mode:** The impact of the SSSC also depends on the operation mode. In general, the impact increases with decreasing current of the SSSC. The current for inductive operation is, under identical boundaries, smaller than for capacitive operation. Therefore, the impact of the SSSC for inductive operation is a little higher than for capacitive operation.

- **Impact of the fault distance:** Since the fault current decrease for more distant faults, it is evident that the impact of the SSSC on the fault impedance increases for faults at the end of the line.

- **Impact of the fault type:** The impact of the fault type is indirectly given by the fault current level. In general, the highest current is expected for the three-phase fault, while the least fault current is expected for the L-G fault. Therefore, the highest impact can occur for the L-G fault, while the impact decreases for the L-L and three-phase fault.

5 Environment for ProtHIL Tests

This section summarises the environment developed for executing ProtHIL Tests. Used for these tests is a DSpace real-time simulator (RTS), coupled with an Omicron amplifier and two protection devices, the Schneider P433 and Siemens 7UT85.

5.1 Topology for the Hardware-In-the-Loop Tests

Regarding the physical setup of the ProtHIL environment, an exemplary overview is given in Figure 76. The following components were used:

- **DSpace DS6001:** processor board for simulating the short-circuits in real-time with frequency of 10 kHz (configuration with DSpace ConfigurationDesk and DSpace ControlDesk)
- **DSpace DS6101:** interface board for controlling the Omicron CMS 156
- **DSpace DS2655:** FPGA board for processing the input signals of the protection devices
- **DSpace DS2655M1:** interface board for the input signals of the protection devices
- **Omicron CMS 156:** amplifier acting as a real-time interface between the short-circuit simulation and the real protection devices
- **Schneider P433:** distance protection relay (configuration with Easergy Studio)
- **Siemens 7UT85:** transformer differential protection relay with an implemented distance protection function group (configuration with DIGSI5)

The circuit breaker of branch CB1 is controlled by the real protection devices. The circuit breaker of branch BC1 is controlled automatically. It opens 60 ms after the start of the fault. For the upcoming tests, the fault distance on line BC is again chosen between 1 and 99 %. The operating time of circuit breaker CB1 is considered with 50 ms.

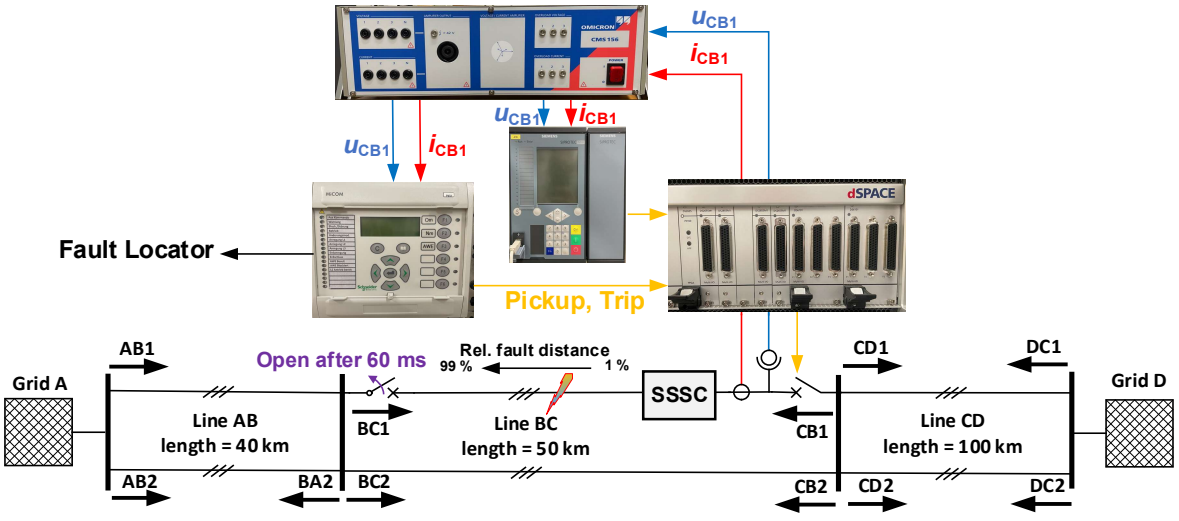


Figure 76: Topology for ProtHIL testing

5.2 Implementation of the Simulink Model onto a DSpace RTS

For the ProtHIL tests, the use case as defined in section 4.3 is implemented on the DSpace RTS. In the first approach, an attempt was made to implement the entire model consisting of the grids, lines and the SSSC inclusive its control on one CPU core. This was the first approach, because it is the easiest to implement on the RTS. Figure 77 illustrates this approach.

Implementation was successful, but leading to the problem of a too high task turnaround time. The task turnaround time is the time needed for the CPU to solve all equations before the next time step approaches. With calculating the system in real-time with 10 kHz, this leads to a step time of 100 µs. Therefore, the task turnaround time also needs to be below 100 µs. Otherwise, the calculation would not be in real-time anymore. With this approach, the task turnaround time was above 100 µs, leading to alternative approaches for implementing the model on the RTS.

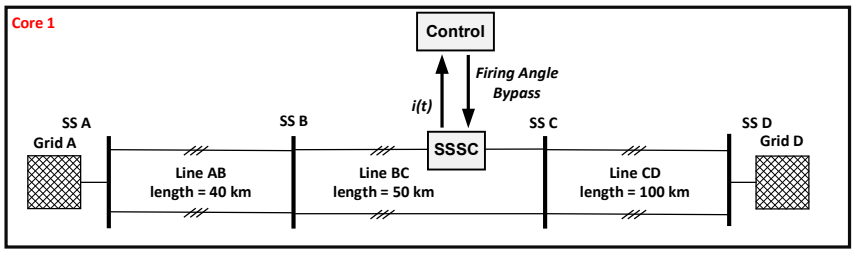


Figure 77: Grid and SSSC implemented on one CPU core

In the second approach, it was tried to implement the model described in the previous section on four CPU cores. This is illustrated in Figure 78. For the interaction of the cores, the Ideal Transformation Method (ITM) is used [18]. This method is widely used for parallel RTS simulations as well as for Power Hardware In the Loop (PHIL). With ITM, the multiple cores are connected via ideal voltage and current sources, controlled by exchanging voltages and currents between them. One challenge with ITM is the time delay for data exchange between the individual cores. The delay is caused by the simulation step of 100 µs. This delay can lead to the occurrence of instabilities, which was the case for this approach. There are solutions available that can avoid these instability issues [18]. Due to the scope and timeline of this thesis, it was decided not to implement these solutions, but to find a different approach for the implementation of the model onto the RTS.

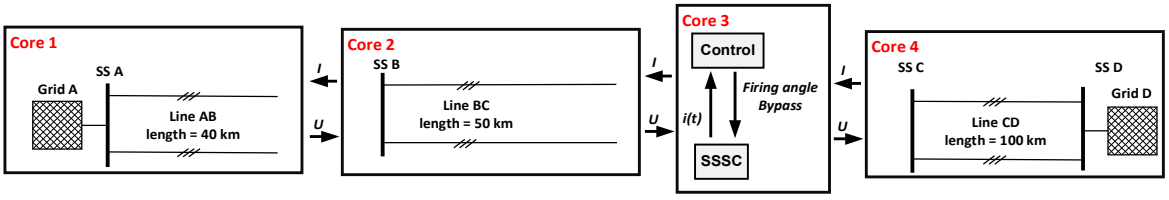


Figure 78: Multicore application with the Simulink model separated on all four cores

The final approach for the implementation of the model onto the DSpace RTS is illustrated in Figure 79. With this implementation, no voltage or current sources that could lead to instabilities are included, leading to a sufficient and stable method for simulating the short-circuits in real-time on the RTS.

The model consists of the grids A and B, all lines and the voltage source of the SSSC are implemented on one core of the RTS. Only the controller of the SSSC was outsourced to a second core. In order to additionally reduce the task turnaround time, the capacitive coupling of the double lines was neglected. With this approach, and neglected capacitive coupling, the task turnaround time of Core 1 and Core 2 was reduced to 50 µs. With this implementation method, the real-time simulation tests were able to be executed with 10 kHz.

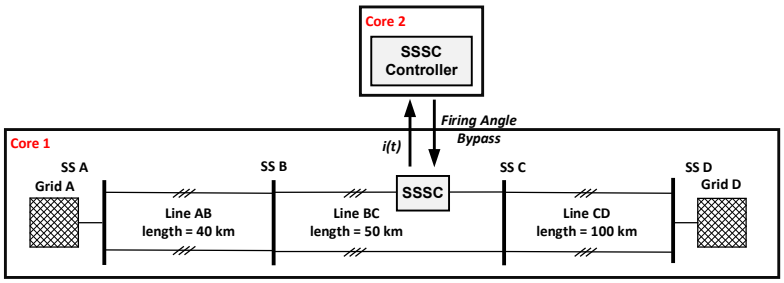


Figure 79: Final solution for real-time simulation

5.3 Parametrisation of Distance Protection Devices and Bypass Configuration

For the following ProtHIL tests, the protection devices were placed in branches CB1 and CB2. Due to the measured error from the missing functionality of mutual compensation, only L-L faults on line CB with $R_f \approx 0\ \Omega$ is considered for ProtHIL tests. For this set of scenarios, the minimal short-current is about 1500 A at the considered branches. The overall pickup current setting I_{pickup} was therefore chosen with 1300 A. The reach of zone 1 of each protection device was chosen with 85 % of line BC's positive-sequence reactance, which is equal to $X1_{Relay} = 17\ \Omega$. For $R1_{Relay}$, a value of $5\ \Omega$ was chosen. As mentioned in section 2.3.1, it is of high relevance to coordinate the bypass threshold value I_{SC} of the SSSC with the pickup current I_{pickup} of the distance protection relay. Ideally, as soon as the distance relay picks up, the SSSC is already bypassed. This can be guaranteed for $I_{SC} < I_{pickup}$. To implement this, it is suggested that I_{SC} of the SSSC should be chosen within the bypass threshold area, marked red in Figure 80. This ensures that the bypass is activated correctly. Therefore, the threshold value was chosen with $I_{SC} = 1100$ A. Regarding the impact of voltage inversion on the direction detection, only protection device P433 was used, as for this device, the threshold for using memorised voltages for direction detection can be controlled. This was mandatory to investigate the impact of memorised voltages for direction detection.

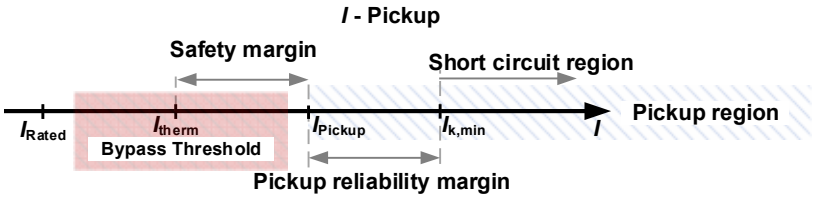


Figure 80: Coordination of the instantaneous current threshold of the SSSC with the overcurrent pickup of distance protection based on Figure 4

6 Investigation of the SSSC in ProtHIL Tests

This section deals with the documentation of the ProtHIL tests executed to investigate the impact of a SSSC on real protection devices. Section 6.1 investigates the impact of the SSSC on the fault locator for the automatic and the deactivated bypass. Section 6.2 examines the dynamic of the bypass on the shifting faults into wrong impedance zones for over- and underreach. Section 6.3 deals with the effect of voltage inversion and the use of memorised voltage.

6.1 Varying the Fault Distance along Line BC

Figure 76 visualises the setup for the following tests. For this investigation, L-L faults are simulated on line BC with the fault distance varying between 1 and 99 %. The protection device is placed in branch CB1 and trips its related circuit breaker inside the simulation (see Figure 76). The circuit breaker of BC1 is controlled automatically and trips 60 ms after the fault starts. The fault distance output by the fault locator of the protection device P433 is noted.

6.1.1 Impact of SSSC on Fault Locator of P433 with $|\underline{U}_{inj}|$ = 1698 V for a L-L fault with $R_f \approx 0\ \Omega$ on Line BC

Figure 81 illustrates the result of the impact of the SSSC for capacitive and inductive operation on the fault locator of device P433. The left diagram shows the measured fault locator distance over the actual controlled fault locator distance in % for automatic control of the bypass. The right diagram illustrates the case for the deactivated bypass of the SSSC. The expectancies for this diagram are therefore set by the simulated results in Figure 68.

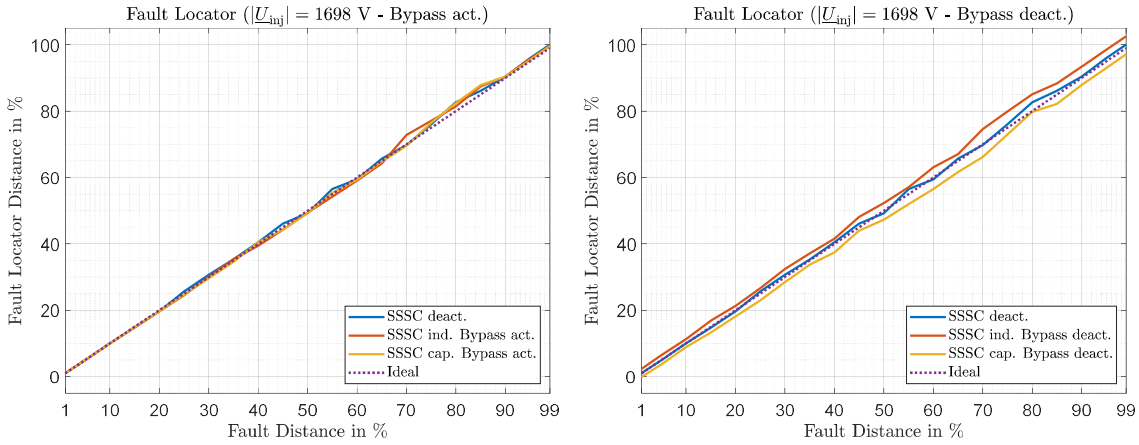


Figure 81: Measured fault distance by the fault locator of protection device P433 for the bypass of the SSSC being activated and deactivated (bypass failure) for $|\underline{U}_{inj}|$ = 1698 V

Expectancies for this measurement results are fulfilled considering the basic influence, that the fault distance is increased for the SSSC operating inductive and decreased for the SSSC operating capacitive.

Figure 82 illustrates the relative fault error (see (59)) of the fault locator for capacitive and inductive operation with and without the bypass of the SSSC activated. The reference distance for the calculation of the relative error is the actual fault distance that is controlled. Additionally, also the relative fault error for the SSSC being in monitoring mode is drawn, since this quantity is independent of the SSSC. It can be seen that the graphs vary significantly, which is explained with the uncertainty of the fault locator. The fault locator is an individual function of a protection device that calculates the fault distance in % based on the measured voltages and currents during a fault event.

The maximum relative error for the SSSC being in monitoring mode, as well as for the bypass being activated for capacitive and inductive operation, is around 2.5 %. Meanwhile, when comparing the graphs for bypass failure with the simulated results in Figure 66, it can be seen that the impact of the SSSC is slightly decreased for the real protection device. Nevertheless, a trend can be observed the impact of the SSSC increases with the fault distance also increasing.

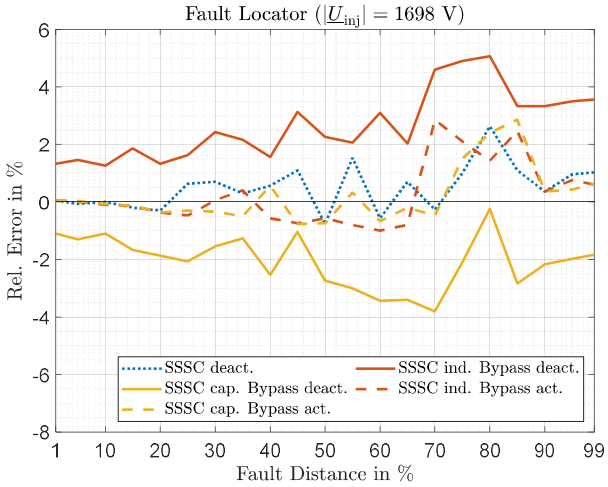


Figure 82: Relative error by fault locator for SSSC deactivated, inductive and capacitive and for bypass activated and deactivated for $|\underline{U}_{inj}|$ = 1698 V

6.1.2 Impact of SSSC on Fault Locator of P433 with $|\underline{U}_{inj}|$ = 8490 V for a L-L fault with $R_f \approx 0\ \Omega$ on Line BC

Figure 83 shows the impact of the SSSC on the fault locator of the P433 with an injected voltage of $|\underline{U}_{inj}|$ = 8490 V. The diagram on the left visualises the fault distance of the fault locator over the actual fault distance with the automatic bypass being activated for capacitive operation. The right diagram illustrates the impact of the SSSC for the bypass deactivated.

The diagram on the right fulfils expectancies regarding the operation mode of the SSSC and its influence on the fault locator. Surprisingly, the influence of the SSSC when operating capacitive is stronger, than for the SSSC operating inductive. This is better visualised in Figure 84.

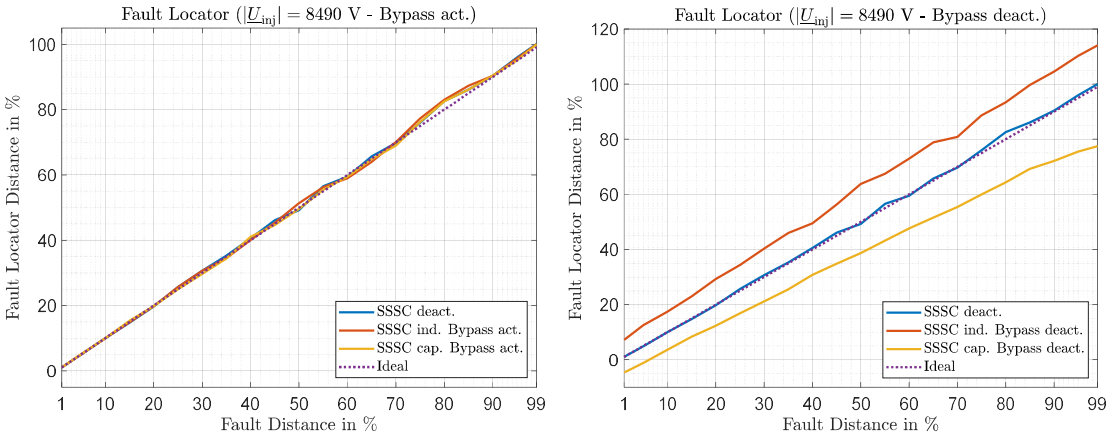


Figure 83: Measured fault distance by the fault locator of protection device P433 for the bypass of the SSSC being activated and deactivated (bypass failure) for $|\underline{U}_{inj}|$ = 8490 V

Regarding the scenarios with the bypass deactivated, can be seen that the maximum relative error during inductive operation occurs when the fault is at 99 % of the line with an error of about 15 %. Meanwhile, the maximum error for capacitive operation with deactivated bypass also occurs for the fault being at 99 % of the line with an error of about 22 %. In cases with the automatic bypass activated and the SSSC being deactivated, results again vary by approximately 2.5 %.

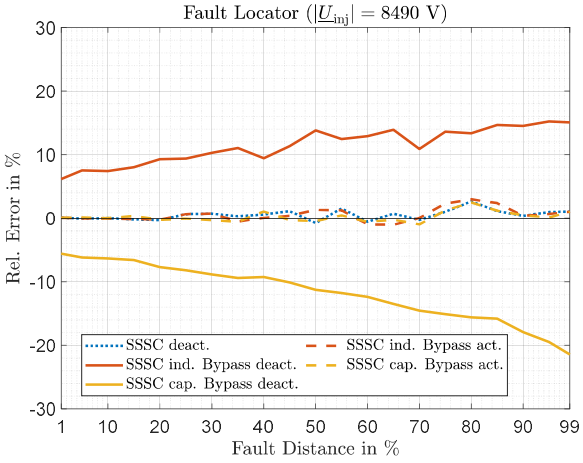


Figure 84: Relative error by fault locator for SSSC deactivated, inductive and capacitive and for bypass activated and deactivated for $|\underline{U}_{inj}|$ = 8490 V

6.1.3 Conclusion: Impact of SSSC on Fault Locator

The results of this chapter can be summarised as follows:

- The distance determination of the fault locator for $|\underline{U}_{inj}|$ = 1698 V lead to significantly varying results. A trend was never-the-less observable. The SSSC influences the fault distance determination of the protection device for up to 5 %.
- With $|\underline{U}_{inj}|$ = 8490 V, the fault locator was strongly influenced. The maximum relative error was given for capacitive operation with approximately -22 %.
- The automatic bypass decisively reduced the influence of the SSSC to no a non-measurable influence.

6.2 Impact of the Bypass Delay on Zone Shifting

The goal of this investigation is to test the impact of the bypass delay on the zone shifting, caused by the operation mode of the SSSC. In order to have clear and definite results, the injected voltage of the SSSC was set to $|\underline{U}_{inj}|$ = 8490 V.

6.2.1 Overreach with L-L Fault at 87 % of Line BC with $R_f \approx 0\ \Omega$ and SSSC operating in Capacitive Mode with $|\underline{U}_{inj}|$ = 8490 V

According to Figure 84, the capacitive influence of the SSSC for faults at approximately 85 % of the line is about –15 %. Zone 1 of the distance relays is set to 85 % of the line reactance. The fault location for this overreach scenario is set slightly beyond the reach so that the fault is reliably detected in zone 2 with the SSSC in monitoring mode. Considering the measurement uncertainty of the fault locator, which is about 2.5 %, it was possible to place the fault at 87 % of line BC, resulting in zone 2 trips only.

In the next step, the automatic bypass of the SSSC was deactivated and instead, the bypass was controlled manually. With the SSSC then operating in capacitive mode and $|\underline{U}_{inj}|$ = 8490 V, a bypass failure would lead to zone 1 trips. The bypass delay was then controlled manually starting from 0 ms and going to up to 50 ms. The 7UT85 and the P433 were then parametrised to use different output ports for whether a zone 1 or zone 2 trip occurred. This allowed measuring the influence of the bypass delay on the trip time. Results for this investigation are illustrated left for the 7UT85 and right for the P433 in Figure 85.

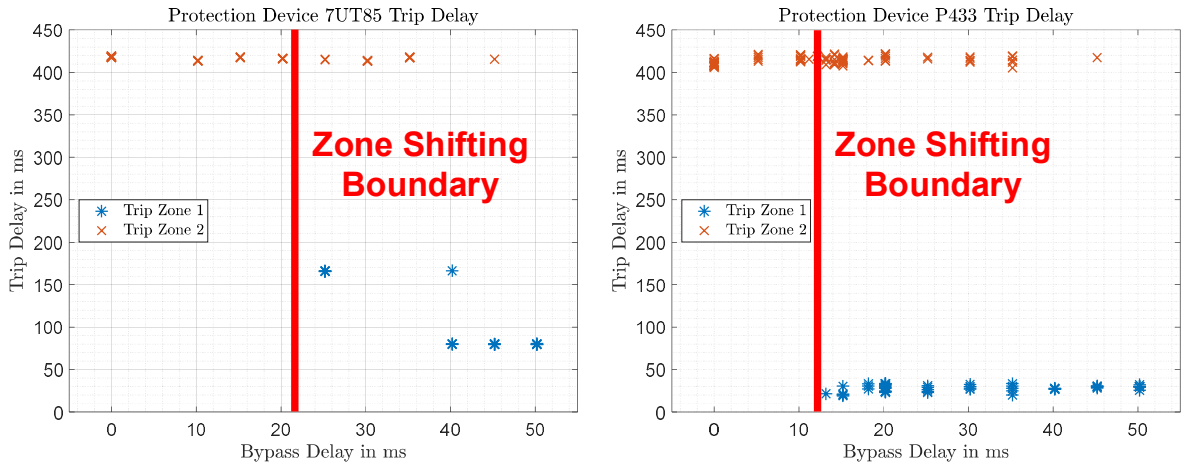


Figure 85: Zone shift from Z2 to Z1(overreach) in dependency of the bypass delay for 7UT85 (left) and P433 (right)

For the 7UT85 it can be observed that the first zone 1 trips occurred when the bypass delay was longer than approximately 20 ms. For the P433, the bypass needed to be faster than about 10 ms to prevent zone 1 trips. When the bypass exceeded 10 ms, both zone 1 and zone 2 trips occurred. With a bypass delay over 40 ms, only zone 1 trips were observed for both relays, except for one outlier at a 45 ms bypass delay.

For overreach, the bypass needs to act reliably and quickly, otherwise it is possible that the protection device trips the fault in zone 1 even though it should have tripped in zone 2. This directly affects the selectivity of the protection system. To mitigate the issue of a too slow bypass, a possible solution can be reducing the reach of zone 1. In addition, the use of teleprotection schemes (section 2.1.2.2) can also act as a fitting measure to overcome this [16,17].

In order to guarantee that the bypass acts fast enough, the pickup of the protection relays must be coordinated with the activation of the bypass.

6.2.2 Underreach with L-L Fault at 84 % of Line BC with $R_f \approx 0\ \Omega$ and SSSC operating in Inductive Mode with $|\underline{U}_{inj}| = 8490$ V

This section investigates the impact of the bypass delay on the occurrence of underreach. For this the fault location was placed at 84 % of the line, slightly below the reach of 85 %. With the fault at 84 % and the SSSC deactivated, only zone 1 trips occurred. The inductive impact of the SSSC for a fault at 84 % is, according to Figure 84, expected to be approximately 14 %. With the SSSC bypass being deactivated, zone 2 trips are expected. For this investigation, the bypass delay is again manually controlled, starting from 0 ms and going up to about 500 ms.

Figure 86 summarises the results of this investigation. For both relays it can be observed that a linear trend between the bypass delay and the trip delay of zone 1 trips is evident. This means, the longer the bypass needs to be active, the longer the influenced relay will not trip the fault in zone 1.

This linear trend can be clearly seen for the 7UT85. For the P433 it is observable that even with an increasing bypass delay, the protection device still detected outliner of fault cases in zone 1 and tripped immediately.

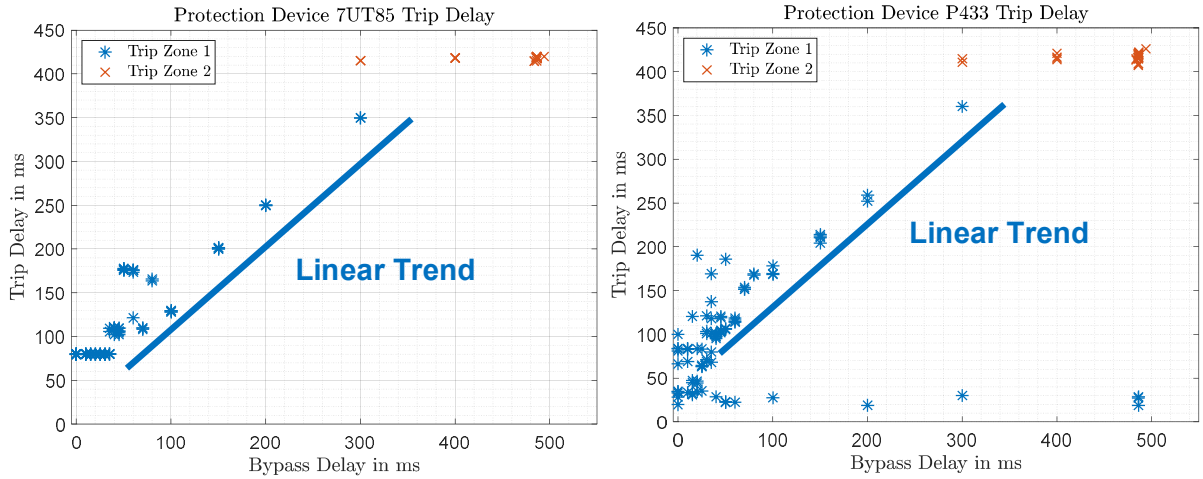


Figure 86: Zone shift from Z1 to Z2 (underreach) in dependency of bypass delay for 7UT85 (left) and for P433 (right)

The underreach is therefore assessed less severe than the overreach. This is because, while overreach with a too slow bypass can directly lead to an unselective trip, for underreach a too slow bypass will only delay the trip. Nevertheless, this needs also to be avoided and can be mitigated with the coordination

of the pickup mechanism of the protection relay with the bypass activation of the SSSC. For overcurrent pickup, this means that the short-circuit bypass threshold current must be chosen below the value of the pickup current of the protection device (Figure 80).

6.3 Voltage Inversion for Three-Phase Faults while SSSC operating Capacitive and $|\underline{U}_{inj}|$ = 8490 V

In this section, impact of using memorised voltages on direction detection and on bypass delay is investigated, regarding the effect of voltage inversion. For this, the fault distance is set to 1 % of line BC. According to Figure 61 and Figure 84, this will lead to voltage inversion, when the SSSC is operating capacitive with $|\underline{U}_{inj}|$ = 8490 V. To ensure that only the voltage memory is used for direction detection, a three-phase fault is simulated.

For the P433, a voltage threshold value U_{th} in % can be defined, below which the relay will use the memorised voltage for the fault direction detection. Starting from the original threshold value of 15 %, this value was then steadily reduced until a pickup in the wrong direction for a three-phase terminal short circuit with the bypass deactivated and the SSSC operating capacitive, occurred.

Figure 87, Figure 88 and Figure 89 illustrate the pickup and trip signals for U_{th} = 15 %, U_{th} = 10 % and U_{th} = 5 %. For these values of U_{th}, no wrong direction detection occurred. The bypass delay in the range of approximately 89 ms to 96 ms is explained by the trip of the relay P433. The fault clearing leads to the activation of the bypass, because with no current flowing, the SSSC cannot synchronise to a current space vector.

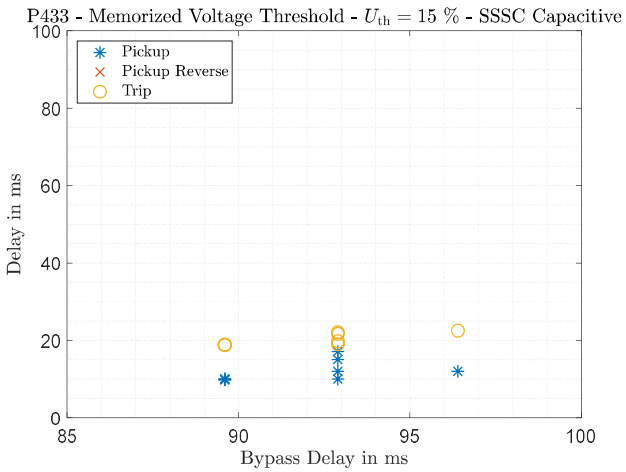


Figure 87: Pickup and trip signals for P433 for memorised voltage threshold U_{th} = 15 %

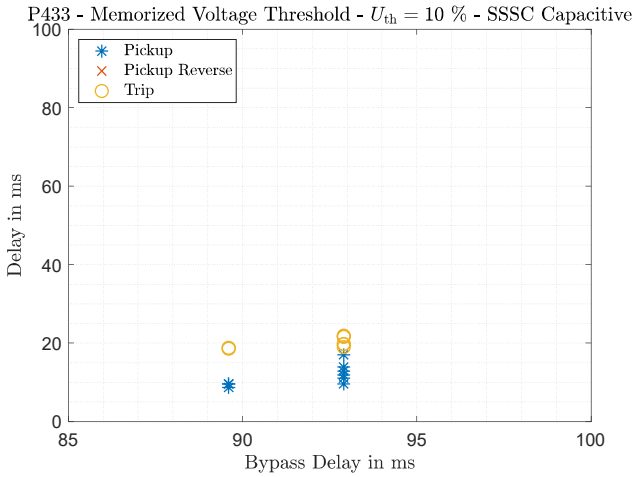


Figure 88: Pickup and trip signals for P433 for memorised voltage threshold U_{th} = 10 %

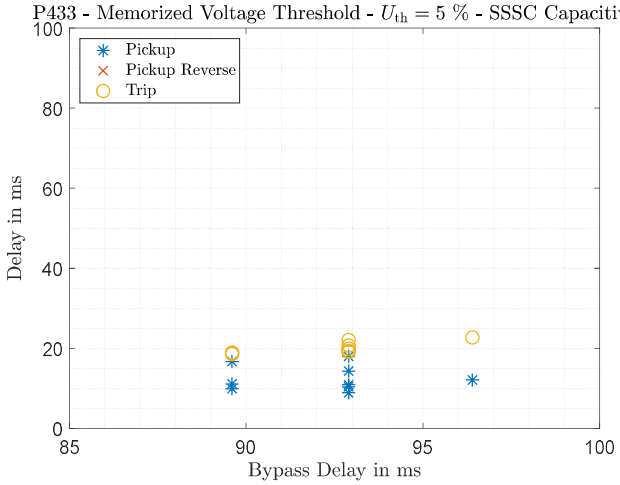


Figure 89: Pickup and trip signals for P433 for memorised voltage threshold U_{th} = 5 %

Finally, when choosing U_{th} = 4 %, reverse pickups occurred. This is illustrated in Figure 90. It can be observed that pickups in reverse direction occurred for the bypass delay being slower than approximately 50 ms. For the bypass acting faster than 50 ms, no pickup in reverse direction occurred. The relay picks up normally after about 10 to 15 ms and trips shortly afterwards.

For the bypass being slower than approximately 50 ms, all faults led to pickups in forward direction and trips in about max. 22 ms. In addition, also the reverse pickups occurred. These reverse pickups did occur about 70 ms after the fault start.

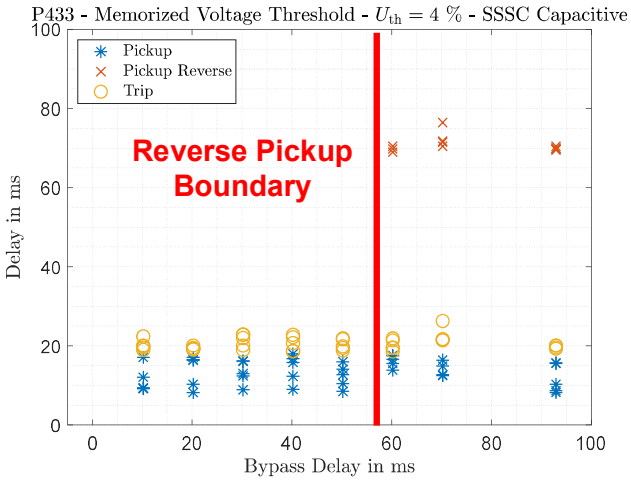


Figure 90: Pickup, pickup reverse and trip signals for P433 for memorised voltage threshold U_{th} = 4 % in dependency of the bypass delay

This is further illustrated in Figure 91, which exemplary visualises the signals for a scenario in which a pickup in reverse direction occurred additionally to the conventional pickup and trip signals.

It can be seen that the fault occurs at 0 ms. The pickup signal of the P433 occurs delayed at approximately 13 ms, shortly followed by a trip signal. After about 50 ms, the trip signal is revised. At about 70 ms, the pickup reverse signal is sent by the P433.

This result is not assessed as a severe issue, because the danger of a wrong fault direction detection can be mitigated by using the voltage memory. To ensure that this works reliably, the threshold value of the voltage memory should not be chosen too small. Additionally, even with pickups in the wrong direction occurring, the protection device tripped before the pickup in the wrong direction.

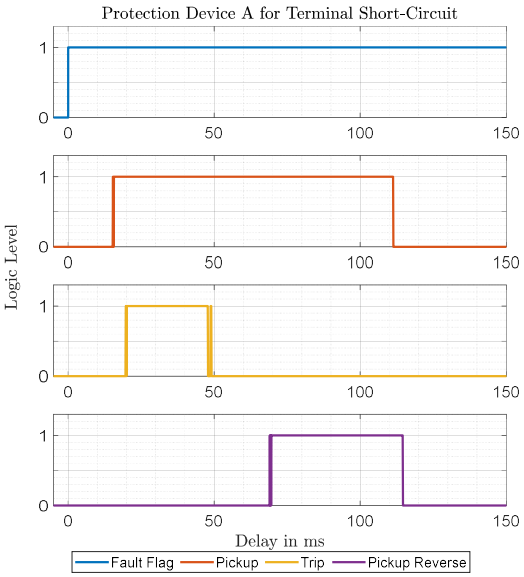


Figure 91: Pickup, pickup reverse and trip signals for P433 for memorised voltage threshold U_{th} = 4 %

In order to avoid zone shifting and wrong direction detection by influenced protection relays, the SSSC must bypass quicker than the protection device can recognize the fault. By choosing the instantaneous current threshold I_{SC} below the pickup current I_{pickup} of the protection device, this can be ensured. Figure

92 visualizes the speed of the protection relay pickup vs. the speed of the automatic bypass functions (SC and DC) for 39 measurements. SC is equal to the overcurrent bypass and DC is equal to the DC protection bypass activation. It can be seen that the given parametrisation ensures a fast bypass of the SSSC. This can also be seen in Figure 81 and Figure 83 (left).

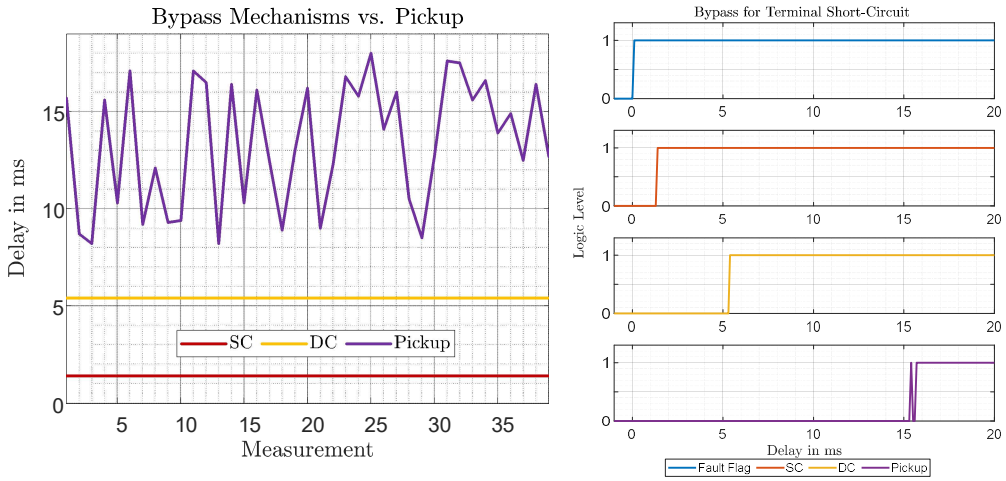


Figure 92: Automatic bypass speed vs. pickup speed of P433

6.4 Conclusion on ProtHIL tests

- **Fault Locator:** Only during bypass failure, the fault locator is measurably influenced by the SSSC. Depending on the operation mode, the distance is decreased for capacitive and increased for inductive mode. The resulting fault distance strays independent of the SSSC, which is explained by the fault locator function. As simulated in section 4.3.3, the impact of the SSSC for $|\underline{U}_{inj}|$ = 1698 V on the fault locator is not severe. For $|\underline{U}_{inj}|$ = 8490 V, the distance of the fault locator is affected by up to 22 %. For the bypass being enabled, no influence of the SSSC on the fault locator is detected

- **Overreach:** Overreach occurs for the SSSC operating capacitive and the fault being located slightly above the reach. For this scenario, a too slow bypass can lead to instantaneous trips in Z1. In order to avoid this, the bypass must be activated within 10 ms for the P433 and 20 ms for the 7UT85.

- **Underreach:** Underreach occurs for the SSSC operating inductive and the fault being located slightly below reach. For the SSSC pushing the fault into Z2, the bypass delay linearly affects the operating speed of the distance protection relay. As soon as the bypass activates, the measured fault distance is in Z1, leading to an instantaneous trip.

- **Fault direction detection:** The use of memorised voltages mitigates the influence of the SSSC on fault direction detection. The threshold value for the use of memorised voltages must not be chosen too small. With the memorised voltages being deactivated (by choosing a too small voltage threshold), reverse pickups can occur for terminal short-circuits.

7 Conclusion and Outlook

The goal of this thesis is to investigate the impact of SSSCs on distance protection relays. Additionally, the results of this investigation are used to develop a protection concept for the implementation of SSSCs into transmission grids. The analysis of this influence is done both analytically and through simulations, yielding the following results:

Grid Topologies

The results in section 4.1 show that the influence of the SSSC on measurable fault impedance strongly depends on the grid topology. Remote protection relays are not directly influenced by the SSSC. Using an additional branch after the SSSC excludes it from fault loops, which prevents any effect on distance protection relays.

Simplified Estimations with Lossless Short-Circuit Calculations and Bypass Failure

The results in section 4.2 analyse the influence of the SSSC on fault impedances in the case of bypass failure. It implies that only the unfortunate combination of very long and very short compensated lines lead to a severe impact of the SSSC on fault loop impedances. It is also evident that decreasing short-circuit currents increase the influence of the SSSC. Voltage inversion for capacitive operation mainly depends on the short-circuit power of the grid and occurs for terminal faults.

Investigation of a Use Case Scenario for Bypass Failure

In section 4.3, offline simulations in Matlab / Simulink allowed a more detailed analysis of the impact of the SSSC for bypass failure. The influence of the SSSC increases with larger fault resistance as well as for more distant faults. For inductive operation, the influence is also greater than for capacitive operation. Generally, the impact is reduced for larger fault currents. The largest impact occurs for L-G faults, followed by L-L faults. The least influence is seen for three-phase short-circuits without fault resistance. For the use-case scenario, the influence of the SSSC under normal conditions, is assessed as not severe.

Bypass Speed

In section 6, ProtHIL tests were used to investigate the dynamic behaviour of the bypass on real protection devices. The speed of the bypass has a decisive impact on the zone shifting of the SSSC. Overreach is strongly affected by a slow bypass, while underreach is a less severe scenario. The voltage memory has a decisive impact on reliable fault direction detection, and the activation threshold should not be set too low to ensure reliable fault direction detection. Setting the instantaneous short-circuit threshold of the bypass below the protection device’s pickup current ensures that the bypass is active before the protection device is influenced by the SSSC.

Suggested Protection Concept

Regarding these results, the following protection concepts are suggested:

- **Teleprotection (section 2.1.2.2):** The fact, that the remote distance protection relay is unaffected by the SSSC can be advantageous. Therefore, using underreach schemes could be a suitable solution. Since the direction detection of the influenced device, when using memorised voltages, is unaffected, a permissive overreach scheme with directional comparison may also be appropriate. When using schemes with the overreach zone of the influenced protection relay, the zone boundary of Z1B should be set above the maximum expected zone shifting by the SSSC. These measures can adress the zone shifting issue caused by the SSSC in the event of bypass failure.

- **Coordination of the bypass activation with the protection pickup:** Additional bypass criteria can ensure that protection relays are not influenced by the SSSC. Choosing the instantaneous overcurrent threshold below the overcurrent pickup value of the protection relay is mandatory but only guarantees a fast enough bypass activation for the overcurrent pickup. This is not the case for different pickup mechanisms. To ensure the reliable activation of the bypass, the SSSC should have all pickup functionalities of the corresponding protection relay. Additionally, corresponding bypass threshold values need to be set below the values of the protection device. This enables that the SSSC bypasses before the protection relay for all pickup mechanisms. Alternatively, an additional communication channel between the SSSC and the protection relay could ensure this as well. This can be analog, or also digital (e.g. IEC 61850). The DC protection mechanism enhances safety for the bypass activation of the SSSC.

Further Investigations

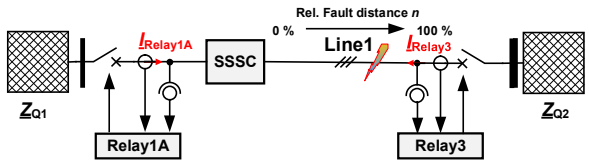
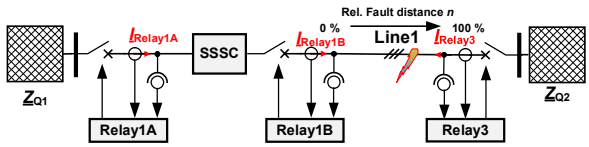
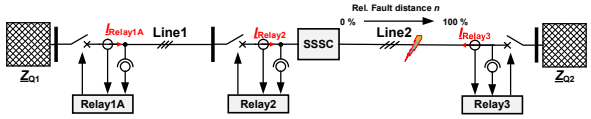
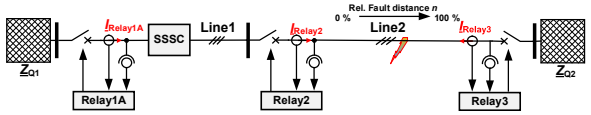
It is recommended to further investigate the following key points:

- Implementation and testing of teleprotection schemes with SSSCs
- Development of guidelines to ensure reliable protection with SSSCs
- Expansion of the SSSC model to include the submodules and the DC link controller for more detailed modulation of the DC section
- Investigation of the dynamic behaviour of the SSSC regarding synchronisation and control

8 Appendix

8.1 Summary Topologies

Table 12: Overview of investigated topologies for analysing the influence of the SSSC on distance protection relays in section 4.1

	Impact	Relay1A	Relay1B	Relay2	Relay3
Topology 1 	Zone Shifting	X	-	-	-
	Voltage Inversion	X	-	-	-
	No Direct Influence	-	X	-	-
Topology 2 	Zone Shifting	X	-	-	-
	Voltage Inversion	X	-	-	-
	No Direct Influence	-	X	X	-
Topology 3 	Zone Shifting	X	-	X	-
	Voltage Inversion	-	-	X	-
	No Direct Influence	-	-	-	X
Topology 4 	Zone Shifting	X	-	-	-
	Voltage Inversion	X	-	-	-
	No Direct Influence	-	-	X	X

8.2 Short-Circuit Verification Results

The following tables summarise the verification calculations and simulations. They show the absolute value of the complex phasor of the RMS of the fundamental of the faulty phase (L1 for L-G and L-L-L; L2 for L-L). Case distinctions are made for the SSSC being deactivated, operating inductive or capacitive. Branches “A” and “B” correspond with the currents of grid A or grid B, “IF” indicates the fault current.

8.2.1 L-G Faults with R_f = 5 Ω at 30 % of Line

Table 13: Grid Verification Results for a L-G fault on line AB at fault distance 30 %

L-G AB 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel.
Branch	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	Error
	A	A	A	A	A	A	%
AB1	7041.88	7040.89	7042.70	6976.83	6975.42	6978.10	0.92
AB2	812.88	816.59	808.99	798.47	802.10	794.66	1.77
BA1	1943.88	1936.81	1951.00	1944.40	1935.75	1953.19	0.11
BA2	812.88	816.59	808.99	802.95	806.67	799.06	1.21
BC1	642.82	605.23	680.17	654.19	606.89	701.58	3.15
BC2	642.82	668.71	617.34	654.24	686.22	622.42	2.62
CB1	642.82	605.23	680.17	643.06	595.81	690.38	1.50
CB2	642.82	668.71	617.34	643.10	675.10	611.26	0.96
CD1	642.82	636.93	648.69	643.07	635.42	650.78	0.32
CD2	642.82	636.93	648.69	643.09	635.45	650.81	0.33
DC1	642.82	636.93	648.69	610.52	602.79	618.33	4.68
DC2	642.82	636.93	648.69	610.55	602.82	618.36	4.68
A	7820.23	7823.61	7816.55	7734.02	7737.56	7730.17	1.10
B	1285.65	1273.86	1297.39	1221.07	1205.61	1236.69	4.68
IF	8960.42	8952.60	8968.17	8899.53	8890.06	8909.03	0.66

Table 14: Grid Verification Results for a L-G fault on line BC at fault distance 30 %

L-G BC 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel.
Branch	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	Error
	A	A	A	A	A	A	%
AB1	2073.13	2071.68	2074.50	2040.56	2038.73	2042.26	1.55
AB2	2073.13	2071.68	2074.50	2040.90	2039.06	2042.59	1.54
BA1	2073.13	2071.68	2074.50	2054.13	2052.33	2055.79	0.90
BA2	2073.13	2071.68	2074.50	2054.48	2052.68	2056.15	0.88
BC1	4058.76	4087.02	4030.13	4028.43	4058.21	3998.41	0.70
BC2	303.71	300.70	310.98	310.62	308.26	316.59	2.51
CB1	1682.54	1632.59	1732.38	1676.91	1624.45	1729.55	0.16
CB2	303.71	300.70	310.98	305.12	301.86	312.01	0.46
CD1	854.19	845.12	863.18	852.97	843.31	862.71	0.05
CD2	854.19	845.12	863.18	853.00	843.34	862.74	0.05
DC1	854.19	845.12	863.18	823.19	813.37	833.10	3.48
DC2	854.19	845.12	863.18	823.22	813.40	833.13	3.48
A	4146.26	4143.36	4149.00	4081.46	4077.79	4084.85	1.55
B	1708.39	1690.23	1726.36	1646.42	1626.78	1666.23	3.48
IF	5703.59	5681.59	5725.47	5671.91	5649.50	5694.32	0.54

Table 15: Grid Verification Results for a L-G fault on line CD at fault distance 30 %

L-G CD 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel.
Branch	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	Error
	A	A	A	A	A	A	%
AB1	1055.39	1046.83	1063.90	1025.34	1015.55	1034.99	2.72
AB2	1055.39	1046.83	1063.90	1025.53	1015.74	1035.18	2.70
BA1	1055.39	1046.83	1063.90	1043.00	1033.31	1052.56	1.07
BA2	1055.39	1046.83	1063.90	1043.21	1033.52	1052.77	1.05
BC1	1055.39	1010.71	1099.98	1043.06	995.51	1090.39	0.87
BC2	1055.39	1082.95	1027.84	1043.15	1071.40	1015.03	1.07
CB1	1055.39	1010.71	1099.98	1053.18	1005.89	1100.26	0.02
CB2	1055.39	1082.95	1027.84	1053.28	1081.48	1025.21	0.13
CD1	2665.32	2653.44	2677.00	2657.01	2644.63	2669.18	0.29
CD2	718.77	721.62	716.07	716.41	718.55	714.45	0.23
DC1	2072.92	2074.06	2071.77	2040.56	2041.85	2039.35	1.55
DC2	718.77	721.62	716.07	688.25	690.44	686.24	4.17
A	2110.79	2093.65	2127.80	2050.86	2031.29	2070.18	2.71
B	2765.18	2769.90	2760.56	2702.40	2706.99	2698.05	2.26
IF	4691.66	4681.62	4701.41	4670.17	4660.42	4679.78	0.45

8.2.2 L-L Faults with R_f = 5 Ω at 30 % of Line

Table 16: Grid Verification Results for a L-L fault on line AB at fault distance 30 %

L-L AB 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel. Error
Branch	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	
	A	A	A	A	A	A	%
AB1	9894.01	9889.72	9898.20	9855.44	9849.98	9860.91	0.38
AB2	1093.73	1098.73	1088.68	1094.98	1100.51	1089.46	0.16
BA1	2702.18	2693.03	2711.32	2696.42	2686.13	2706.70	0.17
BA2	1093.73	1098.73	1088.68	1091.56	1097.10	1086.02	0.15
BC1	826.47	791.20	861.65	829.54	784.25	874.94	1.54
BC2	826.47	847.65	805.37	829.63	859.63	799.69	1.41
CB1	826.47	791.20	861.65	825.48	780.07	870.98	1.08
CB2	826.47	847.65	805.37	825.57	855.64	795.53	0.94
CD1	826.47	819.41	833.49	825.50	817.80	833.20	0.04
CD2	826.47	819.41	833.49	825.55	817.85	833.25	0.03
DC1	826.47	819.41	833.49	809.92	802.03	817.80	1.88
DC2	826.47	819.41	833.49	809.96	802.07	817.84	1.88
A	10977.99	10978.80	10977.05	10936.21	10936.35	10936.08	0.37
B	1652.94	1638.82	1666.99	1619.88	1604.11	1635.64	1.88
IF_L2	12589.19	12575.76	12602.53	12539.33	12523.53	12555.11	0.38
IF_L3	12589.19	12575.76	12602.53	12539.04	12523.24	12554.82	0.38

Table 17: Grid Verification Results for a L-L fault on line BC at fault distance 30 %

L-L BC 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel. Error
Branch	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	|$\underline{I}$| (SSSC deact.)	|$\underline{I}$| (SSSC ind.)	|$\underline{I}$| (SSSC cap.)	
	A	A	A	A	A	A	%
AB1	3048.70	3044.33	3053.02	3039.43	3032.97	3045.86	0.23
AB2	3048.70	3044.33	3053.02	3039.99	3033.54	3046.43	0.22
BA1	3048.70	3044.33	3053.02	3044.47	3038.06	3050.87	0.07
BA2	3048.70	3044.33	3053.02	3045.07	3038.65	3051.47	0.05
BC1	5941.33	5958.63	5923.92	5934.08	5952.87	5915.25	0.10
BC2	246.79	230.45	265.04	259.25	241.00	280.46	5.82
CB1	2344.10	2294.38	2393.72	2344.18	2288.62	2399.57	0.24
CB2	246.79	230.45	265.04	247.64	228.44	269.73	1.77
CD1	1112.49	1100.76	1124.17	1113.12	1101.27	1124.91	0.07
CD2	1112.49	1100.76	1124.17	1113.19	1101.34	1124.98	0.07
DC1	1112.49	1100.76	1124.17	1097.51	1085.37	1109.60	1.30
DC2	1112.49	1100.76	1124.17	1097.57	1085.43	1109.66	1.29
A	6097.40	6088.67	6106.04	6079.42	6066.51	6092.29	0.23
B	2224.99	2201.51	2248.35	2195.08	2170.80	2219.26	1.29
IF_L2	8273.68	8240.59	8306.60	8264.30	8226.66	8301.82	0.06
IF_L3	8273.68	8240.59	8306.60	8264.01	8226.36	8301.52	0.06

Table 18: Grid Verification Results for a L-L fault on line CD at fault distance 30 %

L-L CD 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel. Error
Branch	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	
	A	A	A	A	A	A	%
AB1	1567.84	1556.21	1579.39	1555.41	1540.73	1570.03	0.59
AB2	1567.84	1556.21	1579.39	1555.69	1541.01	1570.32	0.57
BA1	1567.84	1556.21	1579.39	1565.94	1551.35	1580.47	0.07
BA2	1567.84	1556.21	1579.39	1566.25	1551.66	1580.79	0.09
BC1	1567.84	1517.61	1617.80	1566.02	1508.32	1623.50	0.35
BC2	1567.84	1594.86	1541.04	1566.17	1594.74	1537.82	0.01
CB1	1567.84	1517.61	1617.80	1570.41	1513.00	1627.60	0.61
CB2	1567.84	1594.86	1541.04	1570.57	1599.08	1542.29	0.26
CD1	3877.63	3860.68	3894.41	3882.71	3862.14	3903.15	0.22
CD2	814.64	819.50	809.88	815.30	822.09	808.65	0.32
DC1	2776.37	2777.39	2775.33	2765.48	2767.95	2763.02	0.34
DC2	814.64	819.50	809.88	793.17	800.13	786.33	2.36
A	3135.68	3112.43	3158.78	3111.10	3081.74	3140.35	0.58
B	3575.25	3581.66	3568.92	3545.92	3555.88	3536.05	0.72
IF_L2	6634.29	6618.73	6649.65	6634.65	6616.91	6652.21	0.04
IF_L3	6634.29	6618.73	6649.65	6634.35	6616.61	6651.91	0.03

8.2.3 L-L-L Faults with R_f = 5 Ω at 30 % of Line

Table 19: Grid Verification Results for a L-L-L fault on line AB at fault distance 30 %

L-L-L AB 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel. Error
Branch	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	
	A	A	A	A	A	A	%
AB1	9891.86	9890.50	9893.29	9828.30	9826.99	9829.49	0.64
AB2	1037.27	1044.73	1029.84	1025.82	1033.13	1018.41	1.10
BA1	2805.67	2793.92	2817.44	2803.02	2791.42	2814.62	0.09
BA2	1037.27	1044.73	1029.84	1028.03	1035.38	1020.59	0.89
BC1	923.91	873.55	974.51	932.14	882.43	981.75	1.02
BC2	923.91	955.13	892.66	932.24	963.11	901.60	1.00
CB1	923.91	873.55	974.51	923.70	873.97	973.33	0.05
CB2	923.91	955.13	892.66	923.80	954.71	893.11	0.05
CD1	923.91	914.30	933.55	923.73	914.28	933.15	0.00
CD2	923.91	914.30	933.55	923.78	914.33	933.20	0.00
DC1	923.91	914.30	933.55	897.76	888.15	907.35	2.81
DC2	923.91	914.30	933.55	897.80	888.19	907.39	2.80
A	10909.11	10915.51	10902.78	10828.85	10835.22	10822.30	0.74
B	1847.82	1828.60	1867.10	1795.56	1776.34	1814.74	2.80
IF	12684.63	12671.55	12697.80	12618.51	12605.62	12631.31	0.52

Table 20: Grid Verification Results for a L-L-L fault on line BC at fault distance 30 %

L-L-L BC 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel. Error
Branch	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	
	A	A	A	A	A	A	%
AB1	3147.18	3144.36	3150.05	3121.62	3118.62	3124.54	0.81
AB2	3147.18	3144.36	3150.05	3122.21	3119.21	3125.13	0.79
BA1	3147.18	3144.36	3150.05	3132.48	3129.51	3135.36	0.47
BA2	3147.18	3144.36	3150.05	3133.09	3130.12	3135.97	0.45
BC1	6241.82	6268.87	6214.82	6219.77	6246.39	6193.01	0.35
BC2	263.15	256.17	273.60	273.34	268.63	281.98	4.86
CB1	2633.70	2575.24	2692.42	2631.74	2573.25	2689.96	0.07
CB2	263.15	256.17	273.60	264.80	259.29	274.29	1.22
CD1	1318.22	1305.37	1331.16	1318.65	1305.72	1331.47	0.03
CD2	1318.22	1305.37	1331.16	1318.73	1305.79	1331.54	0.04
DC1	1318.22	1305.37	1331.16	1293.97	1280.79	1307.02	1.81
DC2	1318.22	1305.37	1331.16	1294.04	1280.86	1307.09	1.81
A	6294.37	6288.72	6300.10	6243.83	6237.83	6249.66	0.80
B	2636.44	2610.73	2662.32	2588.00	2561.65	2614.11	1.81
IF	8857.15	8824.37	8890.09	8835.17	8802.15	8867.79	0.25

Table 21: Grid Verification Results for a L-L-L fault on line CD at fault distance 30 %

L-L-L CD 30 %	Short Circuit Calculation			Short Circuit Simulation			Max. Rel. Error
Branch	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	$\lvert \underline{I} \rvert$ (SSSC deact.)	$\lvert \underline{I} \rvert$ (SSSC ind.)	$\lvert \underline{I} \rvert$ (SSSC cap.)	
	A	A	A	A	A	A	%
AB1	1579.58	1567.29	1591.90	1552.70	1540.46	1564.91	1.70
AB2	1579.58	1567.29	1591.90	1552.99	1540.75	1565.20	1.68
BA1	1579.58	1567.29	1591.90	1569.70	1557.54	1581.84	0.62
BA2	1579.58	1567.29	1591.90	1570.01	1557.85	1582.15	0.60
BC1	1579.58	1526.52	1632.80	1569.78	1517.24	1622.32	0.61
BC2	1579.58	1608.11	1551.03	1569.94	1598.19	1541.71	0.60
CB1	1579.58	1526.52	1632.80	1579.28	1526.97	1631.61	0.03
CB2	1579.58	1608.11	1551.03	1579.45	1607.67	1551.25	0.01
CD1	4091.85	4074.29	4109.50	4091.05	4073.83	4108.21	0.01
CD2	1030.14	1035.42	1024.85	1030.85	1035.98	1025.74	0.09
DC1	3167.22	3168.71	3165.75	3145.18	3146.67	3143.66	0.70
DC2	1030.14	1035.42	1024.85	1003.09	1008.31	997.89	2.62
A	3159.16	3134.59	3183.79	3105.69	3081.21	3130.11	1.69
B	4180.63	4187.91	4173.34	4132.59	4139.81	4125.36	1.15
IF	7232.10	7216.51	7247.81	7223.44	7208.18	7238.61	0.12

9 Literature

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