Power Hardware-in-the-Loop test system.

Betreuer	Univ.-Prof. DI Dr.techn. Lothar Fickert
Vorgelegt von	Dr. techn. Dipl.-Ing. Ziqian Zhang, BSc

1 Comparative Study on Test Methods

The grid compatibility testing inspects the ability of the operation of DG systems under various grid environments. In order to determine whether the Equipment under Test (EUT), which are DG systems in this thesis, has the adequate grid compatibility, it is necessary to give the grid environment situation (excitation) to the EUT. According to the generation mode of the excitation, the testing can be divided into open loop test method and closed loop test method.

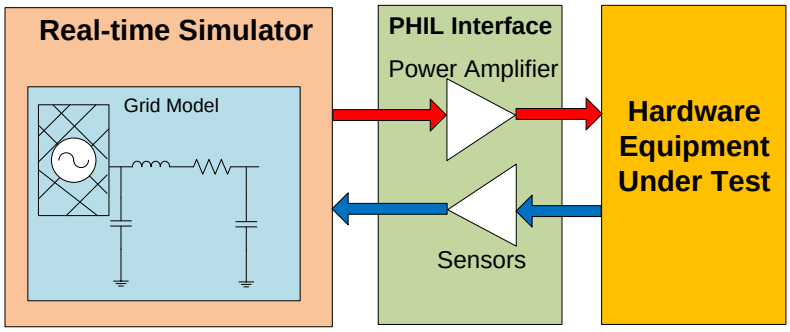
The open loop test method produces the pre-set grid environment situations and feeds into the EUT. The response of the EUT to this excitation is not allowed or not available to affect the following excitation. The test method of the present grid compatibility testing is the open loop test method.

The excitation from the closed loop test method is obtained from the simulation results. The response of the EUT is fed back to the test system, and then the resulting excitation will be affected. Such a test method forms a closed loop process, and is therefore called a closed loop test method. The closed loop test method contains the physical model simulation test method, the numerical model simulation test method, the Controller Hardware-in-the-Loop test method and the Power Hardware-in-the-Loop test method.

2 Power Hardware-in-the-Loop Test System

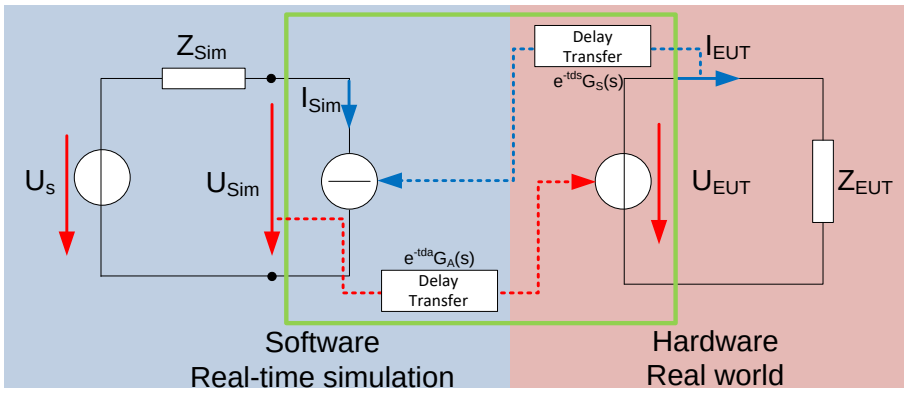
The Hardware-in-the-Loop (HIL) test system can give the EUT any realistic testing environment. The actual response of the EUT can be tested before the EUT goes into service. Some extreme test conditions can be easily reproduced in the HIL testing. This can save a lot of cost and reduce the risk of damage to the EUT. The operation of the HIL test is realized by the simulation model software in the real-time simulator, and the HIL interface, which is used to the information interchange or power exchange between the EUT and the simulation model software.

The EUT in case of a PHIL test system is the complete DG system. Since the signal and power exchange between the EUT and an RTS is through high-power signals, the PHIL interface is required. The PHIL interface is responsible for converting the power signal from the EUT to a low power signal for the RTS through the sensors, simultaneously converting the low power signal from RTS through the power amplifier to generate a high power signal for EUT.



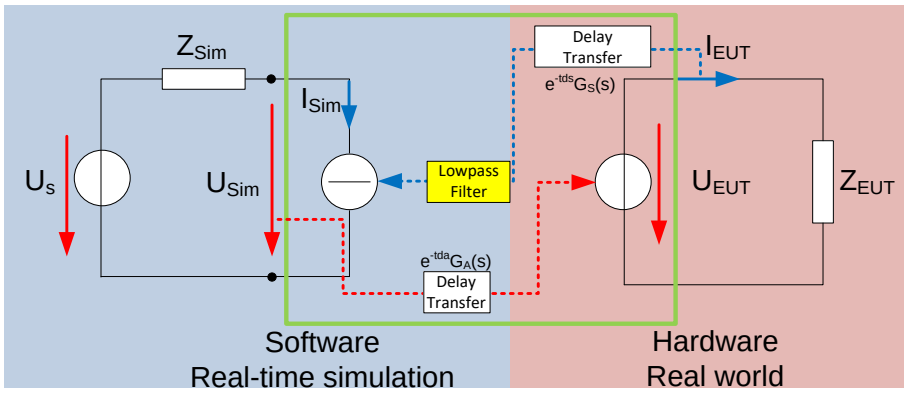
The PHIL interface algorithm is responsible for the interaction between the physical side (EUT) and the software side (numerical grid model) by the sensors and the power amplifier. The accuracy and stability problem of the system, which is caused by the limitation of the hardware of high power PHIL test system (such as delay, bandwidth, noise, etc.), can be improved by the suitable PHIL interface algorithm.

The most classical PHIL interface algorithm is Ideal Transformer Method (ITM). Because of its simple structure and clear principle, it has been widely used.



The accuracy and stability of the system are mainly affected by the delay of the system and the impedances. In order to improve the accuracy and stability of the system, the design and analysis of the compensation method for of Ideal Transformer Method will be carried out.

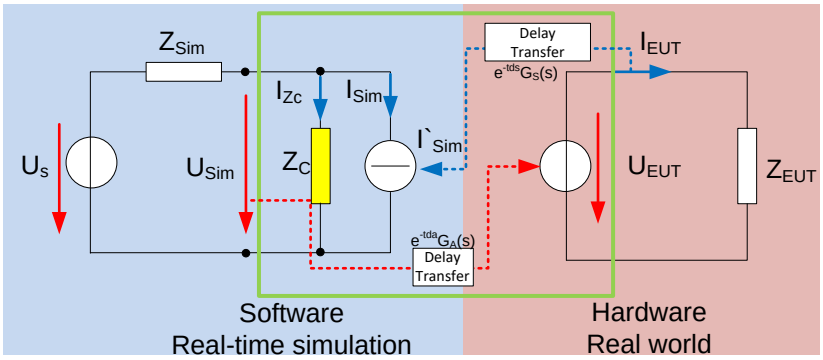
The relative error increases with the frequency. The relative error of ITM for high frequencies is very large, so it will seriously degrade the stability of the system. Therefore, a low pass filter can be added in the ITM to suppress the high frequency signal of the PHIL test system, in order to improve the stability of the system.



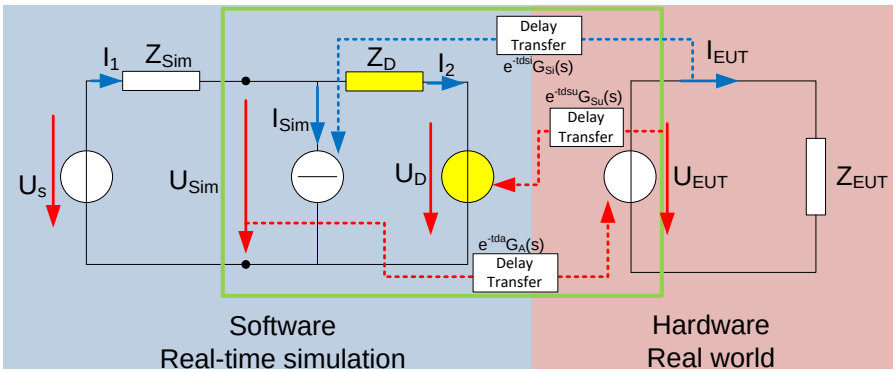
If the impedance of the software side Z_{Sim} is greater than the impedance of the hardware side Z_{EUT}, it will make the system unstable. So one can make the Z_{EUT} larger, or make the Z_{Sim}

smaller, to meet the stability criterion. The method of making the Z_{EUT} larger is that, connect an additionally series impedance in the hardware side. This method obviously changes the characteristics of the EUT. This will make the error in real-time simulation.

In this thesis, the Advanced Ideal Transformer Method (AITM) is presented. The basic principle is that, reduce the impedance on the software side by a parallel connected impedance Z_C, at the same time, the output signal of the controlled current source in software side is compensated, in order to keep the output of the software side U_{Sim} equal to normal Ideal Transformer Method.



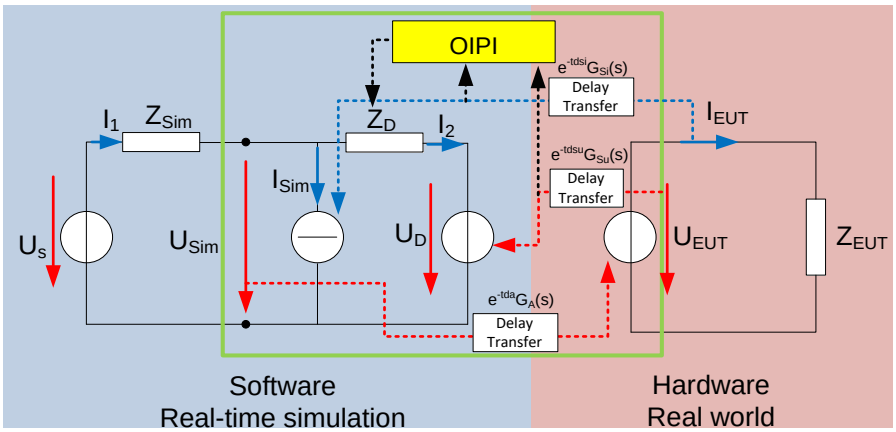
Based on the analysis of ITM, the delay and distortion of interaction between the software side and the hardware side can reduce the stability and accuracy of the system. In order to completely solve this problem, the modeling and simulation of the hardware side is carried out in the side software. In this way, the delay and distortion caused by the PHIL interface are eliminated.



The basic principle of the Damping Impedance Method (DIM) is that, on the software side, a damping impedance Z_D is used to simulate the impedance of the EUT Z_{EUT}, a controlled voltage source U_D is used to simulate the power amplifier U_{EUT}.

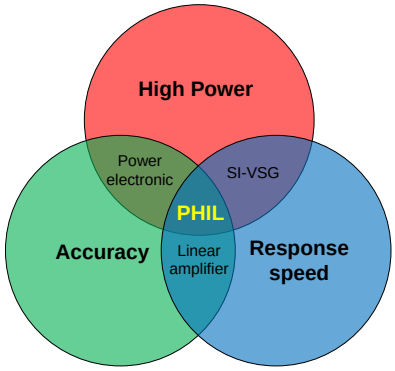
The stability performance of the system is optimal when the damping impedance Z_D exactly equal to the impedance of EUT Z_{EUT}.

The EUTs in this thesis are DG systems, which are composed of nonlinear components. Its output characteristic is related by the controller, so its impedance Z_{EUT} is a nonlinear piecewise function due to the control strategy of the DG system. The EUT is a black box for the PHIL test system. Therefore, its impedance cannot be predicted before the PHIL testing. In order to get the exact impedance parameter of the EUT during the PHIL test with Damping Impedance Method, an Online Impedance Parameter Identification (OIPI) is presented in this thesis.



3 High Power Amplifier

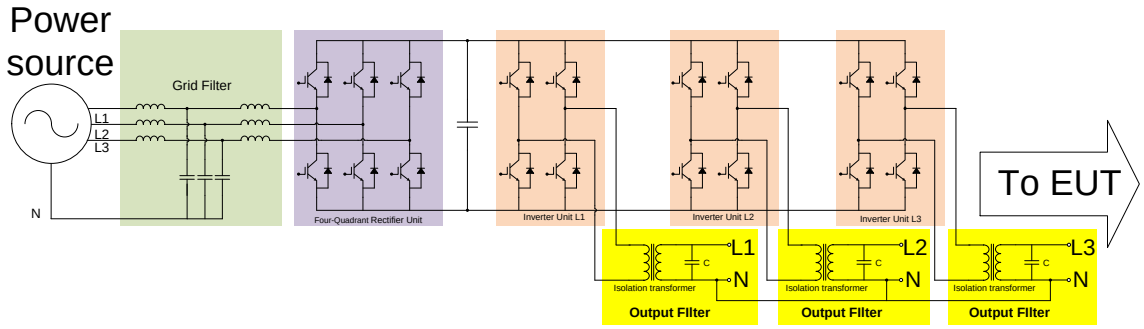
In a Power Hardware-in-the-Loop test system, the power amplifier is responsible for the transfer the calculated result of the grid model software from the real-time simulator to the hardware EUT. According to the system requirement analysis in chapter 3.6, the basic requirement of the power amplifier in high power class PHIL test system is high power, high accuracy and fast response speed. These three requirements are often contradictory.



During the grid compatibility testing of a DG systems, the DG system will transfer the power to the power amplifier. In order to save energy, four-quadrant rectifier is applied in the power amplifier, which provides the bi-directional energy transfer ability for the PHIL test system. The rated power of EUT in this thesis is 500 kVA, considering the variations of output power of EUT, the rated power of the four-quadrant rectifier is also 800 kVA.

Parameter Name	Value
Rated phase voltage U_N	400 V
Voltage range	0%-135% U_N
Rated frequency f_N	50/60 Hz
Frequency range	47 Hz – 63 Hz
Expected harmonic frequency range	<2000 Hz
Accuracy of voltage	<±0.3% U_N
Accuracy of frequency	<0.3% f_N
Response time	≤100 µs
THD (<50th)	<1%

The power amplifier is composed of a rectifier unit and the inverter units. The rectifier unit has a three-phase LCL filter and a three-phase four-quadrant rectifier. The inverter unit has three sets of independent single phase inverter units.



The PI regulator is equivalent to the system with one additional pole and one additional zero. The pole is located in the origin of the coordinates, and improves the steady performance of the system. The zero is located on the axis of the left half plane, improves the damping of the system.

But the PI regulator cannot follow the AC signal without steady-state error. In order to reduce this steady-state error, the integral coefficient has to be enlarged, but then the phase shift between the reference and the output is also increased. When the proportional coefficient is enlarged, this can cause a system oscillation. In the frequency domain, the PI regulator is equivalent to a low pass filter. The high frequency signal will be attenuated by the PI regulator. Hence the requirement for the operation bandwidth cannot be met. A new control strategy is needed, which can achieve the tracking of the AC signal without steady-state error, has a good dynamic performance, and meets the requirements of operation bandwidth.

Aiming at requirements above, the Proportional-Resonant (PR) regulator is presented:

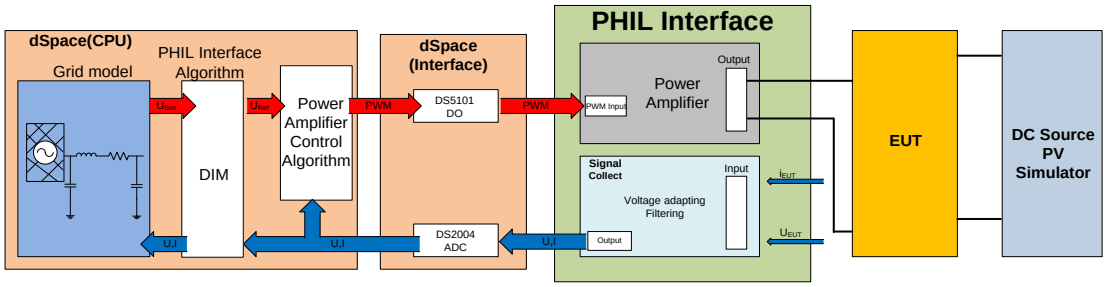
$$G_{PR}(s) = k_P + \frac{2k_R\omega_C s}{s^2 + 2\omega_C s + \omega_0^2}$$

An 800 kVA power amplifier of the PHIL test system is build. The rectifier unit contains of two sets of parallel connected three-phase four-quadrant rectifiers. The inverter unit contains of three sets of independent single-phase inverters. The photos of the power amplifier are shown in below.

It shows the front side and back side of the power amplifier, it contains eight cabinets. From left to right are: switchgear cabinet, rectifier cabinet 1 & 2, inverter cabinet 1, 2, 3 and the controller cabinet.

4 Power Hardware-in-the-Loop testing with Grid-connected Inverters

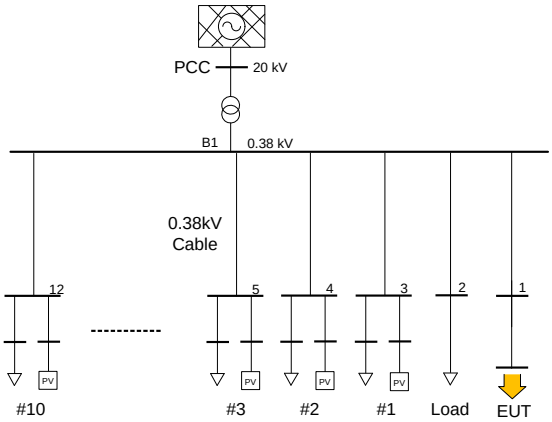
The complete PHIL test system is established based on the configuration. The DC port of the EUT is connected to the DC source, which is the PV simulator. The PV simulator corresponds to simulation the output of the photovoltaic array(s). Base on the grounds of the theoretical analysis in chapter 3 and the experiments results in chapter 6.2, the Damping Impedance Method is applied in the PHIL test system as PHIL interface algorithm.



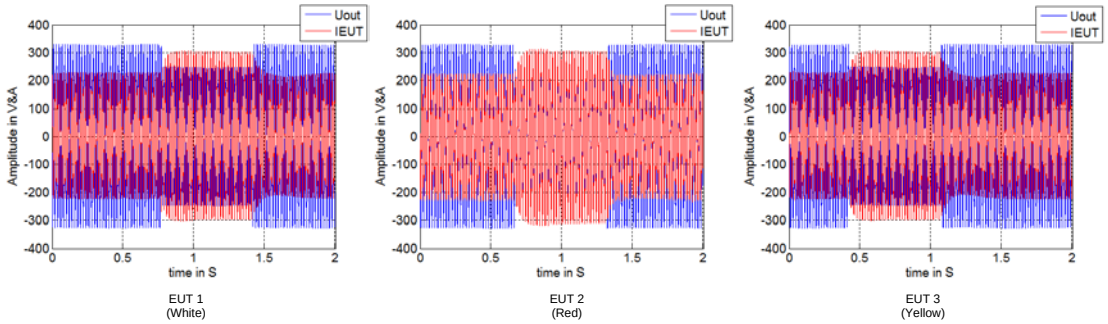
As EUTs in this chapter, the three different photovoltaic grid-connected inverters from three different producers are used. The rated power of all these EUT is all 4000 W, and the rated output voltage is 230 V_{RMS}. From left to right are the EUT1 (white), EUT2 (red) and EUT3 (yellow).

EUT 1 (White) | EUT 2 (Red) | EUT 3 (Yellow)

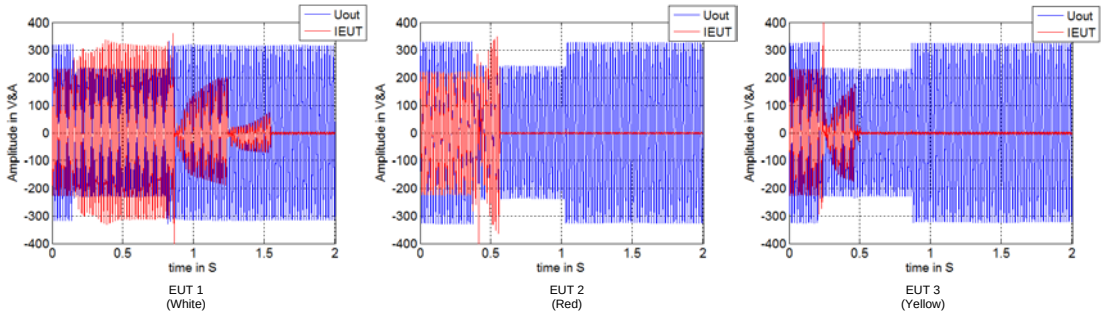
In order to reproduce a residential grid environment, where the photovoltaic grid-connected inverters are used, a grid model is built in dSpace, as shown in below.



Figures below show the LVRT testing results of the three different EUTs with 100% rated output power, the residual voltage of 0.75 p.u. and a duration of 625 ms.



LVRT testing of EUT1, 2 and 3 in 100% rated power with an ideal voltage source



LVRT testing of EUT1, 2 and 3 in 100% rated power with the PHIL test system

The output currents of the EUTs change all smoothly during the test, when the ideal voltage source is applied. So the EUT can easily pass the LVRT testing with ideal voltage source. It shows that the output currents of the EUTs change all dramatically during the test, when the PHIL test system is applied. And none of the EUT can pass the LVRT testing with the same testing condition, because the EUTs all shut down after or during the voltage dips.

Therefore, the ideal voltage source reduces the difficulty of the LVRT testing. The PHIL test system provides a real testing grid environment, which makes the LVRT testing more realistic.