# Power Hardware-in-the-Loop test system.

PHD Thesis

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Thanks to my parents for your support, words cannot express how grateful I am.

Finally, thanks to time, joy and misery.

I hope this paper will not be the end of academic thinking, but a new starting point.

**Abstract**

In the power systems more and more distributed generation systems are to be integrated. To ensure nevertheless the reliability grid operation with an increasing number of distributed generation systems, reliable testing and certification is required.

This thesis studies the difference between the conventional test methods and the real grid situation. Due to the unreality system impedances and the lack of the retroactive effects from the conventional test methods and test generator, the dynamic behaviors of the distributed generation systems during tests are different from the real grid situation. In order to realize the realistic testing grid environmental in the grid compatibility testing of distributed generation systems, this thesis presents a Power Hardware-in-the-Loop (PHIL) test method and, derived from this, a Power Hardware-in-the-Loop test system.

In this thesis, the operation sequence and various Power Hardware-in-the-Loop interface algorithms of the Power Hardware-in-the-Loop test system are analyzed in detail. The stability criteria and the optimized operation sequence of the Power Hardware-in-the-Loop test system are presented. On the basis of the existing Power Hardware-in-the-Loop interface algorithm, this thesis presents a new optimized Power Hardware-in-the-Loop interface algorithm with online impedance parameter identification and an additional phase compensation algorithm based on coordinate transformation in order to enhance the accuracy, stability and dynamic performance of the test system. Based on these researches, the performance requirements of the Power Hardware-in-the-Loop test system are given.

In this thesis, a universal equivalent simplified modeling method for distributed generation systems based on power electronic equipment and grid model is presented in order to keep the accuracy of real-time simulation and to reduce the computational complexity.

The power amplifier in the Power Hardware-in-the-Loop test system will be developed with the four-quadrant rectifier and three sets of single-phase inverters and a Proportional-Resonant regulator in order to meet the requirements of accuracy, response speed and operation bandwidth in the high power PHIL test system.

Finally, a complete Power Hardware-in-the-Loop test system has been built in the laboratory. The function of the PHIL test system is verified by a set of Power Hardware-in-the-Loop tests for distributed generation systems.

**Keywords:** Power Hardware-in-the-Loop, distributed generation, grid compatibility testing, LVRT testing, PHIL interface, grid modeling, grid simulator

**List of Abbreviation**

| | |
|---|---|
| AITM | Advanced Ideal Transformer Method |
| ASM | Asynchronous Motors |
| CHIL | Controller Hardware-in-the-Loop |
| D-PMSG | Direct-drive Permanent Magnet Synchronous Generator |
| DFIG | Doubly-Fed Induction Generator |
| DG | Distributed Generation |
| DIM | Damping Impedance Method |
| GSVSC | Grid Side Voltage Source Converter |
| EUT | Equipment under Test |
| FRT | Fault Ride Through |
| IEC | International Electrotechnical Commission |
| IEEE | Institute of Electrical and Electronics Engineers |
| ITM | Ideal Transformer Method |
| LQR | Linear Quadratic Regulator |
| LVRT | Low Voltage Ride Through |
| MPPT | Maximum Power Point Tracking |
| OIPI | Online Impedance Parameter Identification |
| PCC | Point of Common Coupling |
| PHIL | Power Hardware-in-the-Loop |
| PI | Proportional-Integral |
| PLL | Phase Locked Loop |
| PR | Proportional-Resonant |
| PWM | Pulse Width Modulation |
| RTDS | Real Time Digital Power System Simulation |
| RTS | Real-Time Simulator |
| SI-VSG | Shunt Impedance based Voltage Sags Generator |
| SPWM | Sinusoidal Pulse Width Modulation |

| | |
|---|---|
| VSC-HVDC | Voltage Source Converter based High Voltage Direct Current |
| WFVSC | Wind Farm side Voltage Source Converter |

**Index**

# 1 Introduction

## 1.1 Background

Due to the needs of the environmental protection, as well as the depletion of fossil fuels from society, the demand for renewable energy is growing. “Renewable energy” refers to the wind energy, solar energy, geothermal energy and other non-fossil energy. The energy density of renewable energy is much smaller than that of fossil fuels, so the renewable energy needs to be collected with distributed generation method [1]. The renewable energy that can be used by Distributed Generation (DG) system includes wind power, photovoltaic, geothermal, tidal and so on. In order to make the DG system meet the grid codes, now days power electronic equipment is usually used to connect the DG system and the power system. This type of DG systems is isolated from the power grid by the power electronic equipment, so they are generally described as the Inverter-based Distributed Generation systems. The power electronic equipment has a more complex topology and more complex control strategies than the traditional power generation equipment. This complexity and uncertainty reduces the stability of the power system.

The grid compatibility performance of DG systems has several themes, such as harmonic emission, protection, and fault behavior. The grid compatibility performance related to the control strategy. When the power grid fault occurs and the DG system using the traditional tripping strategy, it will lead to increase the severity of the grid fault and may be cause a cascading failure eventually leads to a blackout or, at least [2], increase the difficulty of power system re-synchronization. On the other hand, the frequent tripping incidents will reduce the utilization efficiency of DG systems and have a negative impact of the economic benefits [3]. In addition, with the wide application of DG systems, when a large number of DG systems is connected to the grid, the interaction between those DG systems may cause resonance effects, voltage fluctuations and other disturbances of the power system, leading to the tripping incidents of the DG systems and the damage of the other electrical equipment.

Now the global renewable DG systems have shown a good development trend. But it should also be seen as a result of the rapid growth of distributed energy, but the stable operation of the power system is now facing great challenges. In order to ensure the reliable operation, improve the efficiency of DG systems, the DG systems should not only be able to operate within a health power grid, but DG systems should also have an adequate grid Fault Ride Through (FRT) ability, which can both protect the power system and quickly restore power supply.

Before the DG systems are connected to the grid, it is necessary to carry out a reliable test method ability to conduct a comprehensive test for its normal operating ability and the FRT

ability. This is a grid compatibility test, which ensures the reliable operation of DG systems in all kinds of power grid environment.

## 1.2 Present Status of the Test Methods

The grid compatibility testing inspects the ability of the operation of DG systems under various grid environments. In order to determine whether the Equipment under Test (EUT), which are DG systems in this thesis, has the adequate grid compatibility, it is necessary to give the grid environment situation (excitation) to the EUT. According to the generation mode of the excitation, the testing can be divided into open loop test method and closed loop test method.

The open loop test method produces the pre-set grid environment situations and feeds into the EUT. The response of the EUT to this excitation is not allowed or not available to affect the following excitation. The test method of the present grid compatibility testing is the open loop test method.

The excitation from the closed loop test method is obtained from the simulation results. The response of the EUT is fed back to the test system, and then the resulting excitation will be affected. Such a test method forms a closed loop process, and is therefore called a closed loop test method. The closed loop test method contains the physical model simulation test method, the numerical model simulation test method, the Controller Hardware-in-the-Loop test method and the Power Hardware-in-the-Loop test method.

The methods of grid compatibility testing are classified as in Figure 1-1:

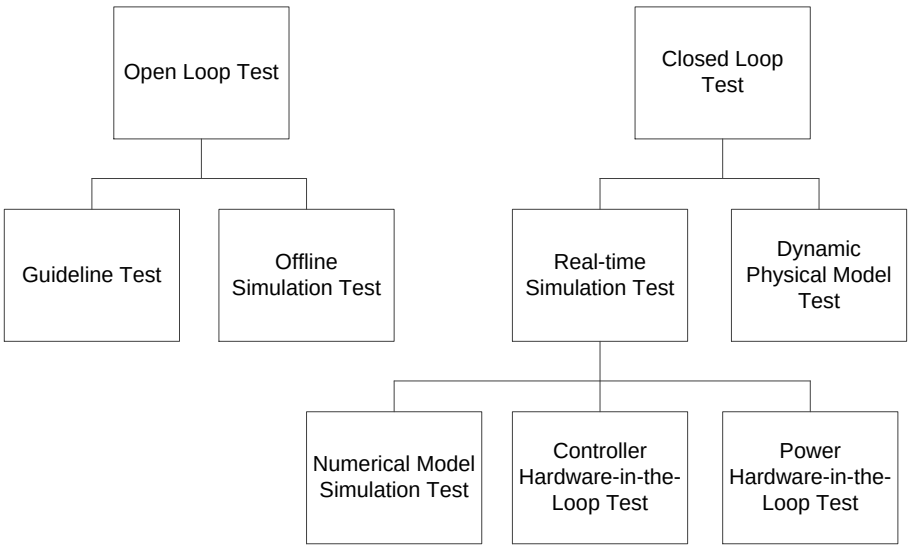



**Figure 1-1; Classification of test methods for grid compatibility testing**

The guideline test and offline simulation test belong to the open loop test method. The guideline test bases on classical cases in power systems, it summarizes and analyses the normal and fault characteristics of power systems, and then the results used as excitation in

the test system, for example, constant voltage amplitude, frequency and so on. The guideline test is now widely used in grid compatibility testing for DG systems. The excitation during offline simulation test is from the simulation results of the built-in grid model or pre-recorded waveforms from real power systems. This test method is now applied to testing of relay/protection equipment [4].

The closed loop test method includes real-time simulation test and dynamic physical model test. The dynamic physical model simulation test is made to simulate the physical process of the prototype grid system by setting up a reduced dimension physical model [5]. There is no doubt that the dynamic physical model test is the most direct and immersive simulation test method. But it is limited by the size of the actual test system, for more accurate reproduction of the characteristics of the original power systems, the simulation model is required to be as big as possible, which also increases the investment, reduces scalability and compatibility. At present, the dynamic physical model test is mainly used in the research of small distributed generation systems.

The real-time simulation test contains the numerical model simulation test, the Controller Hardware-in-the-Loop test method and the Power Hardware-in-the-Loop test method.

The numerical model simulation test carries out numerical modeling of the power systems, which is usually used in the early stage of development of the DG system. Compared with the dynamic physical model simulation test, it has a series of advantages, such as less investment, easier reconstruction and large-scale simulation. But due to the lack of physical hardware components of EUT, the numerical model simulation test can only carry out the theoretical validation of the hardware configuration and control strategy. The accuracy and reliability of this test is not as well as the dynamic physical model simulation test.

The Hardware-in-the-Loop test has the both advantages of the dynamic physical model simulation test and the numerical model simulation test. According to the EUT, it can be divided into the Controller Hardware-in-the-Loop test and Power Hardware-in-the-Loop test.

The EUT of the Controller Hardware-in-the-Loop (CHIL) test is the controller hardware and the embedded control program of the DG system. Let the controller to control the numerical model of hardware part of the DG system in real-time simulation, in order to test the function of the controller.

The EUT of the Power Hardware-in-the-Loop (PHIL) test is the complete DG system, which includes the controller and its hardware part. The EUT is connected to the grid environment, which is modeled and simulated in the real-time simulator, to test the grid compatibility of the DG system. This is the main research content of this thesis.

## 1.3 Present Status of the Power Hardware-in-the-Loop Test

The development of the renewable distributed generation has brought a large number of inverter based distributed generation technology. The response of the DG system to the power systems is closely related to its hardware topology and the control strategy. However, the manufacturers to carry out the technical confidentiality to their products, this makes users and grid operators cannot have a prior prediction of the actual grid compatibility of the DG systems. So it is necessary to adopt a comprehensive test on it with Power Hardware-in-the-Loop test. In the United States and Europe, a number of research institutions have been studied the Power Hardware-in-the-Loop test methods and established the test laboratories accordingly.

Present the world's largest PHIL test system for grid compatibility testing is established in Clemson University in the United States [6].Its rated power is 15 MVA, and the EUT of this test system are the grid-connected equipment of the large offshore wind turbines. The real-time simulator is a Real Time Digital Power System Simulation (RTDS) [7]. The hardware part of the test system contains a group of converters, step-up transformers and shunt impedance based voltage sags generators. The output of the converters is 4.16 kV, then it is stepped up through the transformer to 23.9 kV as the testing voltage. In the testing of Low Voltage Ride Through capability, the converters and the Shunt Impedance based Voltage Sags Generators are connected in series, in order to reduce the impact of the short circuit current on the converters. The topology of the PHIL test system is shown in Figure 1-2. The converters use the Serial Connected H-Bridge topology to increase the output voltage amplitude and the equivalent switching frequency, to get better output performance. The converter modules are connected in parallel to increase the rated capacity of the test system. This PHIL test system has the advantages of large capacity and high accuracy of output voltage waveform. The Hardware-in-the-Loop test method is not used in the test of the Fault Ride Through capability, but the classical guideline test method. So technically, the test system of Clemson University is an incomplete Power Hardware-in-the-Loop test system.

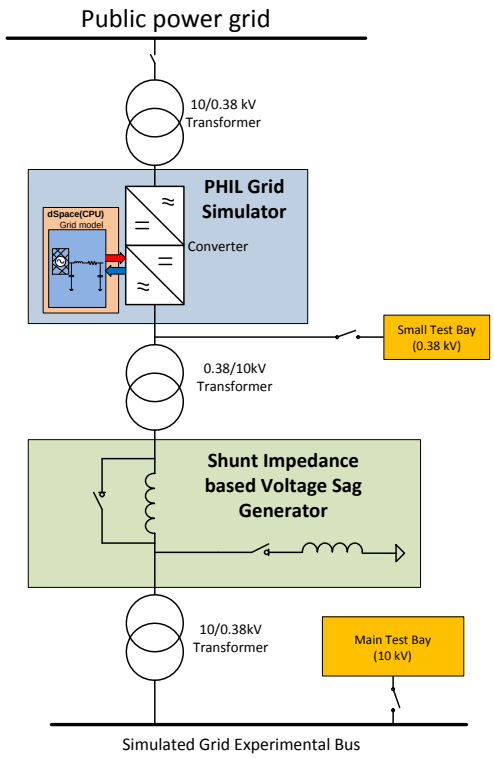



**Figure 1-2; Topology of the PHIL test system in Clemson University**

The rated power of the "Controllable Grid Interface" from the National Wind Technology Center of the United States is 7 MVA [8]. The EUT of this test system are the grid-connected equipment of the large offshore wind turbines, large photovoltaic converters and energy storage systems. The real-time simulator is made by RTDS. The hardware part contains a group of converters and step-up transformers. The topology of the converters consist of three groups of 4-level inverter connected in parallel. The output of the converters is 3.3 kV, then it is stepped up through the transformer to 13.2 kV as the testing voltage.

The rated power of the PHIL test system from the Center for Advanced Power Systems, Florida State University in the United States is 5 MVA [9]. The real-time simulator is RTDS. The hardware part contains a group of converters and step-up transformers. Two sets of 2.5 MVA converters are connected in parallel, through the coupling of the transformer. Its dynamic response time is 0.35 ms.

The Center for Wind Power Drives of Technische Hochschule Aachen in Germany established the Full-Size Wind-Turbine Test Bench [10]. Its rated power is 4 MVA. The EUT of this test bench are the grid-connected equipment of wind turbines. The real-time simulator is RTDS. The hardware part contains a group of converters and step-up transformers. The converters use a three level neutral-point-clamped topology. The output of the converters is 3.1 kV, then through the transformer to 20 kV as the testing voltage. The total harmonic distortion of the output voltage waveform is not greater than 8%. The accuracy of the PHIL test is affected by the quality of the output voltage waveform.

To summarize, testing methods of the above PHIL test systems, especially the testing method of the fault ride through test, are still using the concept of the guideline test. The above PHIL test systems have not paid enough attention to the simulation delay and accuracy problem, and the reproduction ability of the power grid environment is weak. In addition, the operation bandwidth of the output voltage frequency of the above test systems is utility frequency (50/60 Hz), so they cannot produce independently the higher order harmonics. Therefore, it is necessary to improve the existing testing methods, present with new PHIL test system, which is suitable for the grid compatibility test of the DG systems. Specifically, the real-time performance and accuracy need to be improved respectively from hardware and software, and also carry out the wide operation bandwidth, to meet the requirements of the PHIL testing.

## 1.4 Scientific Contributions

This thesis contains the following scientific and technical contributions by the author:

A comparative study of the difference between the real grid situation and test methods from the present standards is given. The present test methods and related test generators caused some tripping incidents of DG systems (see chapter 2.1). This thesis reproduces these tripping incidents in laboratory test and carries out a systematic analysis on them.

The different dynamic behaviors between the real grid situation and present test generators are caused by the unreality system impedances and the lack of the retroactive effects (see chapter 2.4 and 2.5).

In the application of Power Hardware-in-the-Loop testing, this thesis gives new research results concerning the stability analysis of the operation sequence. Accordingly, this thesis presents a stability criterion and an optimized operation sequence for a high power Power Hardware-in-the-Loop test system (see chapter 3.1).

This thesis also presents a new Power Hardware-in-the-Loop interface algorithm, the so called advanced Ideal Transformer Method. This does not need additional voltage sensors, but it can also guarantee the stability and dynamic performance of the Power Hardware-in-the-Loop test system (see chapter 3.3.4.2).

This thesis describes a new online impedance parameter identification algorithm: online obtain the impedance of the EUT, which is a nonlinear time varying system, in order to enhance the performance of the Damping Impedance Method (see chapter 3.4.4)

The phase compensation algorithm based on frequency domain is usually applied for the milliseconds class system delay. Due to the limitation of this algorithm, the result of the phase compensation is not in real-time. This thesis gives an advanced phase compensation

algorithm based on coordinate transformation. It can compensate the phase (system delay) in real-time for the symmetrical voltage signal (see chapter 3.5.2).

This thesis also describes the innovative universal requirements of the Power Hardware-in-the-Loop test system, which including the update frequency of the test system and performance requirements of the power amplifier (see chapter 3.6).

The modeling methods of DG systems are usually detailed electromagnetic transient models. Due to the high computational complexity, it can only be used in off-line simulations. This thesis presents a new universal simplified modeling method of DG systems for real-time simulation, which reduces the computational complexity and keeps the accuracy of the simulation results (see chapter 4.2 and 4.3).

Common high power power amplifiers have a limited operation bandwidth and limited response speed. In this thesis presents a power amplifier with a Proportional-Resonance regulator based on the delta operator is presented. Its operation bandwidth is 0 Hz to 2000 Hz, its response speed is 100 μs (see chapter 5.3).

## 1.5 Main Content of the Thesis

This thesis is based on the “Joint research of testing technology of wind power connect to the distribution network” sponsored by the China and Austria International Cooperation Project (WTZ/OeAD), “Research and development: Test system of grid compatibility for wind power system” and “Research and development: Test system of Low Voltage Ride Through ability for wind turbine” from the Committee of Shanghai Science and Technology Project. This thesis carries out the theoretical research and experiments of the test methods and test generator of the grid compatibility testing for the large distributed generation systems, and also the establishment of a PHIL test system.

The main contents of this thesis are arranged as follows:

In the **chapter 1**, the test methods and test generator of the grid-connected distributed generation systems are summarized in this thesis, which focuses on the present development situation of the Power Hardware-in-the-Loop test system. At the end of chapter 1, the research content and the arrangement of the chapters are described.

The **chapter 2** goes a detailed study of the difference between the test methods of the present standards and the situation in the real power systems, and proves the necessity of the Power Hardware-in-the-Loop test.

In the **chapter 3**, the Power Hardware-in-the-Loop test system will be studied. The research focuses on the operation sequence and the PHIL interface algorithm. Through the analysis of the numerical model of PHIL test system, the stability and the accuracy of the system will be

studied. The scheme of improving the stability and the accuracy of the PHIL test system will be presented.

The **chapter 4** carries on the research on the testing grid environment. Considering the present situation and trends, the universal equivalent simplified modeling method will be presented. While improving the reality and reliability of the PHIL testing, the calculation complexity of the real-time simulation is reduced.

In the **chapter 5**, the power amplifier of the PHIL test system is studied. With a series of novel topology and control strategy, the power amplifier can meet the system requirements from the preceding chapters, which means high accuracy and fast response speed in a wide operation conditions bandwidth.

The **chapter 6** verifies the theoretical derivation of the stability and the accuracy of the PHIL test system and the performance of the power amplifier through the experiments. Finally, through a set of PHIL testing, the function of the PHIL test system and verified.

The **chapter 7** is the conclusion of the thesis and the outlook of future research.

# 2 Comparative Study on Test Methods and Test generator

## 2.1 Background

Tripping incidents of DG systems happens time to time, when the large scale tripping of DG systems occurs, which is caused by power system faults, and this will serious threat to the normal operation of the power systems.

In the large disturbance in the European power system on the 4th of November 2006, a large number of wind turbines tripping from the power system. This increases the load unbalance of the power system, leads to further instability and longtime frequency fluctuations [2]. From 2010 to 2012, a large number of tripping incidents occur in China's wind farms, there were 308 cases [3], [11], [12], [13]. Among them, it is worth noting that, between 1st May and 14th September 2011, due to the local grid failures, there were 153 units / times tripping incidents at Changling wind farm. All of the wind turbines in this wind farm have the low voltage ride through ability, and the testing and inspection of low voltage ride through ability was completed in 23th May, 2010. But they still cannot ride through the fault from the real grid failure. In addition, from 2008 to 2013, there were many large scale tripping incidents in China's wind farms caused by harmonics [14], [15], [16].

All of the wind turbines and wind farms in above tripping incidents have passed the related Fault Ride Through ability testing, but in the actual operation, when the real grid failure or disturbance occurs, they cannot ride through.

The photovoltaic generation equipment also have a similar situation [17]. The photovoltaic generation equipment passed the grid compatibility testing in the test laboratories and obtained the relevant certification, but when they are connect to the real power grid, they still cannot normally operate.

In this chapter, this problem will be theoretical studied in-depth. A detailed comparative analysis will be carried out, which between the impacts from real grid situation on the DG systems and the impact from the test methods and the test generator from the present standards on the DG system.

## 2.2 Impacts from Real Grid Situations on the Distributed Generation System

When the large numbers of DG systems are connected to the power systems, the influence between the power systems and the DG systems is increasingly prominent [18]. Most of DG systems are connected to the power systems through power electronics equipment, due to

the lack of the rotation component, this results in a very fast dynamic response speed. The voltage fluctuation, frequency deviation, harmonic and three-phase unbalance from the power systems can easily interfere with the normal operation of the DG systems. At the same time, the reaction of the DG systems will make the power systems to generate further dynamic interaction, that is, the retroactive effects of power systems [19], [20].The retroactive effects are embodied in the voltage amplitude oscillation, the influence of the grid impedances and the resonance phenomenon of the clustered grid-connected DG systems.

Next, the stability of grid-connected DG system is studied by the modeling of a classical complex power grid, impedance analysis method and controller model analysis method respectively.

### 2.2.1 Study of the Dynamic Behavior of Voltage Dips

The main reasons of the dynamic response from the real power systems during and after the voltage dips are: the other power generation equipment, automatic reclosing, de-loading / re-loading, etc. Among them, the other power generation equipment has the most significant impact on the re-synchronization after the grid fault [21].

In order to quantitatively study the voltage dips problem in a complex power grid environment, a simplified equivalent model is established in Matlab/Simulink. The method of the modeling is described in chapter 4. The singe line diagram is shown in Figure 2-1**.**

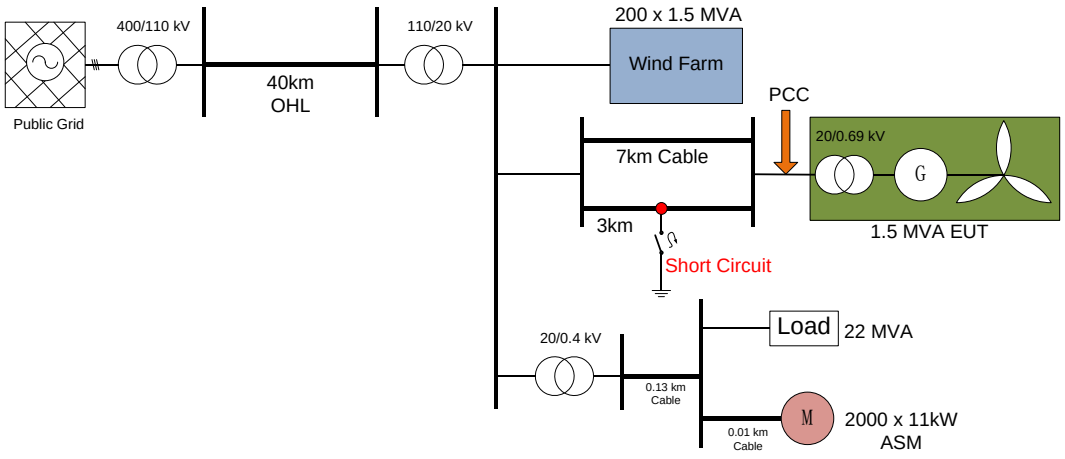



**Figure 2-1; Singe line diagram of a complex power system**

This is shown in Figure 2-1, the grid model contains a wind farm, which consisting of 200 x 1.5 MVA permanent magnet synchronous generator. The 2000 x 11 kVA asynchronous motor and a 22 MVA resistance load are installed in low voltage network. The Equipment under Test (EUT) feeds into the grid through the double line. On one line a three phase fault occurs at 3 km from the network side. This thesis simulates both influences from motors and the wind farm on the voltage dips amplitude curve include the retroactive effect. The parameters of this complex power system is shown in Table 2-1.

Firstly, the wind farm is removed from the model, only the effect of the asynchronous motors on the EUT is observed. The Asynchronous Motors (ASM) experience two phases: During the voltage dip, the stator current of the ASM decreases quickly. Due to the law of the flux conservation, the rotor winding induction current decays slowly to maintain the flux, so that the stator winding induce a residual voltage. After the grid voltage dip, the voltage of the motor stator is below the rated voltage, and this produces an impact current with several times the rated value. This impact current causes an additional voltage dip in the system. Therefore, the voltage is not directly back to normal, but slowly rising.

| Name | Parameter Name | Parameters |
|---|---|---|
| Public grid | Voltage | 400 kV |
| | Short circuit capacity | 34 GVA |
| Overhead line | Specific resistance (positive and zero sequence) | 0.033 Ω/km,1 Ω/km |
| | Specific inductance (positive and zero sequence) | 0.33 mH/km, 1.5 mH/km |
| Cable | Specific resistance (positive and zero sequence) | 0.033 Ω/km ,1 Ω/km |
| | Specific inductance (positive and zero sequence) | 0.16 mH/km, 0.76 mH/km |
| | Specific capacitance (positive and zero sequence) | 1 µF/km, 1 µF/km |
| Loads | Power of the resistive loads | 11 MVA |
| | Power of the ASMs | 2.2 MVA |
| Wind farm | Rated power of a wind power unit | 1.5 MVA |
| | Number of the wind power units | 200 |

**Table 2-1; Parameters of the complex power system**

This is shown Figure 2-2, the blue curve is the voltage of the EUT, which is the simulation result from the grid model without ASM. After the fault is cleared, the voltage rises directly to the rated voltage (1.0 p.u.).The red curve represents the simulation results from the grid model with ASM. After the failure is clear, the voltage rises slower to the rated voltage than in the blue curve.

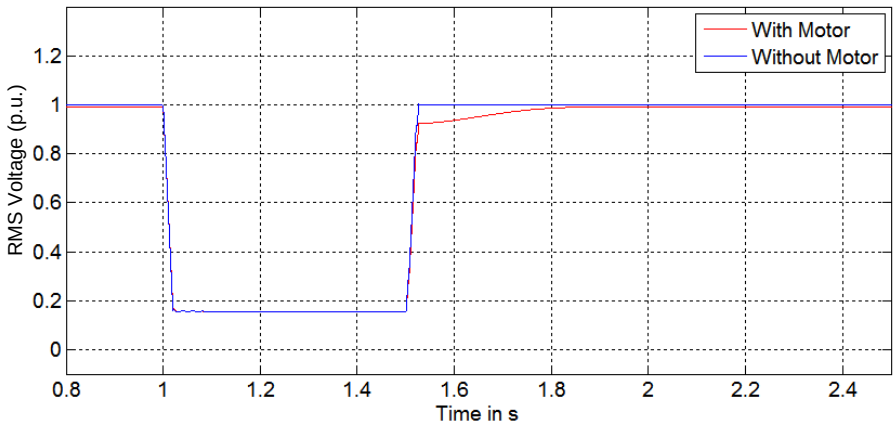



**Figure 2-2; Voltage dip amplitude curve with/without motors**

In order to observe the influence of the wind farm on the EUT, now the wind farm is connected to the grid model. When the voltage dips occurs, the wind farm should continually operate and provide reactive power to support the grid voltage quickly rise to normal. In accordance with the control strategy of DG systems, which the details is described in chapter 4.2, the reference of the output current has an inverse relationship with the grid voltage [22], [23]. Therefore, when the voltage dips occurs, and this is detected by the control system, it will lead to the rapid increase of the current reference. Similarly, when the grid voltage goes back to normal, the control system will reduce sharply the current reference. This is shown in Figure 2-3.

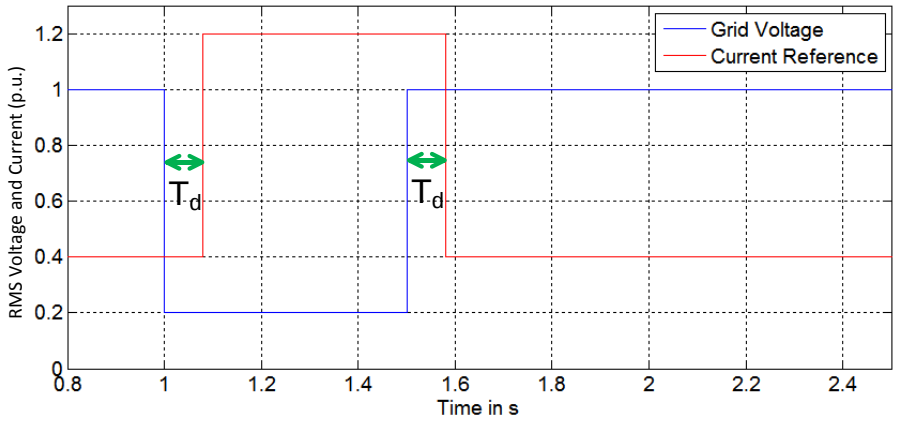



**Figure 2-3; Grid voltage and current reference of the DG system**

In Figure 2-3, the blue curve is the grid voltage, the red curve is the reference of the output current of the DG system. When the grid voltage dips occurs, due to the delay of the grid voltage detecting algorithm and the control algorithm, the current reference will step jump in $T_d$ seconds delay. When the grid voltage rise to 1.0 p.u., the current reference will reduce sharply in $T_d$ seconds delay. So the dynamic response of the DG system will lead to the further voltage fluctuation of the power systems during the voltage dips. In Figure 2-4 is the simulation result with the wind farm.

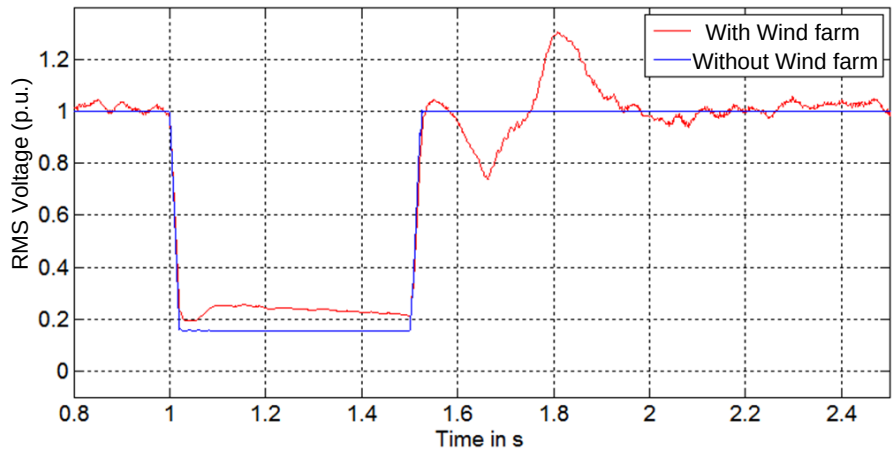



**Figure 2-4; Voltage dip amplitude curve with/without wind farm**

This is shown in Figure 2-4, the red curve represents the voltage at the output of EUT, after the voltage dip occurs, the voltage is reduced to the 0.2 p.u., after few milliseconds the voltage rises to 0.25 p.u.. After the delay caused by the controller of DG systems, the output current amplitude increases, thus raising the grid voltage. Similarly, after the cleaning of the fault, the voltage raises more than 1.0 p.u., and then the oscillation of the voltage amplitude occurs. After 0.5 seconds, grid voltage is stable again. The voltage amplitude oscillation after the voltage recovery may cause the secondary voltage dip, which may lead to the further instabilities of the power systems.

### 2.2.2 Inference of the Grid Impedances upon the Distributed Generation System

Based on the impedance analysis method [24], the system can be divided into two subsystems: the subsystem of the bulk power system and the DG system. The subsystem of the power system usually represent according to the Thevenin equivalent circuit, that is a serial circuit with an ideal voltage source $U_{grid}$ and its output impedance $Z_{grid}$.

Traditionally, an ideal current source and a parallel connected impedance are used to replace the DG system. In the system analysis, the influences of both the output impedance and the output current of the DG system need to be considered. When there is a plurality of external influences, the observation of the system will become difficult. So here use a negative impedance to replace the DG system, which the function of this negative impedance is a nonlinear piecewise function due to the control strategy of the DG system. When the energy input side of the DG system is not considered, the current output of the DG system is only affected by the grid voltage. Therefor the equivalent circuit in Figure 2-5 can be used in the impedance analysis. ZDG is the output impedance of the DG system.

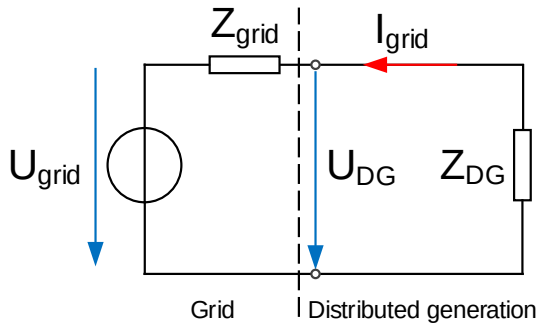



**Figure 2-5; Equivalent circuit of the DG system and power system**

The block diagram can be obtained by Figure 2-5 as shown in Figure 2-6.

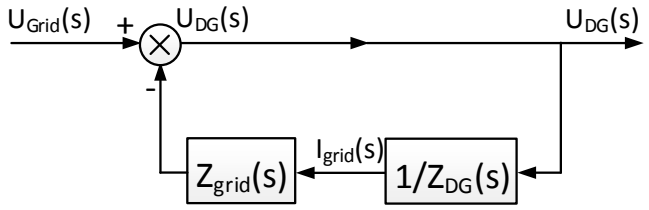



**Figure 2-6; Block diagram of the DG system and power system**

The open loop transfer function of the system can be obtained from Figure 2-6.

$$G_{OL}(s) = \frac{Z_{grid}(s)}{Z_{DG}(s)} \qquad \text{Eq. 2-1}$$

According to the open loop transfer function of the system (Eq.2-1), if the impedance ratio between the grid impedance and the output impedance of the DG system $|Z_{grid}(s)/Z_{DG}(s)|$ meets the Nyquist stability criteria, this system is stable. When the Eq.2-2 is fullfilled, this DG system can stably operate at this grid situation.

$$\left|\frac{Z_{grid}(s)}{Z_{DG}(s)}\right| < 1 \qquad \text{Eq. 2-2}$$

In an ideal grid, the grid impedance $Z_{grid}$ is infinitesimal, so the Eq.2-2 is naturally met, and there is no oscillation phenomenon in this power system. When the Eq.2-2 cannot be met, which caused by the non-zero grid impedance of the real grid and design defects of the controller of the DG system, this may result in oscillations, which leads to the instability of this system.

### 2.2.3 Analysis of Control Models

In chapter 2.2.2, the stability criteria of the power system with DG systems is presented by using the impedance analysis method, in this chapter, the control model analysis method is used to analyze the resonance phenomenon of the DG systems.

#### 2.2.3.1 Control Model Analysis of a Single Distributed Generation System

The inverter topology of the common DG system is shown in Figure 2-7. The output voltage of the inverter bridge $U_{inv}$ will go through the LC filter outputs to the grid side. The capacitor voltage $U_{out}$ is equal to the grid voltage, and the fundamental component of the inductor current $I_L$ is equal to the grid current if the fundamental current of the capacitor is neglected.

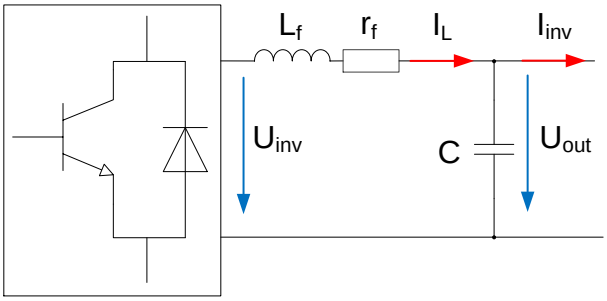



**Figure 2-7; Topology of the inverter topology of a common DG system**

According to Figure 2-7, the block diagram of system can be obtained, as shown in Figure 2-8. The Iref is the reference signal of the output current. The $K_p$ and $K_i$ are the control parameters of the Proportional-Integral regulator.

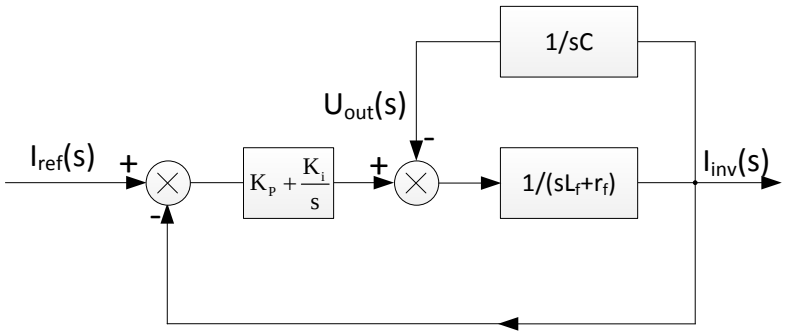



**Figure 2-8; Block diagram of the inverter of a common DG system**

From Figure 2-8, the transfer function for the reference current $I_{ref}(s)$ to the output current $I_{inv}(s)$ is Eq.2-3.

$$G_{Iref}(s) = \frac{I_{inv}(s)}{I_{ref}(s)} = \frac{sK_pC + K_iC}{s^2L_fC + s(K_pC + r_fC) + K_iC + 1} \qquad \text{Eq. 2-3}$$

The parameters of the system in Figure 2-7 are shown in Table 2-2.

| Name | Parameters |
|---|---|
| Rated power | 500 kVA |
| Rated output voltage | 400 V |
| Inductor of the filter | 0.4 mH |
| Equivalent resistance of the filter | 0.001 Ω |
| Capacitor of the filter | 175 µF |

**Table 2-2; Parameters of inverter of a common DG systems**

The Bode diagram is shown in Figure 2-9.

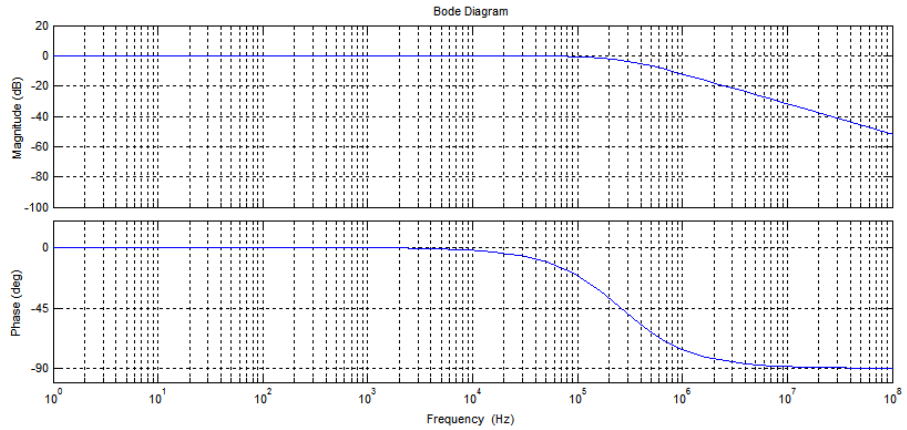



**Figure 2-9; Bode diagram of the inverter of a common DG system**

This is shown in Figure 2-9, there is no resonant point in the output current of the single inverter of a DG system.

### 2.2.3.2 Control Model Analysis of Cluster Distributed Generation Systems

The topology of the cluster DG systems is shown in Figure 2-10. With the increase output current of the inverter, the equivalent impedance ($L_T$ and $r_T$) of the step-up transformer cannot be ignored. With the number of parallel inverter increasing, resulting in the equivalent grid impedance ($L_g$ and $r_g$) also cannot be ignored. $I_{Sum}$ is the sum of the current of the inverters in this system. Taking into account the step-up transformers and grid impedance, the block diagram is shown in Figure 2-11.

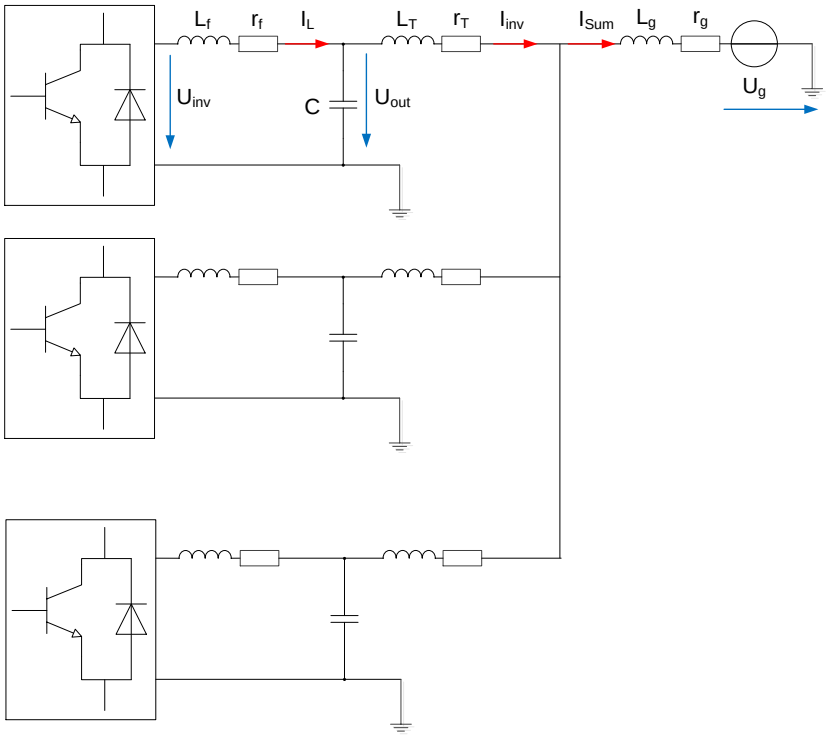



**Figure 2-10; Topology of the cluster DG systems**

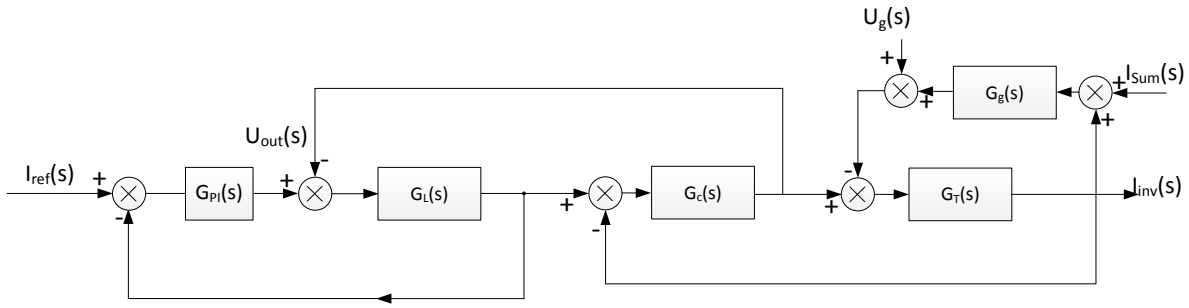



**Figure 2-11; Block diagram of the cluster DG systems**

Among them:

$$\begin{cases} G_{PI}(s) = K_P + \dfrac{K_i}{s} \\ G_L(s) = \dfrac{1}{L_f s + r_f} \\ G_C(s) = \dfrac{1}{Cs} \\ G_T(s) = \dfrac{1}{L_T s + r_T} \\ G_g(s) = \dfrac{1}{L_g s + r_g} \end{cases} \quad \text{Eq. 2-4}$$

The transfer function for the reference current $I_{ref}(s)$ to the output current $I_{inv}(s)$ is Eq.2-4.

$$G_{iref}(s) = \frac{I_{inv}(s)}{I_{ref}(s)} = \frac{G_C(s)G_L(s)G_{PI}(s)G_T(s)}{D(s)} \quad \text{Eq. 2-5}$$

Which D(s) is shown in Eq.2-6.

$$\begin{aligned} D(s) = 1 + G_C(s)G_L(s) + G_C(s)G_T(s) + G_L(s)G_{PI}(s) + G_T G_g(s) \\ + G_C(s)G_L(s)G_{PI}(s)G_T(s) + G_C(s)G_L(s)G_T(s)G_g(s) + G_L(s)G_{PI}(s)G_T(s)G_g(s) \end{aligned} \quad \text{Eq. 2-6}$$

The Bode diagram of the $G_{iref}(s)$ is shown in Figure 2-12.

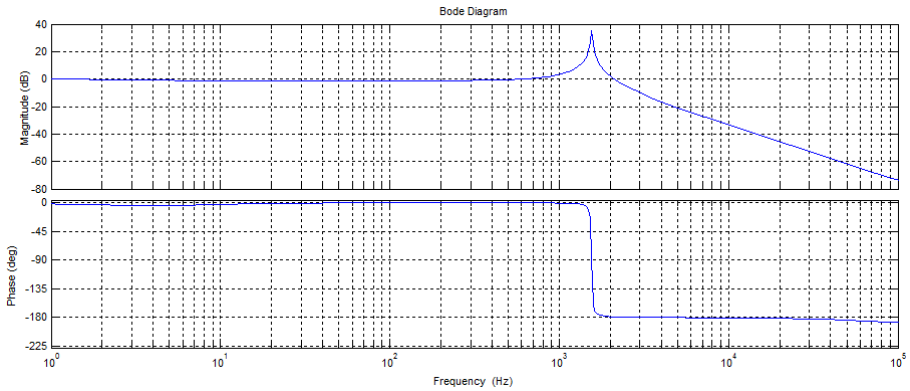



**Figure 2-12; Bode diagram of the cluster DG systems**

The parameters of the system shown in Figure 2-10 are shown in Table 2-3**.**

| Name | Parameters |
|---|---|
| Rated power | 500 kVA |
| Rated output voltage | 400 V |
| Inductor of the filter | 0.4 mH |
| Equivalent resistance of the filter | 0.001 Ω |
| Capacitor of the filter | 175 μF |
| Equivalent Inductor of the transformer | 70 μH |
| Equivalent resistance of the transformer | 0.01 Ω |
| Equivalent Inductor of the grid | 1 mH |
| Equivalent resistance of the grid | 0.025 Ω |
| Number of the DG systems | 8 |

**Table 2-3; Parameters of the cluster DG systems**

As can be seen from Figure 2-12, when considering the influence of the transformer and the grid impedance, the output current of the DG systems has a resonant frequency point. The control strategy of the common DG system is designed for the model in Figure 2-7, not the model of the cluster DG systems in the real power system as shown in Figure 2-10. Compared with the block diagram of Figure 2-8 and Figure 2-11, the control strategy of the common DG system has been no longer applicable to the case of the cluster DG systems.

In order to observe the influence from the grid impedances on the resonance frequency of this system, the transfer function of the output current $U_g(s)$ to the output current $I_{inv}$ (s) is obtained by Figure 2-11:

$$G_{Ug}(s) = \frac{I_{inv}(s)}{U_g(s)} = -\frac{G_T(s) + G_C(s)G_L(s)G_T(s) + G_L(s)G_{PI}(s)G_T(s)}{D(s)} \qquad \text{Eq. 2-7}$$

The Bode diagram of this system with different grid impedances is shown in Figure 2-13.

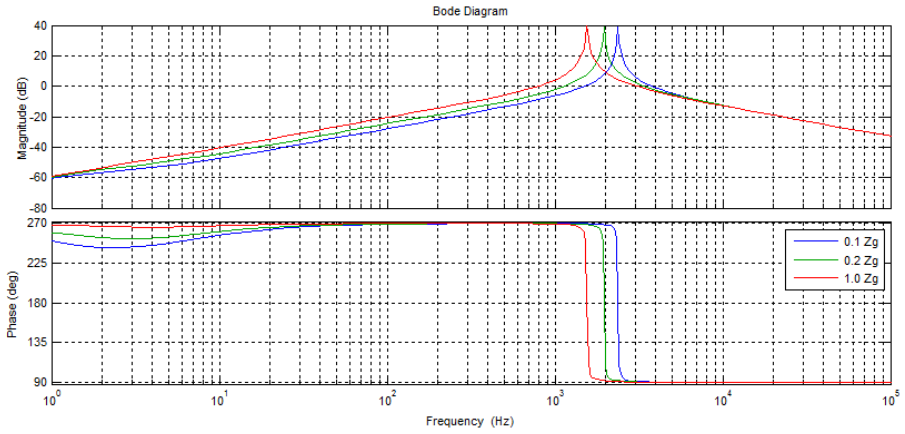



**Figure 2-13; Bode diagram of this system with different grid impedance**

It can be seen in Figure 2-13, when the $Z_g$ is 0.1 times as the grid impedance in Table 2-3, the resonance frequency is the highest. The resonant frequency decreases with the increase of the grid impedance. The lower the resonant frequency of the cluster DG systems, the lower the characteristic harmonic of this system, accordingly, the greater the interference on

control strategy such as phase locked loop algorithm. This may easily lead to instability of the system [25].

By modeling and simulation of a classical complex power system, impedance analysis and control model analysis, there are several reasons for the abnormal operation of DG systems in the real power system: the grid voltage amplitude oscillation caused by the delay of the grid voltage detection algorithm and the control strategy; Instability of DG systems caused by inappropriate grid impedance; Instability due to system resonance, which caused by the parallel operated cluster DG systems.

## 2.3 Study of the Present Testing Standards

The testing standard of distributed generation systems is the technical basis and prerequisite of ensuring of the power quality of power systems and the effective utilization of distributed energy. So the related international organizations such as International Electrotechnical Commission (IEC) and Institute of Electrical and Electronics Engineers (IEEE) have developed the earliest technical standard of the distributed generation systems. In 1994, IEC first developed a series of standards for wind turbine systems, namely the IEC 61400 standards series：<International Standard published by the International Electrotechnical Commission regarding wind turbines>. This standard has been accepted and applied in Europe and Japan and other countries. IEC 61400 standards series covers the design, manufacture, installation and safety, dynamic performance test, power quality test and fault ride through test of wind turbines. In 2003, IEEE proposed the IEEE 1547 standards series, which is called <Standard for Interconnecting Distributed Resources with Electric Power Systems>, to unify all types of the distributed generation systems, IEEE 1547 standards series covers the performance, operation, testing, security and maintenance of the distributed generation systems.

With IEC and IEEE standards as a reference, many countries have developed their own testing standards accord to the practical facts, as shown in Table 2-4.

| Country | Standard number | Standard Name |
|---|---|---|
| Australia | AS4777 | Grid connection of energy systems via inverters |
| Canada | CAN/CSA-C22.2 NO. 257-06 (R2015) | Interconnecting Inverter-Based Micro-Distributed Resources to Distribution Systems |
| Canada | CAN/CSA-C22.3 NO. 9-08 (R2015) | Interconnection of distributed resources and electricity supply systems |
| China | Q/GDW480-2011 | Technical Rule for Distributed Resources Connected to Power Grid |
| China | GB/T 19939-2005 | Technical requirements for grid connection of PV system |
| China | GB/T 19963-2011 | Technical rule for connecting wind farm to power system |
| Germany | VDE-AR-N4105 | Erzeugungsanlagen am Niederspannungsnetz, Technische Mindestanforderungen für Anschluss und Parallelbetrieb von Erzeugungsanlagen am Niederspannungsnetz |
| Germany | | Bundesverband der Energie- und Wasserwirtschaft-Richtlinie für Anschluss und Parallelbetrieb von Erzeugungsanlagen am Mittelspannungsnetz |
| Germany | | Fördergesellschaft Windenergie und andere Erneuerbare Energien: Technischen Richtlinie 1-8 |
| Spain | RD1663/2000 | Real Decreto 1663/2000, de 29 de septiembre, sobre conexión de instalaciones fotovoltaicas a la red de baja tension |
| United Kingdom | G83/1-1 | Recommendations for the Connection of Small – scale Embedded Generators (Up to 16A per Phase |
| United States of America | UL 1741 | Standard for Inverters, Converters, Controllers and Interconnection System Equipment for Use With Distributed Energy Resources |

**Table 2-4; Standards of the DG system in different countries**

These standards are very similar in the certification processes, test methods and the requirements of the test cases. The following analysis and research will be carried out separately in the certification processes, test methods, test cases and test generator of these standards.

### 2.3.1 Certification Processes and Test Methods

The relevant certification must be obtained before the DG system is connected to the grid. Taking IEC 61400-22:2010 <Wind turbines - Part 22: Conformity testing and certification> as an example, the certification processes of wind turbines are divided into type certification and the project certification. In the type certification, the design of the wind turbine shall be evaluated, and the type testing shall be carried out. In the project certification, the reliability and performance of the wind turbine shall be evaluated under various wind conditions, other

environmental conditions and also electrical network conditions. In addition, some standards also require the model validation of the wind turbines, such as FGW TR4 <Fördergesellschaft Windenergie und andere Erneuerbare Energien: Technischen Richtlinie 4>.

The testing processes, which is specified in the certification processes, are as follows: A set of test conditions will be fed into the EUT by certification body, and then the response of the EUT will be observed and recorded by the certification body. Take as an example: the response to abnormal frequency testing in testing standard IEEE 1547, the EUT will be connected to a grid environment with a frequency of 60.5Hz, and the record the waveform is started until the EUT stops operation.

The grid-connected related testing in the certification processes are: safety and function testing, load testing, power characteristic testing, power quality testing, low voltage ride through testing. According to the classification of test methods in the chapter 1.2, the grid-connected related testing in the certification processes is classified as an open loop guideline test. The test conditions are produced by the abstraction of healthy and faulty situations in the power systems.

These test conditions must be able to cover most of the situation in power systems and also represent the real grid environment, in order to ensure the reliability and credibility of the testing.

### 2.3.2 Test Cases

Through the summary of the above test standards, the grid-connected related testing are the testing of the power quality and the testing of the response to the abnormal electrical network conditions.

In all above standards, the test cases of the power quality are voltage amplitude fluctuation, flicker, harmonic content of current and DC component of current.

The test cases of the response to the abnormal electrical network conditions are the response of abnormal voltage amplitude and frequency. In addition, each standard also includes the safety functions of the DG system. It should have the following functions: over/under-voltage protection, over/under-frequency protection, anti-islanding protection, etc.

The testing of the abnormal response of the voltage amplitude and frequency is the fault ride through testing. The DG system should stay connected to the grid under a certain abnormal condition. For example, the Low Voltage Ride Through (LVRT) testing requires the DG system to stay connect during the voltage dips. With LVRT ability, DG system must in some case provide reactive power to support the recovery of grid voltage during the voltage dips, and smooth operate after the voltage dips, in order to improve the stability of the power systems.

### 2.3.3 Test generator

According to the test standards, in the power quality test, a static grid environment has to been feed into EUT. The static grid environment can be produced by the public power grid or an ideal voltage source [26].

A dynamic grid environment has to be produced in the testing of the abnormal response. The dynamic grid environment can be produced by a grid fault simulator, which provides various grid fault situations, such as voltage deviations, frequency deviations or harmonic contant, etc.

The grid fault simulator can be in a generator mode [27], shunt impedance based voltage sags generator mode [28], transformer mode [29] and ideal voltage source mode, which is described in chapter 2.4 in greater detail. The most commonly used are the shunt impedance based voltage sags generator mode and the ideal voltage source mode, the characteristics of the both modes will be detailed analysis in the following chapters.

According to the standards of <IEC61400-21> and <TR4 FGW>, the electrical model of the EUT needs to be simulated and verified. In <TR4 FGW>, manufacturers need to provide the electrical model of the wind turbines based on the simulation software, such as Powerfactory, Matlab and PSCAD. According to the test cases in the related test standard, the electrical model of the test generator is simulated and tested by the certification body. The test conditions and test generator used in the model test are the same as in the normal test. Such as the test generator for LVRT testing, which is specified in the <FGW TR4>, is also the shunt impedance based voltage sags generator.

### 2.3.4 Limitations of the Present Testing Standards

The testing standards are the guidance document for the research and development of grid-connected distributed generation systems. Many research institutions and manufacturers design the DG system according to those testing standards and its test methods. Due to the lag of the standard development, and the special characteristic of the power systems, which is mentioned in chapter 2.2, the guideline test cannot cover the entire operation environment of a distributed generation systems. Therefore, it can't guarantee the reliability of the design of the distributed generation systems and the credibility of the testing. This brings a series of hidden dangers, which has been reflected in the chapter 2.1 and the chapter 2.2. The test method is embodied in the test generator. The following chapters are the detailed analysis of the characteristics of the test generator specified in the current standards.

## 2.4 Shunt Impedance based Voltage Sags Generator

### 2.4.1 Topology and Characteristics

According to the test standard, for example, GB/T 19963-2011: <Technical rule for connecting wind farm to power system>, the Shunt Impedance based Voltage Sags Generator (SI-VSG) is the first choice of the test generator in LVRT testing. Figure 2-14 describes the equivalent circuit of the SI-VSG.

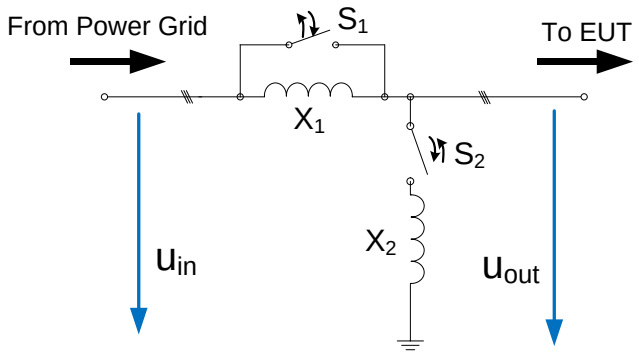



**Figure 2-14; Equivalent circuit of the SI-VSG**

In Figure 2-14, generally the input of SI-VSG $U_{in}$ is the public grid. The output voltage of SI-VSG is $U_{out}$. $X_1$ is the current-limiting inductor and $X_2$ is grounding inductor. The amplitude of the output voltage is controlled by the state of the switches $S_1$ and $S_2$. When the switch $S_1$ is closed and the switch $S_2$ is opened, the output voltage $U_{out}$ is equal to the grid voltage $U_{in}$. When the switch $S_1$ is opened and the switch $S_2$ is closed, the output voltage $U_{out}$ is shown in Eq. 2-8, which is the assuming that, the short circuit capacity of the power grid is infinitive and the output current of the EUT is zero.

$$u_{out}(t) = \frac{X_2}{X_1 + X_2} u_{in}(t) \qquad \text{Eq. 2-8}$$

As can be seen in the Eq. 2-8, the SI-VSG is a voltage divider. The input voltage is proportional to the output voltage.

A SI-VSG should also protect the public grid which it connected during the LVRT testing, that means: the short circuit capacity at the test points shall be at least 3 times to 10 times the rated capacity of the EUT according to testing standard <IEC61000-4-11>, and the voltage deviation of the grid caused by voltage dips should be allowed in the range of rated voltage deviation.

Calculation for the current-limiting inductor is carried out by using the Eq. 2-9:

$$X_1 = \frac{U_{EUT}^2}{nS_{EUT}}$$ Eq. 2-9

$U_{EUT}$… Rated output voltage of EUT;

$S_{EUT}$… Rated power voltage of EUT;

n… Coefficient of the proportion from the short-circuit capacity of the test point to the EUT.

For example, if the rated voltage of EUT is 35 kV, the rated power of EUT is 1.5 MVA, and the short-circuit capacity of the test point is set to 4 times of the EUT, $X_1$ is 204 Ω. This exceeds the real grid impedances by far. When the system impedances is far greater than the normal system impedances, the stable operation of the EUT will be greatly affected, which is mentioned in chapter 2.2.2.

### 2.4.2 Difference Influence Between a Shunt Impedance based Voltage Sags Generator and Real Power Systems

The dynamic characteristic of SI-VSG is different from the real power systems. These difference are caused by retroactive effects, system impedances and so on. This is shown in Figure 2-15, the output voltage curve from SI-VSG has a large difference to the real grid fault.

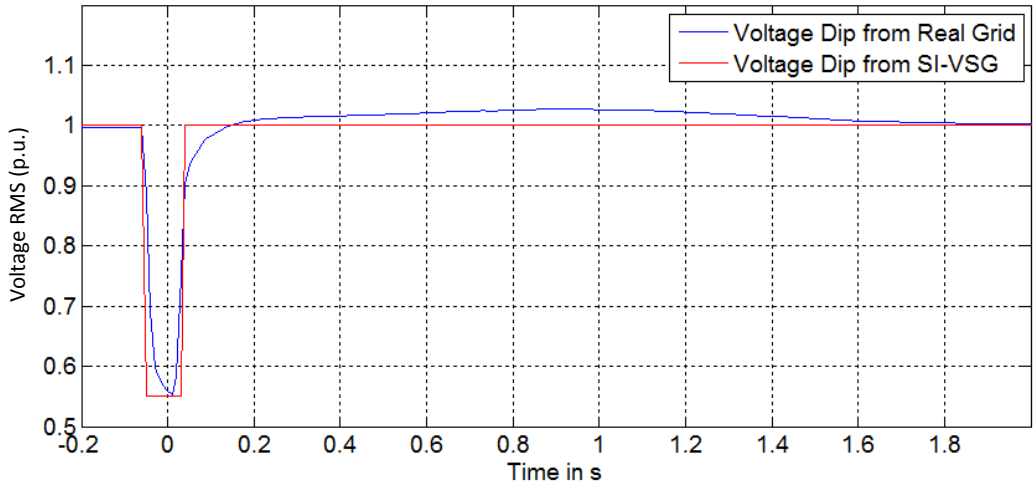



**Figure 2-15; Voltage dip curve of the SI-VSG and the real grid**

This is shown in Figure 2-15, the red curve presents the voltage dip curve from SI-VSG, the blue curve is from the fault records of the voltage dip in a 400 kV grid. It can be seen difference, such as the real voltage dip curve is not a rectangular curve.

### 2.4.2.1 Lack of Dynamic Response from Neighboring Distributed Generation Systems

The SI-VSG is unable to reproduce the dynamic response from neighboring DG systems. That is the voltage amplitude oscillation which is mentioned in chapter 2.2.1. As the SI-VSG is a voltage divider, the output voltage is proportional to the input voltage, so when the grid voltage is stable, the SI-VSG will not produce an oscillating output voltage.

Due to the existence of the current limiting inductor $X_1$, it has only a confined impact to a power system. Therefore, there is a system based de-coupling between the EUT and other possibly oscillating sources. It cannot produce the millisecond class dynamic response caused by the real grid fault situation.

Taking the voltage dip curve of Figure 2-4 in chapter 2.2.1 as an example, the Figure 2-16 shows the comparison between SI-VSG and the complex grid with neighboring DG systems.

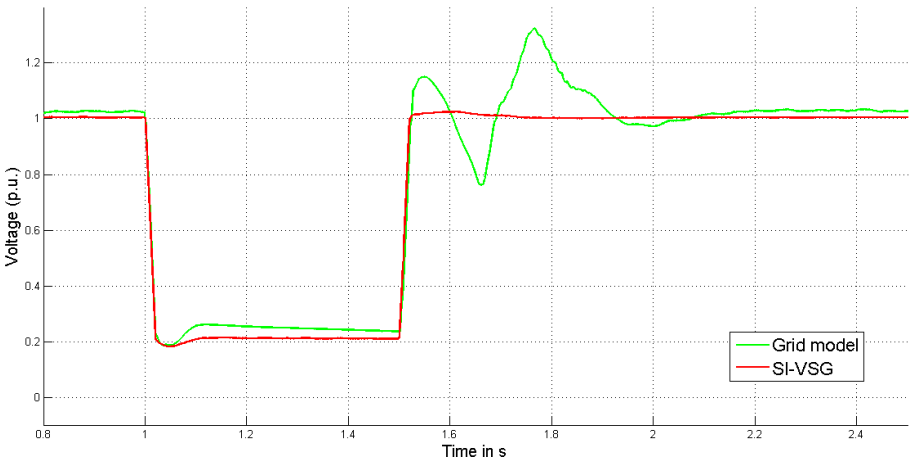



**Figure 2-16; Comparison between SI-VSG and the complex grid with neighboring DG systems**

Figure 2-16 shows that during voltage dip, there is not much difference between SI-VSG and the complex grid. But the voltage dip, the difference between those is very large. Due to the neighboring DG systems, there is a significant voltage amplitude oscillation. In this case, overvoltage tripping might occur, depending on the protection setting of the DG and the de-coupling devices. In this case, overvoltage tripping might occur, depending on the protection settings of the DG system and the de-coupling devices.

### 2.4.2.2 Large System Impedances

According to the chapter 2.2.2, the large grid impedances may lead to the instability of the DG system. This is shown in Figure 2-17, the SI-VSG is used to test the LVRT ability of a wind turbine, the control of the current waveform is unstable due to the large system impedances.

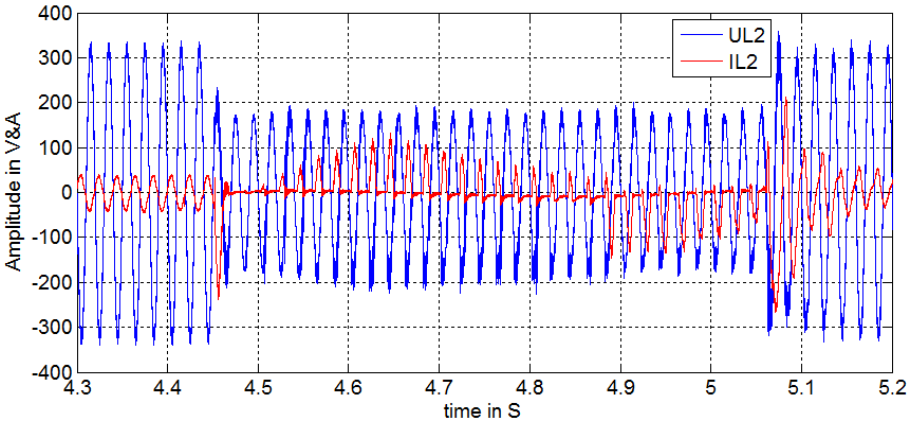



**Figure 2-17; LVRT testing for a wind turbine use SI-VSG**

Figure 2-17 shows the output voltage and current waveform (Phase B / L2) of EUT during a LVRT testing of a wind power generation system. The rated power of this wind power generation system is 100 kVA. The short-circuit capacity of SI-VSG is 400 kVA. The residual voltage is 0.5 p.u., the duration is 625 ms. During the voltage dip, there is the distortion of the output current waveform. This indicates that the control of the current waveform is unstable.

In addition, when the output current of the EUT oscillates, this will cause voltage oscillations at the PCC of the EUT, as seen the Eq. 2-10. The voltage amplitude oscillation is proportional to the impedance of SI-VSG.

$$u_{EUT}(t) = Z_{SI-VSG} i_{EUT}(t) \qquad \text{Eq. 2-10}$$

The voltage oscillations will further exacerbate the current oscillations, which may also lead the destabilize of the EUT. In addition, due to the large system impedances, SI-VSG will produce large voltage harmonics at the beginning of the voltage dip. These harmonics can cause the failing of the phase locked loop in the controller of EUT, which causes the destabilization of the control. It may also trigger the protection function of EUT, such as over/under-frequency protection and some anti-islanding protection algorithms [30]. The peak value of voltage harmonics may even trigger the transient overvoltage protection of EUT.

Therefore, when certain test organizations carry out the LVRT testing with the SI-VSG, the EUT will be allowed to block other protection procedures and only test the LVRT function of the EUT. In order to avoid triggering other protection during the LVRT testing, let the EUT shut down. But in a real power system, the voltage waveform distortion and voltage oscillations caused by the voltage dips exist, but in a lesser degree because of the lower system impedance. This method, which with SI-VSG and blocking of protection functions, cannot be used to comprehensively test the response of the EUT. It may cause such a case as in [3], where EUT passed the test of LVRT testing with SI-VSG, but in the face of real grid voltage dips, it never the less cannot ride through.

## 2.5 Ideal Voltage Source

According to the recommendation from the standards, such as GB/T 19939-2005: <Technical requirements for grid connection of PV system>, the grid compatibility testing of the DG system can also be done by using the ideal voltage source. The output voltage of an ideal voltage source is independent of its load current. Its output voltage u(t) is linear to the reference signal $u_{ref}(s)$. Figure 2-18 describes the principle of the ideal voltage source.

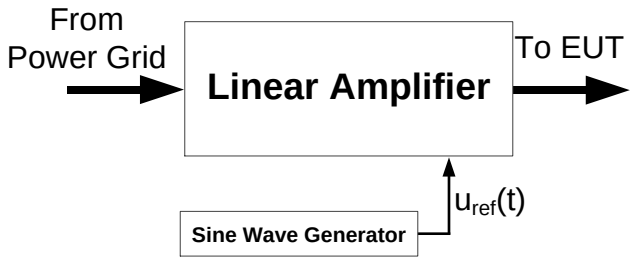



**Figure 2-18; Principle of the ideal voltage source**

The ideal voltage source is equivalent to a linear amplifier in Figure 2-18. The given reference generated by a sinusoidal wave generator.

The output voltage waveform of the linear amplifier can be controlled by setting the voltage amplitude, frequency and phase angle. These parameters can be set to a constant, or a step function. When the voltage amplitude is set to a piecewise function, it can generate a voltage dip waveform, the example is shown in Figure 2-19.

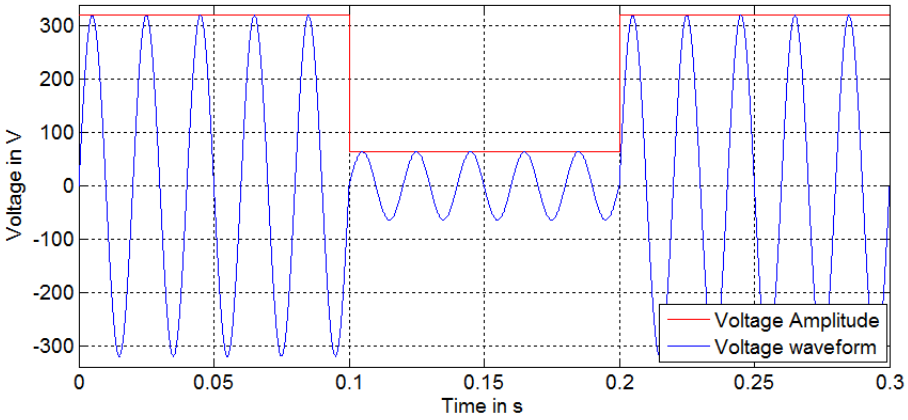



**Figure 2-19; Amplitude curve and waveform of the ideal voltage source**

Theoretically, the output voltage of ideal voltage source will not be affected by the load current, and the influence of the load current should be suppressed through the control software. In fact, due to the hardware and the limitation of the accuracy of the control software, which in a linear case would be equivalent to a small output impedance. But because of this effect is very small, so it can still be regarded as an ideal voltage source.

Due to the very small influence of the current upon the voltage waveform, it can be regarded as a very large short-circuit capacity.

According to the research on the influence of the grid impedances to DG system in the chapter 2.2, the EUT has now a very good performance of stabilization, thus the EUT can easily pass the grid compatibility testing.

In the real power systems however, the DG systems are usually connected to the end of the grid, the grid impedances caused by the transformer and long transmission lines cannot be ignored. Therefore, the ideal voltage source with very small system impedances cannot reproduce the real grid environment.

The test result with an ideal voltage source is shown in Figure 2-20. The details of this testing are presented in chapter 6.3.

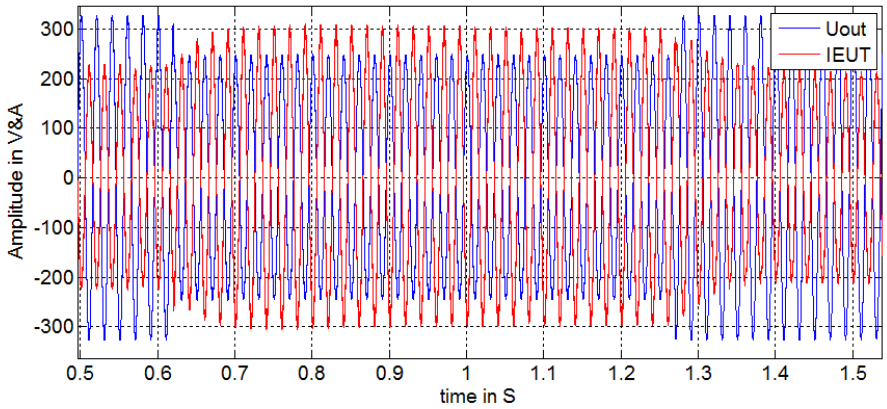



**Figure 2-20; Test result with an ideal voltage source**

This is shown in Figure 2-20, the blue curve represents the voltage dip waveform from the ideal voltage source, the residual voltage is 0.75 p.u. and the duration is 625 ms. The output current (red curve) from EUT is smoothly increased during the voltage dip, and gradually decrease after the voltage dip. During the test, the current waveform has no observable distortion. Due to the small grid impedances in this test, this DG system is stable.

A LVRT testing with the same test condition is carried out on the same EUT with the real grid environment (see chapter 6.3). The test result is shown in Figure 2-21.

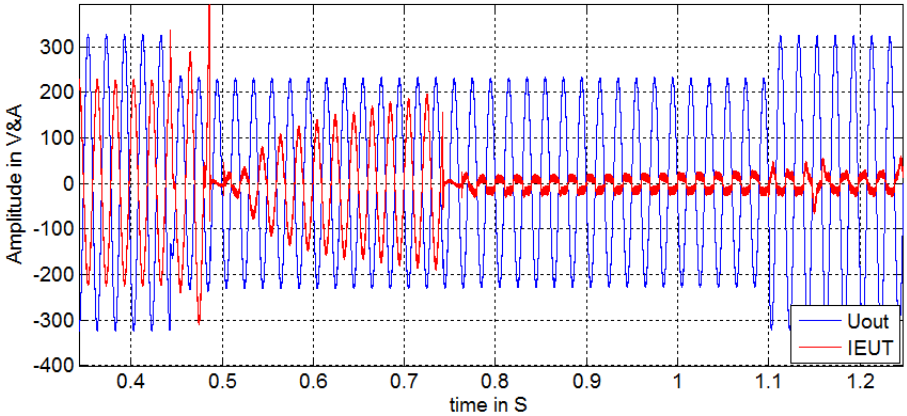



**Figure 2-21; Test result with real grid environment**

This is shown in Figure 2-21, during the voltage dip, the output current (red curve) from EUT is changing dramatically. At the beginning of the voltage dip (0.45s), the output current suddenly is increased and drops to zeros at 0.48s. In 0.75s, the current waveform gets out of control. Due to the influence of the grid impedances and the retroactive effects which are mentioned in the chapter 2.2, this makes the operation of the EUT unstable.

Therefore, the grid compatibility testing with the ideal voltage source cannot reproduce the impact on EUT caused by real grid impedance. The testing under the ideal grid environment reduces the difficulty of the grid compatibility test, and reduces the credibility of the test.

## 2.6 Summary of this Chapter

This chapter focuses on the problem, that the DG system passed the fault ride through ability testing, but when a real grid failure occurs, the DG system cannot ride through the fault. In this chapter, the difference between the real grid situation and test methods and the test generators from the present standards is systematic analyzed and studied.

The voltage amplitude oscillations caused by the cluster of distributed generation systems, the resonance phenomena and the real impedances will affect the grid-connected performance of the DG system. The test methods and the test generator from the present standards are unable to reproduce these situations.

In case of SI-VSG, too large system impedances of the SI-VSG resulted in the too large dynamic response, which makes the grid compatibility testing too difficult. It is also too simple to use the ideal voltage source in the testing too easy. Both reduce the reliability and credibility of the testing.

This thesis proposes the test method and test generator based on Power Hardware-in-the-Loop, it tests the EUT as in different real grid environments, to simulate the real behavior of the health grid operations and the real grid fault. According to the existing test standards, combined with the testing of both the type certification and the project certification, the design of the EUT will be verified in the real electrical network conditions, which generated by the Power Hardware-in-the-Loop test system.

# 3 Power Hardware-in-the-Loop Test System

## 3.1 Introduction

The Hardware-in-the-Loop (HIL) test system can give the EUT any realistic testing environment. The actual response of the EUT can be tested before the EUT goes into service. Some extreme test conditions can be easily reproduced in the HIL testing. This can save a lot of cost and reduce the risk of damage to the EUT.

The operation of the HIL test is realized by the simulation model software in the real-time simulator, and the HIL interface, which is used to the information interchange or power exchange between the EUT and the simulation model software. The general principle of the HIL test can be seen in Figure 3-1.

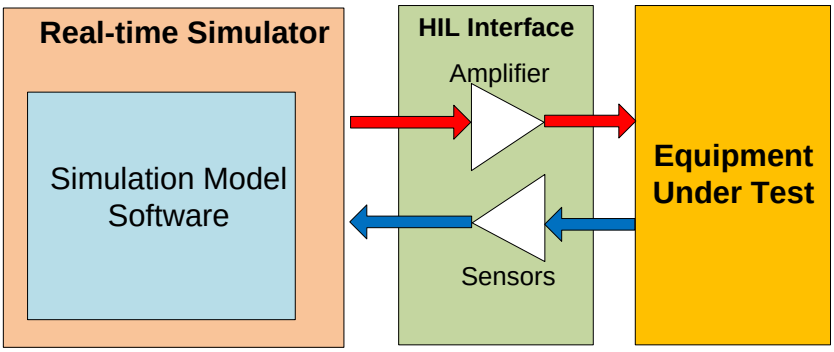



**Figure 3-1; General principle of the HIL test**

### 3.1.1 Controller Hardware-in-the-Loop Test

The EUT of Controller Hardware-in-the-Loop (CHIL) test is the controller of the DG systems itself. The controller is actually built and programmed, and the numerical model of the hardware of the DG system is simulated in a Real-Time Simulator (RTS) (Figure 3-2, left). Through the CHIL interface, the controller controls the model of the hardware of the DG system in the RTS.

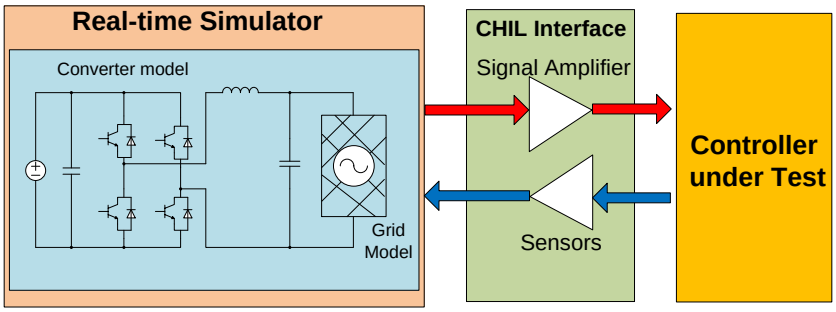



**Figure 3-2; Principle of the CHIL test**

### 3.1.2 Power Hardware-in-the-Loop Test

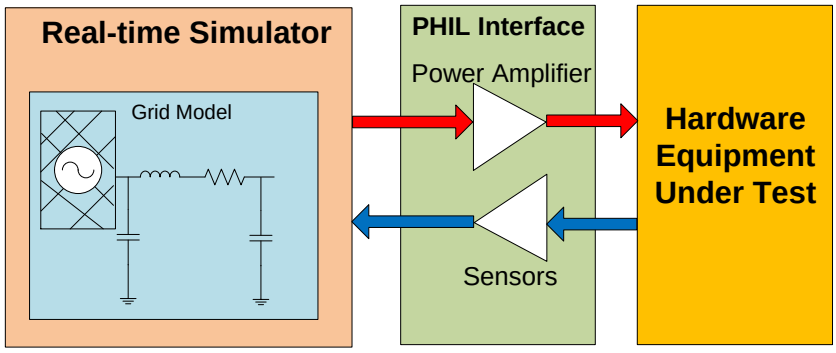



**Figure 3-3; Principle of the PHIL test**

The EUT in case of a PHIL test system is the complete DG system. Since the signal and power exchange between the EUT and an RTS is through high-power signals, the PHIL interface is required (Figure 3-3, green box). The PHIL interface is responsible for converting the power signal from the EUT to a low power signal for the RTS through the sensors, simultaneously converting the low power signal from RTS through the power amplifier to generate a high power signal for EUT.

The RTS, power amplifiers and sensors will inevitably lead to a system delay problem. This problem will affect the accuracy and stability of the real-time simulation.

In this chapter, the operation sequence and the time delay of the three units will be analyzed, the precondition of the stability of the PHIL test system will be given (chapter 3.2). Then the accuracy and stability of the PHIL interface algorithm will be analyzed and improved, so that the PHIL interface algorithm can provide high accuracy and stable operation in the case of time delays and signal distortions (chapter 3.3, 3.4). The problems resulting form high latency in the high power PHIL test will be analyzed, and the algorithm of delay compensation will be presented (chapter 3.5). Also, the requirement analyses of the PHIL test system will be carried out (chapter 3.6).

## 3.2 Operation Sequence and Time Delays in Real-time Simulation

The operation sequence of the PHIL test can be divided into three phases:

1. **Measurement and sampling phase**: the voltages and currents are measured by the sensors, then channeled through the sampling circuit and AD conversion circuit, to the input to the real-time simulator.
2. **Real-time calculation phase (RTC)**: the input voltage and current signals are used as boundary conditions of real-time calculation. From this, the grid model state and the variables of the next time step will be calculated in the simulation step.

3. **Power amplify phase**: the numerical calculation results will be sent through the D/A into analog (or through digital communications) to the power amplifier controller as a reference signal. The power amplifier will amplify this reference signal into a power signal, as the boundary conditions in the physical operation of the EUT.

A process that these three phases complete once in sequence is defined as one frame of the PHIL simulation. There are two kinds of operation sequence in the real-time simulation: serial sequence and non-serial sequence.

### 3.2.1 Serial Sequence

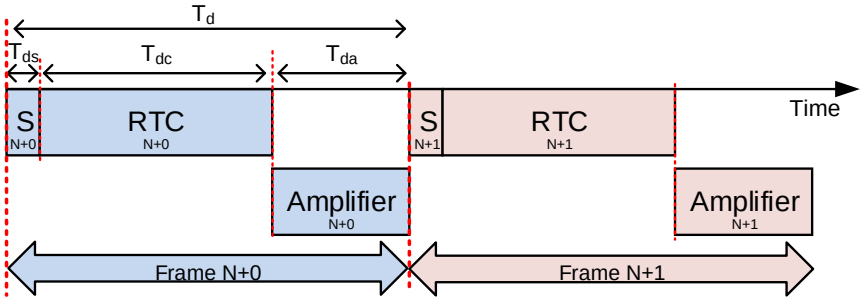



**Figure 3-4; Serial sequence**

In the Figure 3-4, the “S” block represents the measurement and sampling phase, and its running time is $T_{ds}$. The “RTC” block represents the real-time calculation phase, and its running time is $T_{dc}$ (i.e., simulation step size). The “Amplifier” block represents the power amplifying phase, its running time is $T_{da}$.

The “S” and “RTC” phases will not overlap in practical applications. Therefore, the “S” phase and the “RTC” phase can be considered as one phase. The “S” and “RTC” phase should be synchronized with the “Amplifier” phase, in order to avoid the overlap between those phases.

The delay of the power amplifier $T_{da}$ is caused by the calculation step of the controller in power amplifier. This delay $T_{da}$ does not contain the delay caused by the phase shift from the power amplifier hardware. Detailed discussion can be found in chapter 3.5.

The running time of one frame of the PHIL simulation is the system delay:

$$T_d = T_{ds} + T_{dc} + T_{da} \qquad \text{Eq. 3-1}$$

In the serial sequence, these three phases operate in sequence (1-2-3). The end of one frame is the beginning of the next frame. There is no overlap between the two adjacent frames.

### 3.2.2 Non-serial Sequence

When there is an overlap between the two adjacent frames, this is a non-serial sequence, as shown in Figure 3-5.

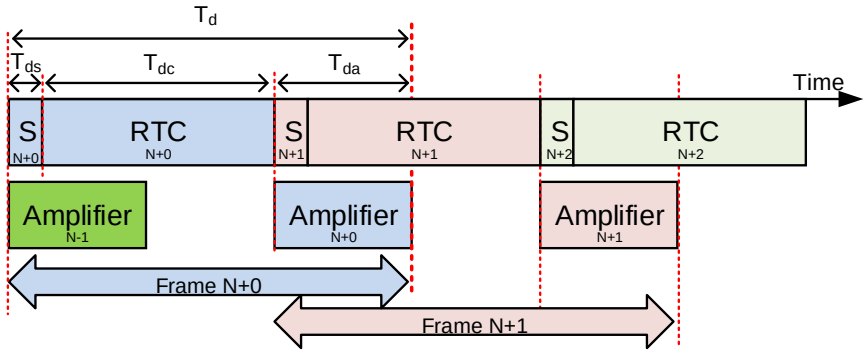



**Figure 3-5; Non-serial sequence**

Figure 3-5 shows the operation schedule of the non-serial sequence. After the “RTC” phase ($RTC_{N+0}$), the “S” phase ($S_{N+1}$) of the next frame (N+1) and the “Amplifier” phase ($Amplifier_{N+0}$) of this frame (N+0) begin in same time.

In the non-serial sequence, the “S” and “RTC” phase not have to be synchronized with the “Amplifier” phase. After “RTC” phase, the reference signal will be sent to the power amplifier. Otherwise, if no new reference signal is sent, the power amplifier will keep the previous state.

The Figure 3-6 shows the operation schedule of the non-serial sequence, when the $T_{da}$ is longer than $T_{ds}+T_{dc}$. That is, the running time of the “Amplifier” phase is longer than the sum of the “S” and “RTC” phase.

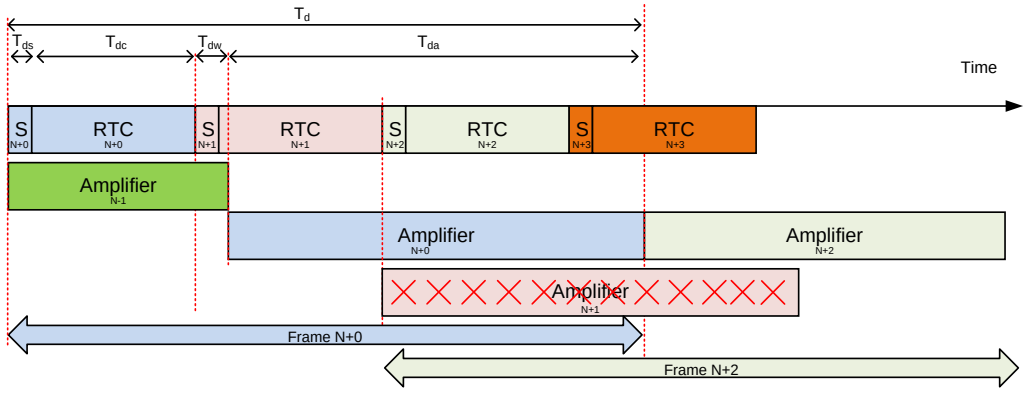



**Figure 3-6; Non-serial sequence ($T_{da}>T_{ds}+T_{dc}$) in the LIFO method**

This is shown in Figure 3-6, when the “RTC” phase ($RTC_{N+0}$) has been completed, the “Amplifier” phase ($Amplifier_{N-1}$) is still not yet finished, the execution of the “Amplifier” phase ($Amplifier_{N-0}$) must be waited for $T_{dw}$. When the Amplifier phase ($Amplifier_{N-0}$) is finished, both “RTC” phases ($RTC_{N+1}$) and ($RTC_{N+2}$) are already finished. If the power amplifier uses the LIFO (last-in, first-out) method, then only the last update of the calculation results from “RTC” will be used in power amplifier. The N+1 frame is ignored.

When the power amplifier uses the FIFO (first-in, first-out) method, the first update of the calculation results from RTS will be used in the power amplifier. This ensures that each frame is executed, but the system delay will gradually become larger. This is shown in Figure 3-7.

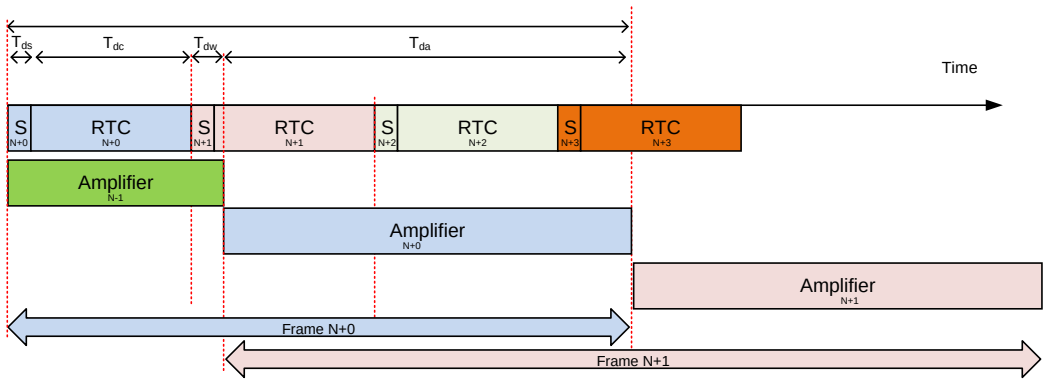



**Figure 3-7; Non-serial sequence ($T_{da}$>$T_{ds}$+$T_{dc}$) in the FIFO method**

Take $T_{ds}$+$T_{dc}$ = 100 µs and $T_{da}$=150 µs as an example, then the length of each frame in LIFO and FIFO method is shown in Figure 3-8.

In FIFO method, the frame length increases with the number of frames, this will cause loss of stability of the system. In LIFO method, the frame length changes and some frames are ignored. This will weaken the accuracy and stability performance of the system.

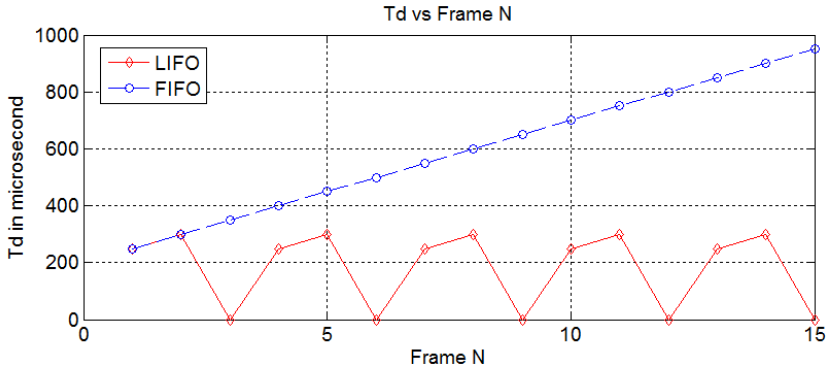



**Figure 3-8; Length of each frame in the LIFO and the FIFO method**

In order to ensure the stable operation of the system, the sum $T_{ds}$+$T_{dc}$ must be greater than or equal to the $T_{da}$. That is the precondition of the stability of the PHIL test system:

$$T_{ds} + T_{dc} \geq T_{da} \qquad \text{Eq. 3-2}$$

The delay from the measurement and sampling phase $T_{ds}$ is very small, the main delay in the system is caused by the real-time calculation phase and the power amplify phase. In order to enhance the accuracy of the system, the smaller $T_{dc}$ is the better. But this is limited by the performance of the computer, so the calculation step $T_{dc}$ in practical is has a lower limit.

A low power linear power amplifier has a very small $T_{da}$ (such as 10 µs), then the Eq. 3-2 can be easily met. Due to the limitation of the switching frequency, the power amplifier based on

power electronics with large output power has usually a large $T_{da}$. In order to meet the Eq.3-2, the calculation step $T_{dc}$ should be increased, but it will also increase the total system delay.

### 3.2.3 Optimization of the Operation Sequence

In the serial mode, the “RTC” and “Amplifier” phases are required to be synchronized, in order to avoid an overlap between those phases. The synchronization between real-time simulator and power amplifier usually needs to be realized through an external trigger. Due to the communication interference and delay, the external synchronous communication may cause the different length of each frame and reduces the stability performance of the system. In addition, the computing power of the real-time simulator is wasted, as shown in Figure 3-4. After the “RTC” phase, the real-time simulator idles until the Amplifier phase is finished. For the non-serial mode, it is difficult to meet the $T_{ds}+T_{dc} \geqq T_{da}$ in the high power PHIL test system. Therefore, it cannot be guaranteed that, the stable operation of the PHIL test system with non-serial sequence is obtained.

In this thesis, an optimization of the operation sequence is presented. This operation sequence inserts the “Amplifier” phase into the “RTC” phase. That is, the real-time simulator is responsible for the calculation of the grid model, and also for the control software of the power amplifier, as shown in Figure 3-9.

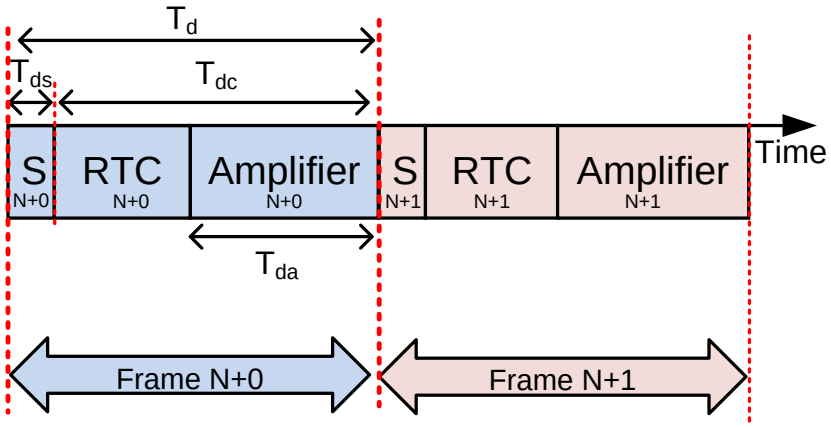



**Figure 3-9; Optimization of the operation sequence**

The calculation results of the grid model will be directly transferred to the control software of the power amplifier, which through the read/write operation of the register in real-time simulator. So it will not have any delay and signal distortion. In addition, due to the advantages of a real-time simulator in floating point calculation, the complex control software can be used in the power amplifier to meet the requirements of high accuracy and fast response speed of the PHIL test system.

The optimized operation sequence reduces the system delay and improves the utilization rate of the real-time simulator. It is suitable for a high power PHIL test system.

## 3.3 Ideal Transformer Method

The PHIL interface algorithm is responsible for the interaction between the physical side (EUT) and the software side (numerical grid model) by the sensors and the power amplifier. The accuracy and stability problem of the system, which is caused by the limitation of the hardware of high power PHIL test system (such as delay, bandwidth, noise, etc.), can be improved by the suitable PHIL interface algorithm.

The most classical PHIL interface algorithm is Ideal Transformer Method (ITM) [31]. Because of its simple structure and clear principle, it has been widely used. This chapter will analyze the accuracy and stability of ITM, and present an optimization algorithm for ITM.

### 3.3.1 Principle of the Ideal Transformer Method

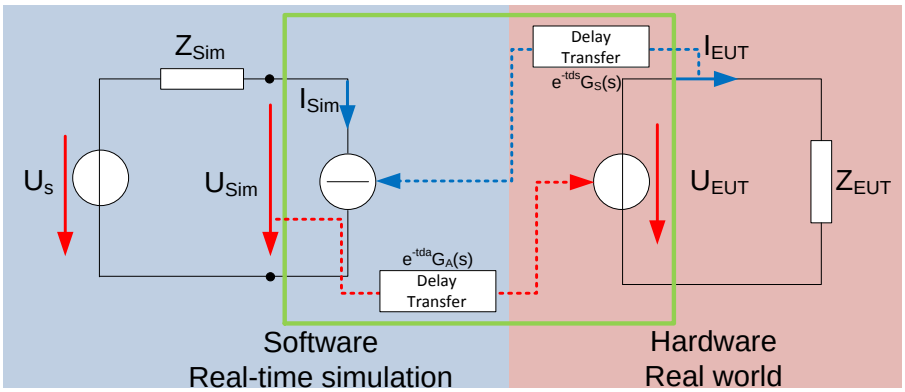



**Figure 3-10; Principle of the Ideal Transformer Method**

The principle of ITM is shown in Figure 3-10. In the left side is the software part of the system. $U_s$ is the voltage source of the grid model, $Z_{Sim}$ is the grid impedance of the grid model, $I_{Sim}$ represents the influence of the EUT current upon the grid in the form of a current source. In the right side is the hardware real world. $U_{EUT}$ is the output voltage of the power amplifier. $Z_{EUT}$ is the impedance of the hardware real world. The interaction of the grid model and the hardware real world is realized by the PHIL interface (green box in Figure 3-10). The output voltage signal of the grid model is fed to the EUT, and the current signal of EUT will be feedback to the grid model by the simulating current source.

The voltage signal $U_{Sim}$ from the software side is transmitted to the physical world through the power amplifier, and becomes $U_{EUT}$. Due to the control software and hardware of the power amplifier, this signal transmission has delays and distortions.

In the operation of the real-time simulator, the calculation results are only be given out when the run time is equal to the simulation step, so the simulation step is the delay between the input and the output of the real-time simulator.

This delay is considered in the study of the relationship between the amplifier and the real time simulator. It is presented in the frequency domain as follows:

$$U_{EUT}(s) = e^{-st_{dc}} e^{-st_{da}} G_A(s) U_{Sim}(s) \quad \text{Eq. 3-3}$$

$t_{da}$… Delay caused by the controller of the power amplifier;

$t_{dc}$… Delay caused by real-time simulator, also simulation step;

$G_A(s)$ … Transfer function of the power amplifier after deduction of the signal delay.

The current signal $i_{EUT}$ from the hardware side is transmitted to the numerical grid model in real-time simulator through the sensors, sampling circuits and the ADC of the real-time simulator. So there is also a delay and distortion in the signal transmission. It is presented in the frequency domain as follows:

$$I_{Sim}(s) = e^{-st_{ds}} G_S(s) I_{EUT}(s) \quad \text{Eq. 3-4}$$

$t_{ds}$… Delay caused by the sensors, sampling circuits and the ADC;

$G_s(s)$ … Transfer function of the sensors, sampling circuits and the ADC after deduction of signal delay.

According to Kirchhoff's second law, the frequency domain of the circuit equation of the grid model is presented as follows:

$$U_{Sim}(s) = U_S(s) - I_{Sim}(s) Z_{Sim}(s) \quad \text{Eq. 3-5}$$

### 3.3.2 Stability Analysis of the Ideal Transformer Method

The stability analysis of the ITM will be carried out in both the time domain and frequency domain. As introduction of the stability analysis of the ITM in discrete-time domain, the chapter 3.3.2.1 will use the certain simplifications, which all quantitation are real values.

#### 3.3.2.1 Stability Analysis of the Ideal Transformer Method in Time Domain

Since the PHIL test system is discrete, the analysis is carried out in the discrete-time domain.

At time step n, the voltage error (ΔUA[n]) between $U_{Sim}[n]$ to $U_{EUT}[n]$, which is caused by the power amplifier, is presented as follows:

$$\Delta UA[n] = U_{Sim}[n] - U_{EUT}[n] \quad \text{Eq. 3-6}$$

For the convenience of the analysis, the $Z_{EUT}$ and $Z_{Sim}$ are regarded as real constant, and then $I_{EUT}$ is:

$$I_{EUT}[n] = \frac{U_{EUT}[n]}{Z_{EUT}}$$ Eq. 3-7

The current error (ΔIA[n]), which caused by the power amplifier, is presented as follows:

$$\Delta IA[n] = \frac{\Delta UA[n]}{Z_{EUT}}$$ Eq. 3-8

The current error (ΔIS[n]) between $I_{EUT}[n]$ and $I_{Sim}[n]$, which caused by the sensors, is presented as follows:

$$\Delta IS[n] = I_{EUT}[n] - I_{Sim}[n]$$ Eq. 3-9

At time step n+1, the new value of the $U_{sim}$ is:

$$U_{Sim}[n+1] = U_S[n+1] - I_{Sim}[n]Z_{Sim}$$ Eq. 3-10

By inserting the Eq.3-6 ~ Eq.3-9 to Eq.3-10, get the voltage error ($\Delta U_{Sim}$) at time step n+1. This is caused by both the power amplifier and the sensors, is presented as follows:

$$\Delta U_{Sim}[n+1] = -\frac{Z_{Sim}}{Z_{EUT}} \Delta UA[n] \Delta IS[n]$$ Eq. 3-11

In the Eq3-11, $-Z_{Sim}/Z_{EUT}$ is the error transfer coefficient. If the absolute value of the error transfer coefficient is greater than 1 ($|Z_{Sim}/Z_{EUT}| > 1$), the error will be expanded and results in destabilizing of the system. When the absolute value of the error transfer coefficient is less than 1 ($|Z_{Sim}/Z_{EUT}| < 1$), the error will converge and the system will be stable.

By the above analysis, the stability of the PHIL test system is rated to the impedance in the software and hardware side. The PHIL test system will be unstable when the impedance of the software side is greater than the impedance of the hardware side.

In order to carry out a quantitative analysis of the stability of the system, the following analyses are made in the frequency domain.

### 3.3.2.2 Stability Analysis of the Ideal Transformer Method in Frequency Domain

The block diagram is obtained by Eq.3-4 ~ Eq.3-6 and shown in

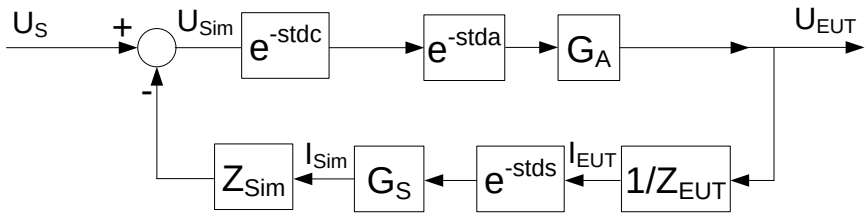



**Figure 3-11; Block diagram of the Ideal Transformer Method**

The complete closed loop transfer function of the ITM PHIL test system can be obtained from the Figure 3-11.

$$G_{ITM\_CL}(s)=\frac{U_{EUT}(s)}{U_S(s)}=\frac{e^{-st_{dc}}e^{-st_{da}}G_A(s)Z_{EUT}(s)}{e^{-st_{ds}}e^{-st_{dc}}e^{-st_{da}}G_S(s)Z_{Sim}(s)+Z_{EUT}(s)} \quad \text{Eq. 3-12}$$

And also the open loop transfer function:

$$G_{ITM\_OL}(s)=-e^{-st_{ds}}e^{-st_{da}}e^{-st_{dc}}G_A(s)G_S(s)\frac{Z_{Sim}(s)}{Z_{EUT}(s)} \quad \text{Eq. 3-13}$$

In order to facilitate the analysis, the assumption is made that the signal transfers through the sensors and power amplifier has a unit gain.

$$\begin{cases}G_A(s)=1\\G_S(s)=1\end{cases} \quad \text{Eq. 3-14}$$

The combination of those delays yields:

$$t_d=t_{da}+t_{ds}+t_{dc} \quad \text{Eq. 3-15}$$

Then the open loop transfer function is simplified into:

$$G_{ITM\_OL}(s)=-e^{t_d}\frac{Z_{Sim}(s)}{Z_{EUT}(s)} \quad \text{Eq. 3-16}$$

According to the Nyquist stability criterion, the stability of the system can be determined by observing the Nyquist curve of the open loop transfer function. The number of poles of the open loop transfer function in the right half plane must be equal to the number of the anti-clockwise circling of the Nyquist curve around (-1, j0).

The influence of the impedances on the stability of the system is analyzed by two cases. In these cases, $Z_{Sim}$ and $Z_{EUT}$ are both resistance and inductor in series. Their parameters are as shown in Table 3-1. Case1 is $|Z_{Sim}/Z_{EUT}|>1$, Case 2 is $|Z_{Sim}/Z_{EUT}|<1$. The number of poles of the open loop transfer function in the right half plane in both cases is zero.

| | **Case 1** | | **Case 2** | |
|---|---|---|---|---|
| **$t_d$** | 100 µs | | 100 µs | |
| | $Z_{Sim}$ | $Z_{EUT}$ | $Z_{Sim}$ | $Z_{EUT}$ |
| **R** | 2 Ω | 1 Ω | 1 Ω | 2 Ω |
| **L** | 2 mH | 1 mH | 1 mH | 2 mH |

**Table 3-1; Parameters of Case 1 and Case 2**

From these data, the Nyquist curve is obtained, see Figure 3-12.

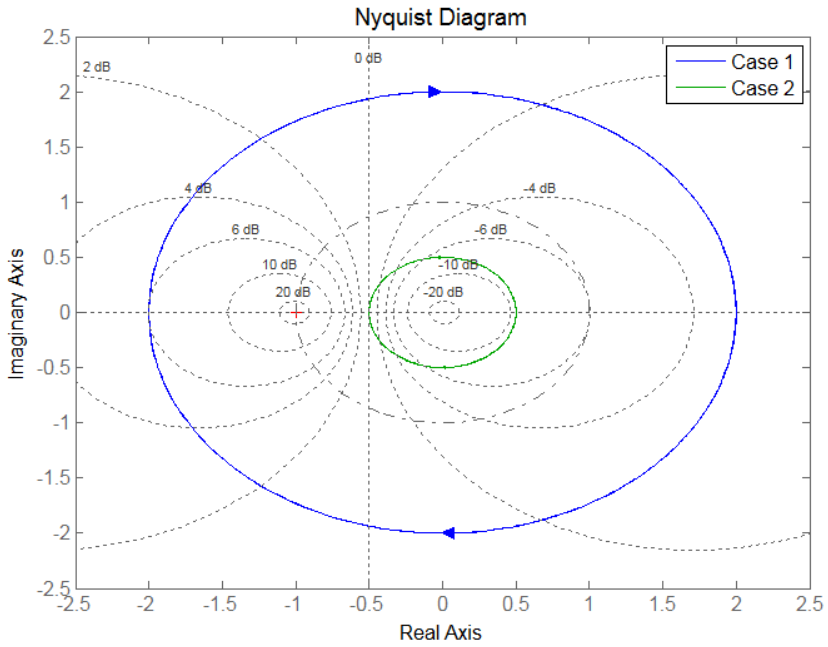



**Figure 3-12; Nyquist curve of Case 1 and Case 2 in ITM**

This is shown in Figure 3-12, the Nyquist curve of Case 1 (blue curve) is a circle including the point (-1, j0). According to the Nyquist stability criterion, this system is unstable. The Nyquist curve of Case 2 (green curve) does not circle around (-1, j0), so this system is stable. The same conclusion can be obtained in frequency domain analysis. The PHIL test system will be unstable when the impedance of the software side is greater than the impedance of the hardware side.

In order to get the detailed conditions of the stability of the system, the Ruth-Hurwitz rule is used.

From Eq.3-16 the characteristic equation of the closed loop transfer function is obtained:

$$e^{-st_d} Z_{Sim}(s) + Z_{EUT}(s) = 0 \qquad \text{Eq. 3-17}$$

With:

$$\begin{cases} Z_{Sim}(s) = R_{Sim} + sL_{Sim} \\ Z_{EUT}(s) = R_{EUT} + sL_{EUT} \end{cases} \qquad \text{Eq. 3-18}$$

Application the first order Padé approximation on the delay component $e^{-std}$ yields:

$$e^{-st_d} = \frac{1 - s\frac{t_d}{2}}{1 + s\frac{t_d}{2}} \qquad \text{Eq. 3-19}$$

By inserting Eq.3-18 and Eq.3-19 into Eq.3-17:

$$t_d(L_{EUT}-L_{Sim})s^2+(R_{EUT}t_d-R_{Sim}t_d+2L_{Sim}+2L_{EUT})s+2R_{EUT}+2R_{Sim}=0 \quad \text{Eq. 3-20}$$

According to the Ruth-Hurwitz rule, when meet the following equations are met, this system is stable.

$$\begin{cases} L_{EUT}-L_{Sim}>0 \\ t_d>-2\dfrac{L_{EUT}+L_{Sim}}{R_{EUT}-R_{Sim}} \end{cases} \quad \text{Eq. 3-21}$$

From the Eq.3-21, the PHIL test system is stable, when the inductance or resistance of the hardware side is greater than the inductance or resistance of the software side. In the case when the resistance of the hardware side is smaller than the resistance of the software side, the system delay $t_d$ must fulfil the Eq.3-21. Therefore, the stability of the system is not only related to the impedance, but also is related to the total delay of the system.

### 3.3.3 Accuracy Analysis of the Ideal Transformer Method

The accuracy analysis is carried out with the closed loop transfer function (Eq.3-12) in frequency domain.

Use the simply in Eq.3-14, and due to the very small delay of the sensors, the $t_{ds}$ can be negligible. Therefore, the system delay is presented as:

$$t_d=t_{da}+t_{ds}+t_{dc}\approx t_{da}+t_{dc} \quad \text{Eq. 3-22}$$

By inserting the Eq.3-14 and Eq.3-22 into Eq.3-12 yields:

$$G_{ITM\_CL}(s)=\frac{U_{EUT}(s)}{U_S(s)}=\frac{e^{-st_d}Z_{EUT}(s)}{e^{-st_d}Z_{Sim}(s)+Z_{EUT}(s)} \quad \text{Eq. 3-23}$$

The closed loop transfer function of the ideal PHIL test system, without delay is:

$$G_{ITM\_Ideal}(s)=\frac{U_{EUT}(s)}{U_S(s)}=\frac{Z_{EUT}(s)}{Z_{Sim}(s)+Z_{EUT}(s)} \quad \text{Eq. 3-24}$$

The relative error of the system in frequency domain is as follows:

$$Error_{ITM}(s)=20\log\left(\left|\frac{G_{ITM\_CL}(s)-G_{ITM\_Ideal}(s)}{G_{ITM\_Ideal}(s)}\right|\right) \quad \text{Eq. 3-25}$$

When using the parameter of impedances in Case 2 in Table 3-1, and set the delays are 10 µs, 50 µs and 100 µs respectively, the resulting relative error of the system in frequency domain is shown in Figure 3-13.

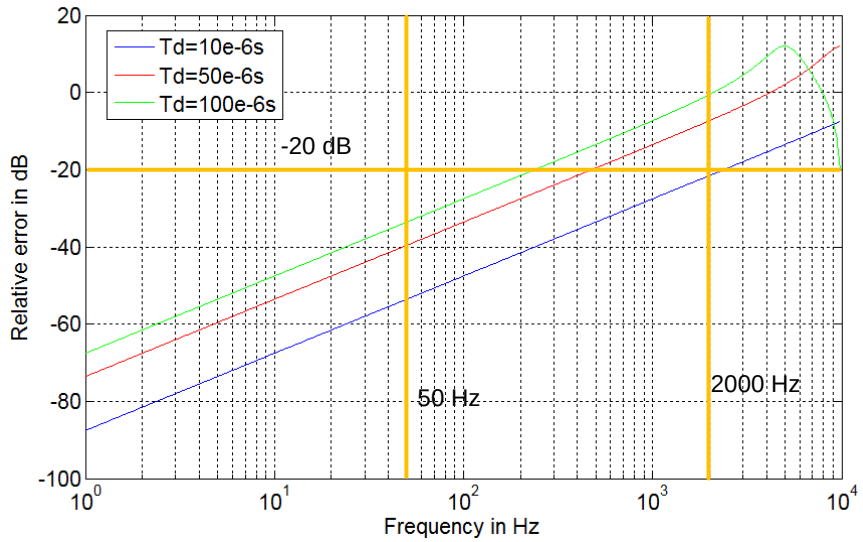



**Figure 3-13; Relative error of the ITM in frequency domain with different $t_d$**

In Figure 3-13**,** the relative error increases with the frequency of the same delay. At the same frequency, the relative error increases with the delay. This reflects the limited operation bandwidth of the PHIL testing system in a certain error tolerance. In this example case, when the frequency is 50 Hz, the relative error is below -20 dB with each of the system delays above. When the frequency is 2000 Hz, the relative error is below -20 dB only with the 10 µs system delay (blue curve).

The relative error can be also affected by the different combinations of impedances. Take the parameters in Table 3-2 as an example.

| | **Case 3** | | **Case 4** | | **Case 5** | |
|---|---|---|---|---|---|---|
| **$t_d$** | 10 µs | | 10 µs | | 10 µs | |
| | $Z_{Sim}$ | $Z_{EUT}$ | $Z_{Sim}$ | $Z_{EUT}$ | $Z_{Sim}$ | $Z_{EUT}$ |
| **R** | 1 Ω | 2 Ω | 1 Ω | 10 Ω | 1 Ω | 100 Ω |
| **L** | 1 mH | 2 mH | 1 mH | 10 mH | 1 mH | 100 mH |

**Table 3-2 Parameters of Case 3, Case 4 and Case 5**

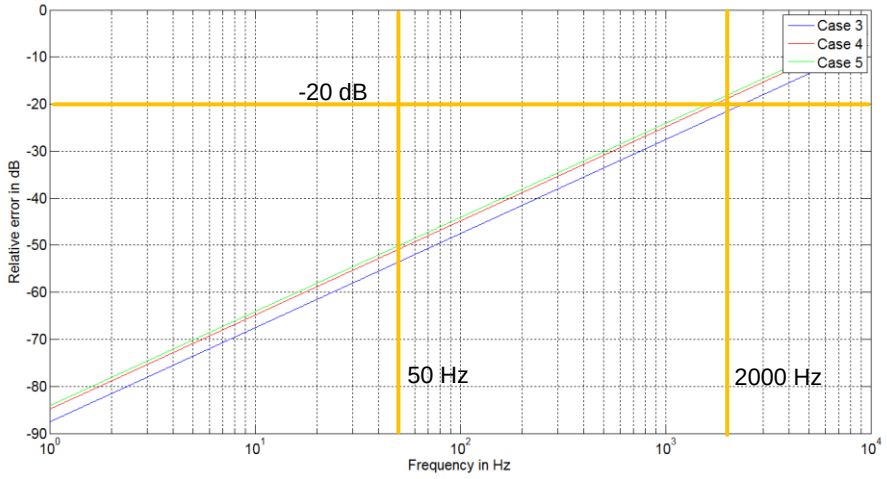



**Figure 3-14; Relative error of the ITM in frequency domain with different combinations of impedances**

This is shown in Figure 3-14, the relative error of Case 3 is the smallest and the relative error of Case 5 is biggest. The difference between the two impedances in Case 3 is the least and the difference between the two impedances in Case 5 is the largest. The following conclusion can be obtained, for the Ideal Transformer Method: Under the premise of keeping the system stable, the smaller the difference between $Z_{EUT}$ and $Z_{Sim}$, the smaller the relative error and the higher the accuracy of the system.

### 3.3.4 Compensation Method of the Ideal Transformer Method

As shown for the Ideal Transformer Method, the accuracy and stability of the system are mainly affected by the delay of the system and the impedances. In order to improve the accuracy and stability of the system, the design and analysis of the compensation method for of Ideal Transformer Method will be carried out in the following chapters.

#### 3.3.4.1 Ideal Transformer Method with Low Pass Filter Method

In the analysis of the accuracy of the ITM (Figure 3-13), the relative error increases with the frequency. The relative error of ITM for high frequencies is very large, so it will seriously degrade the stability of the system. Therefore, a low pass filter can be added in the ITM to suppress the high frequency signal of the PHIL test system, in order to improve the stability of the system, as shown in Figure 3-15.

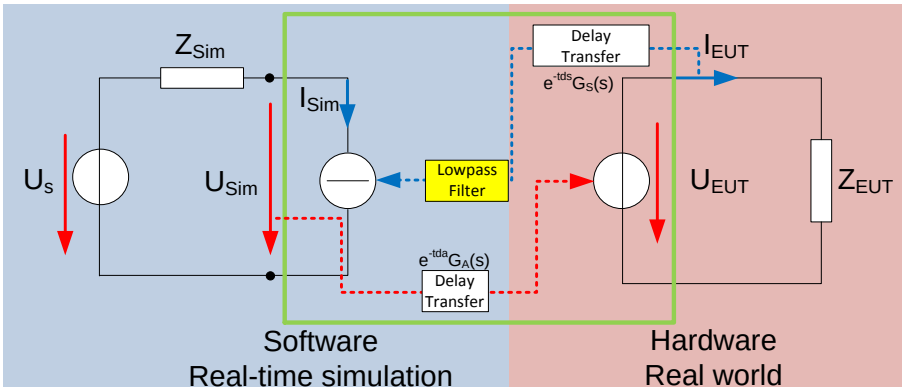



**Figure 3-15; Principle of Ideal Transformer Method with Low pass filter method**

This is shown in Figure 3-15, on the basis of the ITM, a low pass filter (yellow box in Figure 3-15, and the $G_{SLPF}$ in Figure 3-16) is added into the transmission of the current signal. The block diagram of this system is shown in Figure 3-16.

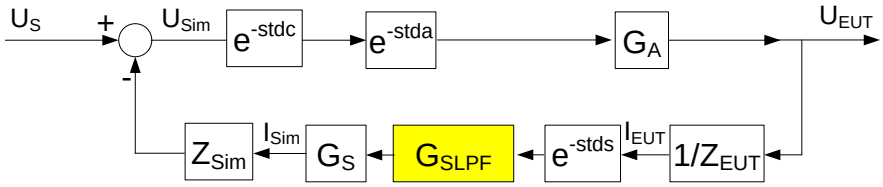



**Figure 3-16; Block diagram of Ideal Transformer Method with Low pass filter method**

With the same simplification in Eq.3-14 and Eq.3-15, the closed loop transfer function is presented as:

$$G_{ITM\_CL}(s) = \frac{U_{EUT}(s)}{U_S(s)} = \frac{e^{-st_d} Z_{EUT}(s)}{e^{-st_d} Z_{Sim}(s) G_{SLPF}(s) + Z_{EUT}(s)} \quad \text{Eq. 3-26}$$

And the open loop transfer function is:

$$G_{ITM\_OL}(s) = e^{-st_d} G_{SLPF}(s) \frac{Z_{Sim}(s)}{Z_{EUT}(s)} \quad \text{Eq. 3-27}$$

$G_{SLPF}(s)$ … Transfer function of the low pass filter on current sensor.

Here the second order low pass filter is used.

$$G_{SLPF}(s) = \frac{1}{(1 + \frac{s}{2\pi f_c})^2} \quad \text{Eq. 3-28}$$

The Bode diagram of $G_{ITM\_CL}(s)$ with cutoff frequency is 500Hz and the parameters in Case 2 is shown in Figure 3-17.

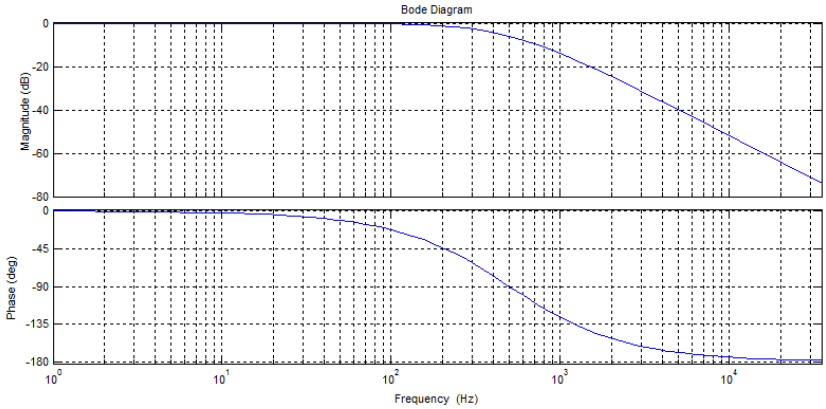



**Figure 3-17; Bode diagram of Ideal Transformer Method with Low pass filter method**

The Nyquist curve of $G_{ITM\_OL}(s)$ with the parameters in Case 1 is shown in Figure 3-18.

This is shown in Figure 3-18, with the same impedance combinations, the Nyquist curve of ITM with Low pass filter (green curve) does no more inculde (-1, j0), so this system is now stable.

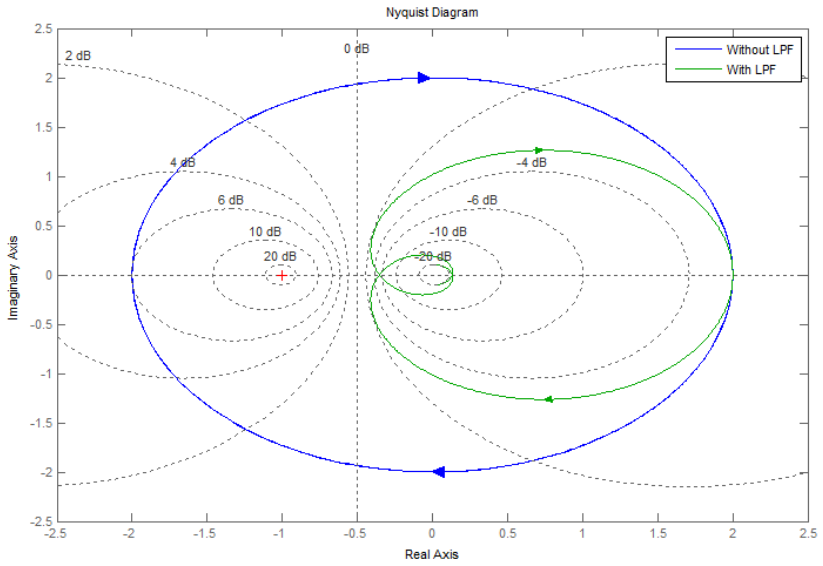



**Figure 3-18; Nyquist curve of Ideal Transformer Method with/without Low pass filter**

In order to get the detailed conditions of the stability of the system, the Ruth-Hurwitz rule is used again. The cutoff frequency of the low pass filter should meet the following equation to make the system stable.

$$f_c < \frac{2}{\pi t_d (k-1)} \qquad \text{Eq. 3-29}$$

k… Ratio of the absolute value of $Z_{Sim}$ and $Z_{EUT}$

Figure 3-19 shows the stability boundary conditions of cutoff frequency of the low pass filter. The values below the curve are stable.

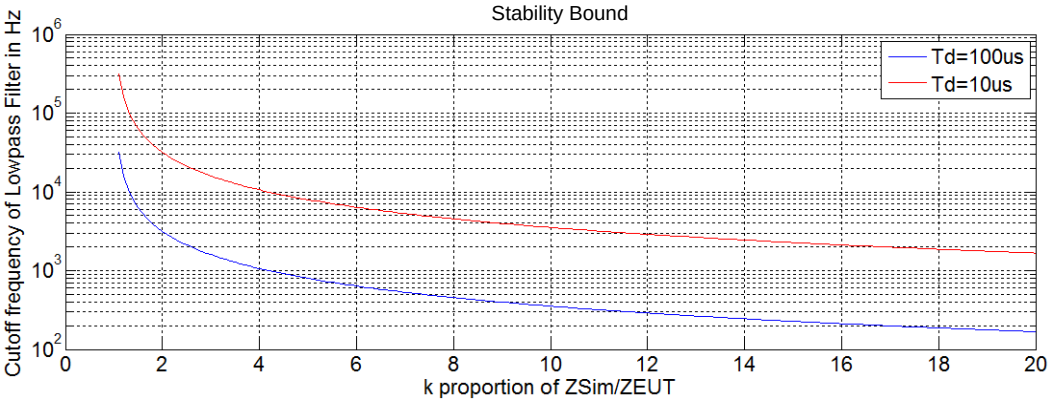



**Figure 3-19; Stability boundary conditions of $f_c$ of the low pass filter in different $t_d$**

According to Figure 3-19, when $t_d$=100 µs and k=2 (Case 1), in order to make the system stable, the cutoff frequency must be to less than 2000 Hz. When k=10, which means that the impedance of software side is far more bigger than in hardware side, in order to make the system stable, the cutoff frequency must be less than 250 Hz. It can also be seen, when the system delay is very small ($t_d$ =10 µs), the cutoff frequency can be higher with the same k.

In order to ensure the stability of the system, a lower cutoff frequency of the low pass filter of the feedback current signal is better. But the lower cutoff frequency will lead on the other hand to a phase shift of the signals, which will reduce the accuracy of the system.

Using the parameter of impedances in Case2 in Table 3-1, is the delay set to 100 µs. The relative error of the system in frequency domain is shown in Figure 3-20.

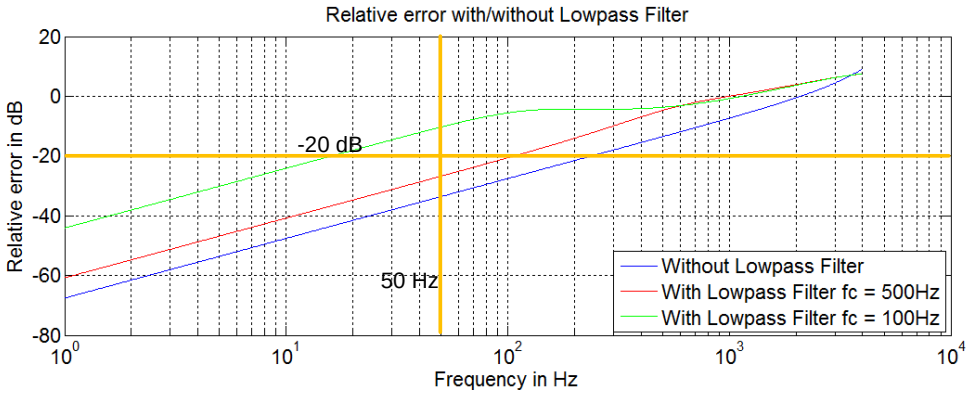



**Figure 3-20; Relative error of the ITM in frequency domain with different $f_c$**

This is shown in Figure 3-20, when there is no low pass filter (blue curve), the relative error of the system is the lowest in all frequencies. The lower the cutoff frequency of the low pass filter, the greater becomes the relative error of the system. When the cutoff frequency is 100Hz (green curve), the relative error at 50 Hz is already -10 dB. Although the gain of low pass filter in the low frequency domain is 0 dB, there is no signal attenuation, but it will still cause the signal phase shift, as shown in the Bode diagram of low pass filter (Figure 3-17). This error is caused by the phase shift of the output waveform. So in order to keep accuracy, the cutoff frequency of low pass filter cannot be selected as too low.

Because the power amplifier has a limitation in operation bandwidth, it can also be regarded as a low pass filter. The stability of the system will be enhanced, and the relative error of the system can be increased due to the phase shift at the same time.

### 3.3.4.2 Advanced Ideal Transformer Method

According to the stability criterion of ITM in chapter 3.3.2, if the impedance of the software side $Z_{Sim}$ is greater than the impedance of the hardware side $Z_{EUT}$, it will make the system unstable. So one can make the $Z_{EUT}$ larger, or make the $Z_{Sim}$ smaller, to meet the stability criterion.

The method of making the $Z_{EUT}$ larger is that, connect an additionally series impedance in the hardware side [32]. This method obviously changes the characteristics of the EUT. This will make the error in real-time simulation.

In this thesis, the Advanced Ideal Transformer Method (AITM) is presented. The basic principle is that, reduce the impedance on the software side by a parallel connected

impedance $Z_C$, at the same time, the output signal of the controlled current source in software side is compensated, in order to keep the output of the software side $U_{Sim}$ equal to normal Ideal Transformer Method.

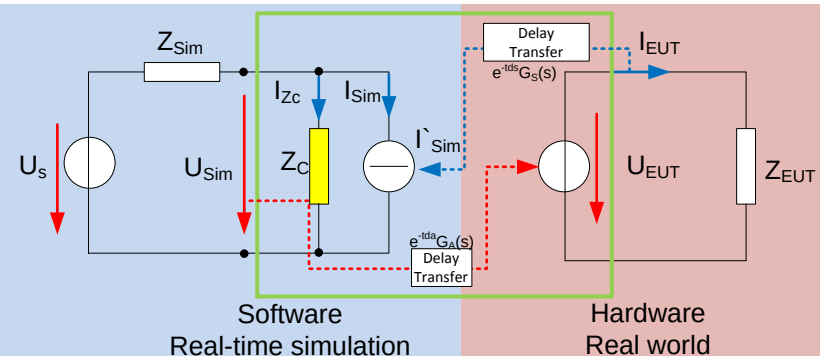



**Figure 3-21; Principle of Advanced Ideal Transformer Method**

Figure 3-21 shows the principle of Advanced Ideal Transformer Method. A compensation impedance $Z_C$ is connected in parallel to controlled current source, in order to reduce the impedance of software side. At the same time, the output signal of the controlled current source is compensated, let the $i_{Sim}$ equal to the difference between $i`_{Sim}$ and $i_{ZC}$ (current on $Z_C$). This ensures that the output of real-time calculation $U_{Sim}$ stays unchanged.

The relationships between the signals are represented in the frequency domain:

$$\begin{cases} U_{EUT}(s) = e^{-st_{dc}} e^{-st_{da}} G_A(s) U_{Sim}(s) \\ I`_{Sim}(s) = e^{-st_{ds}} G_S(s) I_{EUT}(s) \\ I_{Sim}(s) = I`_{Sim}(s) - e^{-st_{dc}} \dfrac{U_{Sim}(s)}{Z_C(s)} \\ U_{Sim}(s) = U_S(s) - Z_{Sim}(s)(I_{Sim}(s) + \dfrac{U_{Sim}(s)}{Z_C(s)}) \end{cases} \qquad \text{Eq. 3-30}$$

The block diagram can be obtained from Eq.3-30, as shown in Figure 3-22.

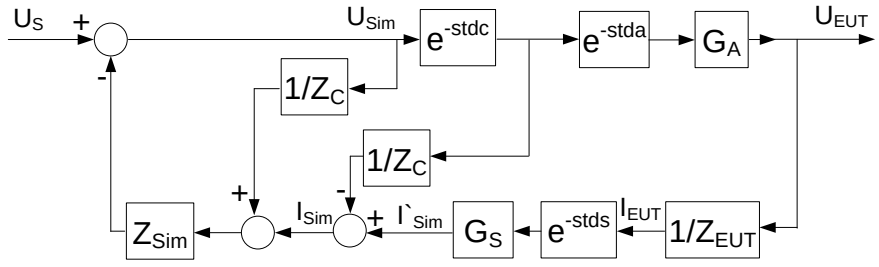



**Figure 3-22; Block diagram of Advanced Ideal Transformer Method**

With the same simplification in Eq.3-14 and Eq.3-15, the closed loop transfer function is presented as：

$$G_{CL-ATIM}(s)=\frac{U_{EUT}(s)}{U_S(s)}=\frac{e^{-st_d}}{1+e^{-st_d}\frac{Z_{Sim}(s)}{Z_{EUT}(s)}-(e^{-st_{dc}}-1)\frac{Z_{Sim}(s)}{Z_C(s)}} \quad \text{Eq. 3-31}$$

Because the total delay $t_d$ is larger than the delay from the real-time calculation $t_{dc}$, set

$$t_d = nt_{dc}(n>1) \quad \text{Eq. 3-32}$$

n… Ratio of the total delay $t_d$ to the delay from real-time calculation $t_{dc}$.

By inserting Eq.3-32 into Eq.3-31 and obtain:

$$G_{CL-ATIM}(s)=\frac{U_{EUT}(s)}{U_S(s)}=\frac{e^{-st_d}}{1+e^{-st_d}\frac{Z_{Sim}(s)}{Z_{EUT}(s)}-(e^{-s\frac{t_d}{n}}-1)\frac{Z_{Sim}(s)}{Z_C(s)}} \quad \text{Eq. 3-33}$$

Take the parameters in Table 3-3 as an example, here all impedance are pure resistance, the stability of system is analyzed with the Nyquist criterion in Figure 3-23.

| | Case 6 | |
|---|---|---|
| **$t_d$** | 100 µs | |
| **$R_C$** | 1 Ω | |
| **n** | 2 | |
| | $Z_{Sim}$ | $Z_{EUT}$ |
| **R** | 2 Ω | 1 Ω |

**Table 3-3; Parameters of Case 6**

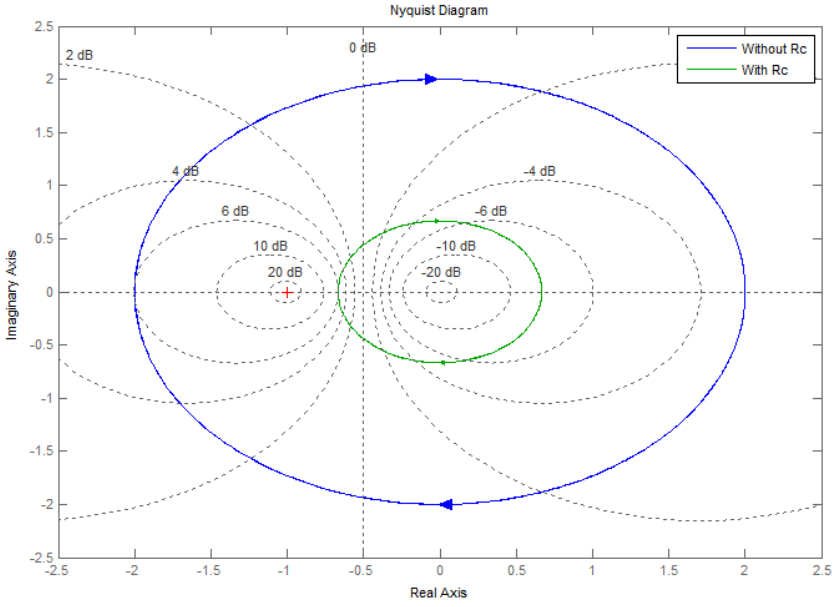



**Figure 3-23; Nyquist curve of Ideal Transformer Method and Advanced Ideal Transformer Method**

This is shown in Figure 3-23, with the same impedance combinations, the Nyquist curve of AITM (green curve) is no more around (-1, j0), so this system is stable.

In order to get the detailed conditions of the stability of the system, the Ruth-Hurwitz rule is used. The compensation impedance should meet the following equation to make the system stable.

$$R_C < \frac{2R_{EUT}R_{Sim}}{R_{Sim} - R_{EUT}} \qquad \text{Eq. 3-34}$$

Using the parameter of impedances in Case 6, the relative error of the system in the frequency domain is shown in Figure 3-24.

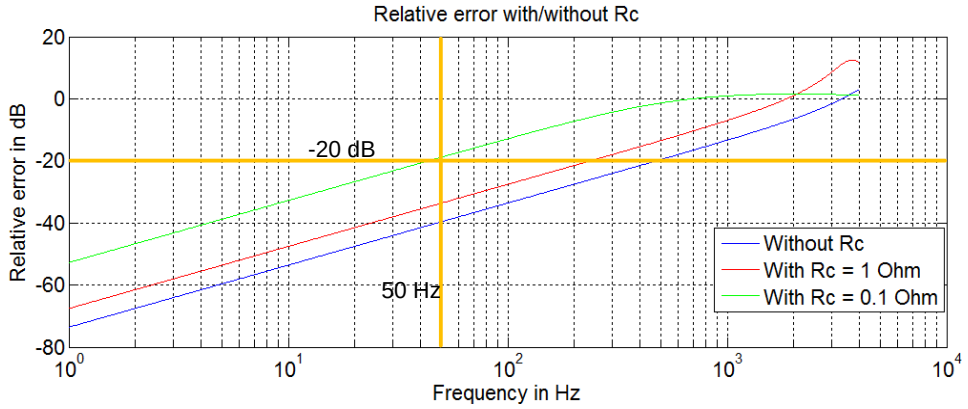



**Figure 3-24; Relative error of the AITM in frequency domain with different $R_C$**

This is shown in Figure 3-24, the relative error of the normal ITM (blue curve) is the lowest in all frequencies. The lower the compensation impedance $R_C$, the relative error of the system is greater. Therefore, the $R_C$ should not only meet to the boundary conditions of stability, but also be considered under the aspect of accuracy. $R_C$ should not be selected as too small.

### 3.3.4.3 Other Compensation Method

In addition to the modification of the PHIL interface algorithm, the grid model in the software side can be also modified to improve stability, such as the reduced scale method and Multi-Rating method [33].

a) Reduced scale method

In order to ensure the $Z_{Sim} < Z_{EUT}$, to meet the boundary conditions of stability, the impedance of all the components in the grid model is scaled-down, the input signals is also scaled-down at the same time. The output signal is scaled-up, to ensure that the output of real-time calculation $U_{Sim}$ keeps unchanged.

b) Multi-Rating method

Split the grid model in two parts, so that $Z_{Sim}=Z_{Sim1}+Z_{Sim2}$, where $Z_{Sim1}$ is simulated with a slower simulation step, and $Z_{Sim2}$ is simulated with a faster simulation step. The principle is shown in Figure 3-25.

This is shown in Figure 3-25, the simulation result from the slower simulation step part will be switched to the faster simulation step part by a virtual PHIL interface (left green box). The simulation result from the faster simulation step part will be transfered to the hardware side by the real PHIL interface (right green box).

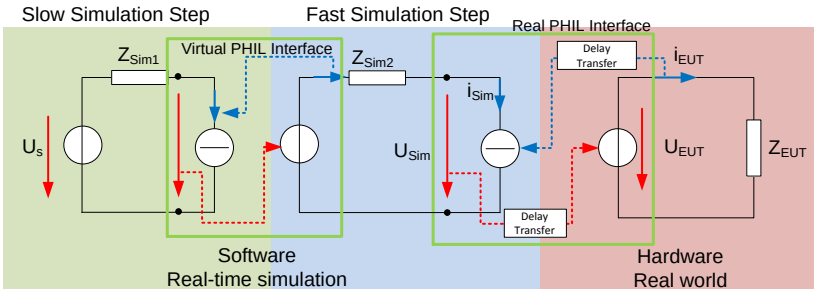



**Figure 3-25; Multi-Rating method**

When $Z_{EUT}>Z_{Sim2}$, this part of system is stable (blue and pink part). The stability in the two subsystems (green and blue part) is determined by the difference between the simulation steps. When the difference of the simulation steps between the two subsystems is large enough, the two subsystems can be dynamically decoupled. So the stability of the system is no more affected by the impedances.

Both of above methods need to modify the grid model, and this is very inconvenient in the practical application.

## 3.4 Damping Impedance Method

Based on the analysis of ITM in chapter 3.3, the delay and distortion of interaction between the software side and the hardware side can reduce the stability and accuracy of the system. In order to completely solve this problem, the modeling and simulation of the hardware side is carried out in the side software. In this way, the delay and distortion caused by the PHIL interface are eliminated.

### 3.4.1 Principle of the Damping Impedance Method

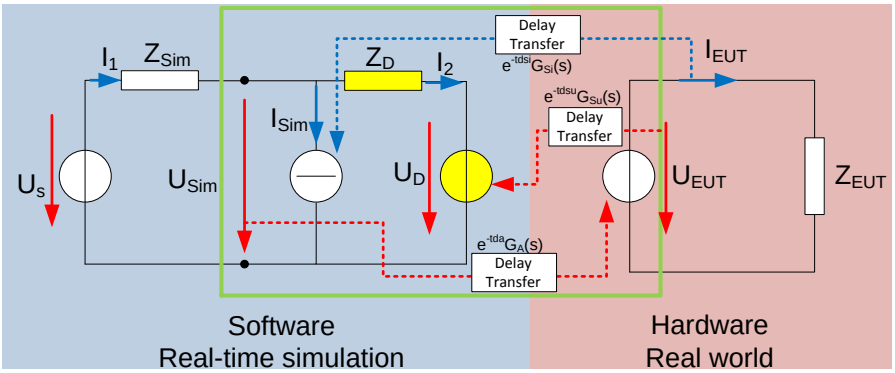



**Figure 3-26; Principle of the Damping Impedance Method**

The basic principle of the Damping Impedance Method (DIM) is that, on the software side, a damping impedance $Z_D$ is used to simulate the impedance of the EUT $Z_{EUT}$, a controlled voltage source $U_D$ is used to simulate the power amplifier $U_{EUT}$.

As in the ITM, the signal transmission in DIM has also delay and distortion. The relationship between the signals is presented in the frequency domain as follows:

$$\begin{cases} U_{EUT}(s) = e^{-st_{dc}} e^{-st_{da}} G_A(s) U_{Sim}(s) \\ i_{Sim}(s) = e^{-st_{dsi}} G_{Si}(s) i_{EUT}(s) \\ U_D(s) = e^{-st_{dsu}} G_{SU}(s) U_{EUT}(s) \end{cases} \quad \text{Eq. 3-35}$$

$t_{da}$… Delay caused by the controller of the power amplifier;

$t_{dsi}$… Delay caused by the current sensors, sampling circuits and the ADC;

$t_{dsu}$… Delay caused by the voltage sensors, sampling circuits and the ADC;

$G_A(s)$ … Transfer function of the power amplifier after deduction of signal delay;

$G_{Si}(s)$ … Transfer function of the current sensors, sampling circuits and the ADC after deduction of signal delay;

$G_{Su}(s)$ … Transfer function of the voltage sensors, sampling circuits and the ADC after deduction of signal delay.

### 3.4.2 Stability Analysis of the Damping Impedance Method

From the Figure 3-26 and Eq.3-35, the block diagram of DIM can be drawn, as shown in Figure 3-27.

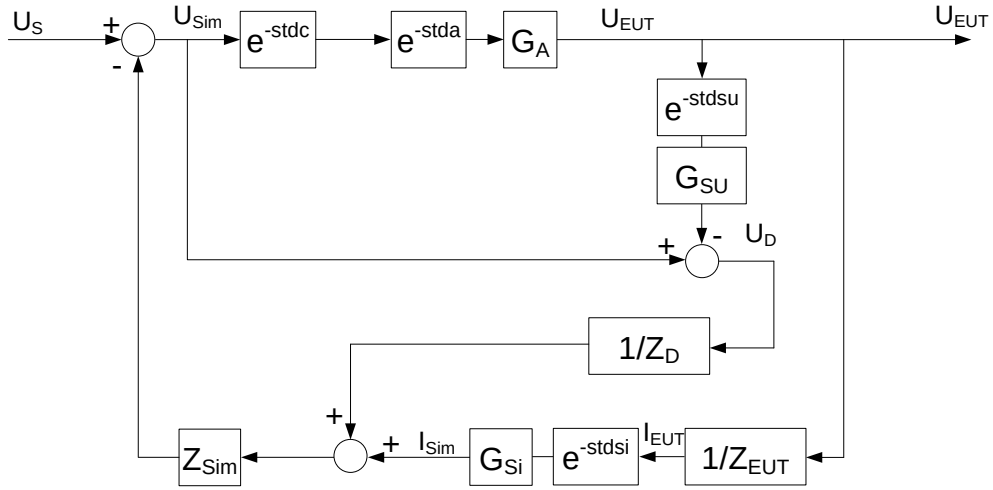



**Figure 3-27; Block diagram of Damping Impedance Method**

The closed loop transfer function of the DIM PHIL test system can be obtained from the Figure 3-27.

$$G_{DIM\_CL}(s)=\frac{U_{EUT}(s)}{U_S(s)}=\frac{e^{-s(t_{da}+t_{dc})}G_A(s)Z_D(s)Z_{EUT}(s)}{Z_{Sim}(s)[e^{-st_{dsu}}G_{Si}(s)Z_D(s)-e^{-st_{dsi}}G_{SU}(s)Z_{EUT}(s)]e^{-s(t_{da}+t_{dc})}G_A(s)+Z_{EUT}(s)[Z_{Sim}(s)+Z_D(s)]}$$

Eq. 3-36

As well as the open loop transfer function:

$$G_{DIM\_OL}(s)=\frac{e^{-st_{dsi}}G_{Si}(s)Z_D(s)-e^{-st_{dsu}}G_{SU}(s)Z_{EUT}(s)}{Z_{Sim}(s)+Z_D(s)}\cdot\frac{Z_{Sim}(s)}{Z_{EUT}(s)}\cdot G_A(s)\cdot e^{-s(t_{da}+t_{dc})}$$ Eq. 3-37

The difference of the delay time and the transfer function between different sensors is very small, so it can be assumed that, the current and voltage sensors have the same delay and transfer function.

$$\begin{cases} t_{ds}=t_{dsi}=t_{dsu} \\ G_S(s)=G_{Si}(s)=G_{SU}(s) \end{cases}$$ Eq. 3-38

By inserting Eq.3-38 into Eq.3-37, the open loop transfer function of DIM becomes:

$$G_{DIM\_OL}(s)=\frac{Z_D(s)-Z_{EUT}(s)}{Z_{Sim}(s)+Z_D(s)}\cdot\frac{Z_{Sim}(s)}{Z_{EUT}(s)}\cdot G_A(s)G_S(s)e^{-s(t_{da}+t_{dc}+t_{ds})}$$ Eq. 3-39

When the damping impedance can perfect simulate the impedance of the EUT in software side, which is:

$$Z_D(s)=Z_{EUT}(s)$$ Eq. 3-40

By inserting the Eq.3-40 into Eq.3-39, and then the open loop transfer function of DIM becomes:

$$G_{DIM\_OL}(s) = \frac{0}{Z_{Sim}(s) + Z_D(s)} \cdot \frac{Z_{Sim}(s)}{Z_{EUT}(s)} \cdot G_A(s) G_S(s) e^{-s(t_{da}+t_{dc}+t_{ds})} = 0 \qquad \text{Eq. 3-41}$$

When the open loop transfer function is equal to zero, according to the Nyquist stability criterion, the Nyquist curve will be not circle around (-1, j0) at any delays and any impedances, so this system is always stable, as shown in Figure 3-28.

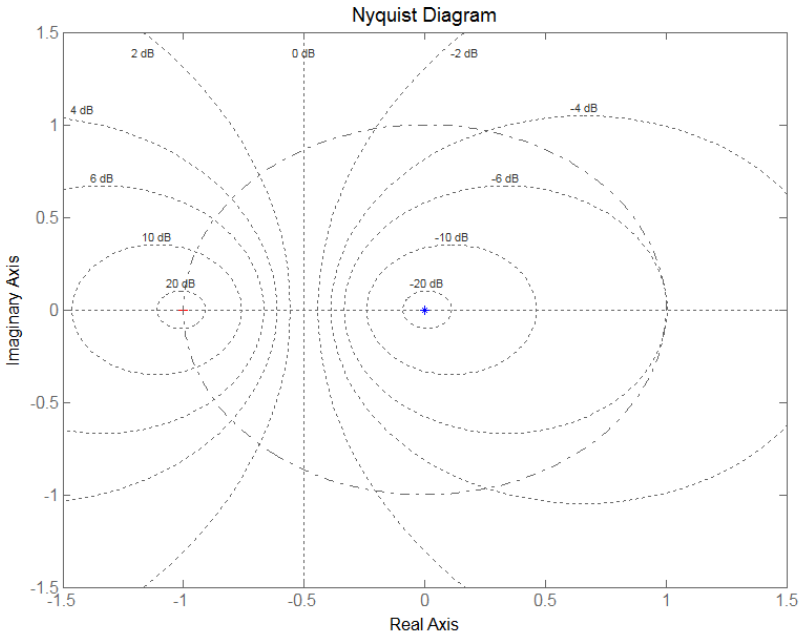



**Figure 3-28; Nyquist curve of Damping Impedance Method in ideal condition**

When $Z_D$ is not exactly equal to $Z_{EUT}$, the stability performance of the system will be affected, but due to the characteristics of the DIM, but the stability performance of the DIM is still higher than ITM.

With the same simplification in Eq.3-14 and Eq.3-15, the open loop transfer function is presented as:

$$G_{DIM\_OL}(s) = \frac{Z_D(s) - Z_{EUT}(s)}{Z_{Sim}(s) + Z_D(s)} \cdot \frac{Z_{Sim}(s)}{Z_{EUT}(s)} \cdot e^{-st_d} \qquad \text{Eq. 3-42}$$

Use the parameter of impedances in Case 6 and ratio of $Z_D/Z_{Sim}$ is set to 0.1, 3 and 5 respectively in order to show gross mismatching.

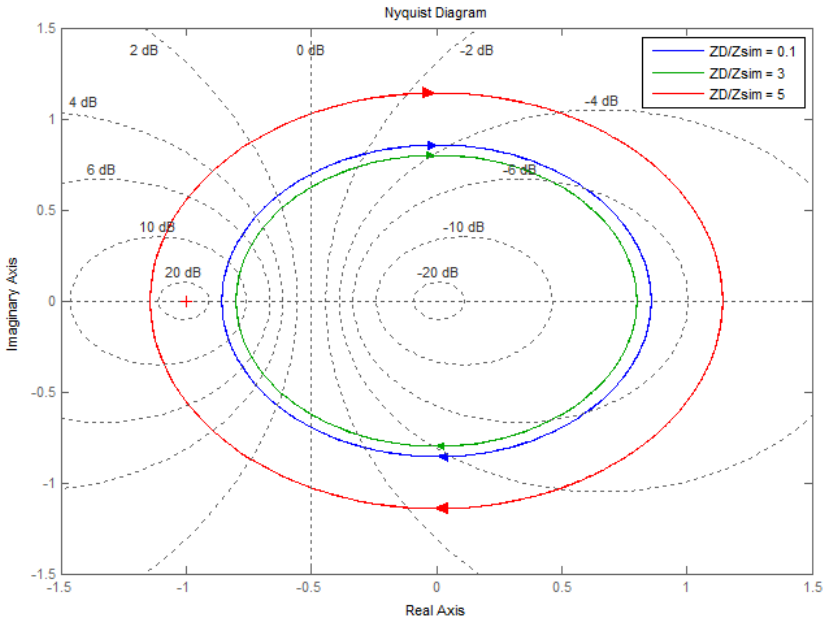



**Figure 3-29; Nyquist curve of Damping Impedance Method in different $Z_D/Z_{Sim}$**

This is shown in Figure 3-29, when the ratio of $Z_D/Z_{Sim}$ is equal to 0.1, the Nyquist curve of the Damping Impedance Method in non-ideal condition (blue curve) does not include (-1, j0), so this system is still stable.

Even in extreme cases, which $Z_D$ is equal to zero:

$$G_{DIM\_OL}(s) = \frac{-Z_{EUT}(s)}{Z_{Sim}(s)} \cdot \frac{Z_{Sim}(s)}{Z_{EUT}(s)} \cdot e^{-st_d} = -e^{-st_d} \qquad \text{Eq. 3-43}$$

This system is still in the steady-state. Therefore, when $Z_D$ is smaller than $Z_{EUT}$, the system is stable. But when $Z_D$ is larger than $Z_{EUT}$, the system may become unstable, for example, when $Z_D/Z_{Sim}$ is equal to 3, the Nyquist curve (red curve) circle around (-1, j0), and the system is unstable.

In order to get the detailed conditions of the stability of the system, the Ruth-Hurwitz rule is used again.

From Eq.3-37 the characteristic equation of the closed loop transfer function can be obtainedd:

$$Z_{Sim}(s)[Z_D(s) - Z_{EUT}(s)]e^{-st_d}G_A(s)G_s(s) + Z_{EUT}(s)[Z_{Sim}(s) + Z_D(s)] = 0 \qquad \text{Eq. 3-44}$$

By inserting Eq.3-38 into Eq.3-44, the characteristic equation of DIM is simplified to:

$$Z_{Sim}(s)[Z_D(s) - Z_{EUT}(s)]e^{-st_d} + Z_{EUT}(s)[Z_{Sim}(s) + Z_D(s)] = 0 \qquad \text{Eq. 3-45}$$

In order to facilitate the analysis, these impedances are regarded as pure resistances:

$$\begin{cases} Z_{Sim}(s) = kR_{EUT} \\ Z_{EUT}(s) = R_{EUT} \\ Z_D(s) = n_D R_{EUT} \end{cases}$$ Eq. 3-46

k… Ratio of the absolute value of $Z_{Sim}$ and $Z_{EUT}$

$n_D$… Ratio of the absolute value of $Z_D$ and $Z_{EUT}$

By inserting Eq.3-46 into Eq.3-45:

$$t_d(n_D k - 2n_D - k)s - 2k(n_D + 1) = 0$$ Eq. 3-47

The system should meet the following equation to make the system stable.

$$n_D < \frac{2k}{k-1}$$ Eq. 3-48

From Eq.3-48, when the $Z_{Sim}$>$Z_{EUT}$ (k>1), as long as the $Z_D$ is less than $Z_{EUT}$ ($n_D$<1), the system is stable. When $n_D$>1, the stability boundary of the system must be met as shown in Figure 3-30 with the parameter in Case 6. All values below the curve are stable.

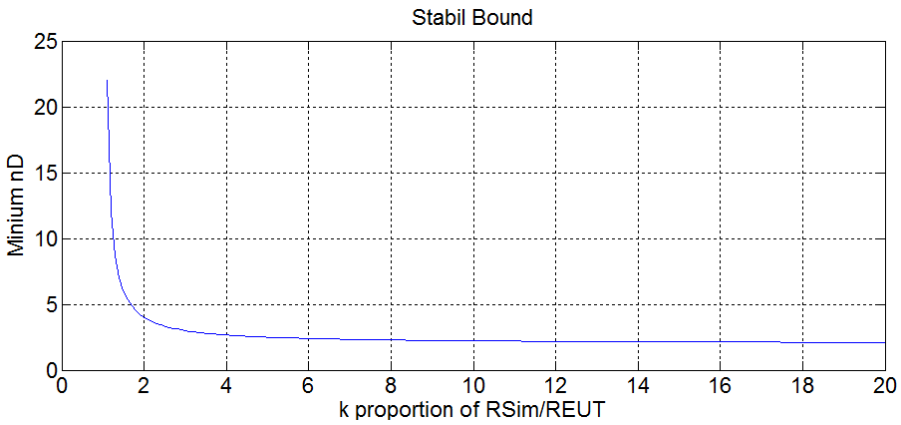



**Figure 3-30; Stability boundary of Damping Impedance Method**

### 3.4.3 Accuracy Analysis of the Damping Impedance Method

With the same simplification in Eq.3-14 and Eq.3-38, also ignoring the delay from sensors ($t_{dsi}$=$t_{dsu}$=0), the closed loop transfer function is presented as：

$$G_{DIM\_CL}(s) = \frac{U_{EUT}(s)}{U_S(s)} = \frac{e^{-st_d} Z_D(s) Z_{EUT}(s)}{Z_{Sim}(s)[Z_D(s) - Z_{EUT}(s)]e^{-st_d} + Z_{EUT}(s)[Z_{Sim}(s) + Z_D(s)]}$$ Eq. 3-49

And meet the ideal condition of $Z_D$, which is $Z_D$ equal to $Z_{EUT}$ (Eq.3-40).

By inserting Eq.3-40 into Eq.3-49 to get the simplified closed loop transfer function:

$$G_{DIM\_CL}(s) = \frac{U_{EUT}(s)}{U_S(s)} = \frac{e^{-st_d} {Z_{EUT}}^2(s)}{Z_{EUT}(s)[Z_{Sim}(s) + Z_{EUT}(s)]}$$ Eq. 3-50

The closed loop transfer function of the ideal DIM, which without delay is:

$$G_{DIM\_Ideal}(s) = \frac{Z_{EUT}{}^{2}(s)}{Z_{EUT}(s)[Z_{Sim}(s) + Z_{EUT}(s)]} \qquad \text{Eq. 3-51}$$

The relative error of the system in frequency domain is as follows:

$$Error_{DIM}(s) = 20\log\left(\left|\frac{G_{DIM\_CL}(s) - G_{DIM\_Ideal}(s)}{G_{DIM\_Ideal}(s)}\right|\right) \qquad \text{Eq. 3-52}$$

When using the parameter of impedances in Case 2 in Table 3-1, and setting the total system delays $t_d$ to 10 µs, 50 µs and 100 µs respectively, the simulation steps $t_{dc}$ to 5 µs, 25 µs and 50 µs respectively, the relative error of the system in frequency domain is shown in Figure 3-31.

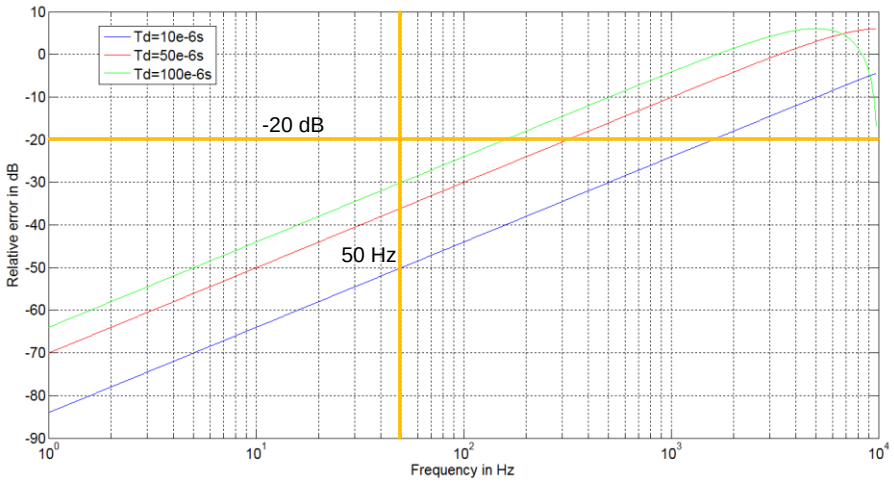



**Figure 3-31; Relative error of the Damping Impedance Method in frequency domain**

This is shown in Figure 3-31, the relative error increases with the frequency of the same delay just like the situation in the ITM (Figure 3-13).

The different combinations of impedances from software and hardware side can affect the relative error of ITM (Figure 3-14), in order to analyze the influence of different combinations of impedances on DIM, the parameters in Table 3-4 are taken as an example.

| | Case 7 | | Case 8 | | Case 9 | | Case 10 | |
|---|---|---|---|---|---|---|---|---|
| $t_d$ | 10 µs | | 10 µs | | 10 µs | | 10 µs | |
| | $Z_{Sim}$ | $Z_{EUT}$ | $Z_{Sim}$ | $Z_{EUT}$ | $Z_{Sim}$ | $Z_{EUT}$ | $Z_{Sim}$ | $Z_{EUT}$ |
| **R** | 1 Ω | 2 Ω | 1 Ω | 10 Ω | 2 Ω | 1 Ω | 10 Ω | 1 Ω |
| **L** | 1 mH | 2 mH | 1 mH | 10 mH | 2 mH | 1 mH | 10 mH | 1 mH |

**Table 3-4; Parameters of Case 7, Case 8, Case 9 and Case 10**

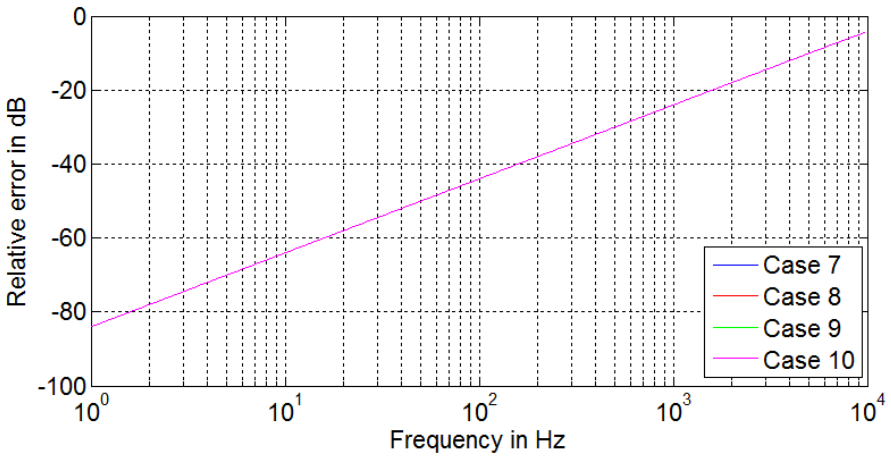



**Figure 3-32; Relative error of the DIM in frequency domain with different combinations of impedances**

This is shown in Figure 3-32, there is no difference in the relative error in all frequencies, so in the Damping Impedance Method, the relative system error is independent of the different combinations of impedances from software and hardware side.

In order to compare several PHIL interface methods and compensation methods, the relative errors of those interface methods in frequency domain are shown in Figure 3-33, which the parameters of Case 2 in Table 3-1 and total system delay $t_d$ is 100 µs.

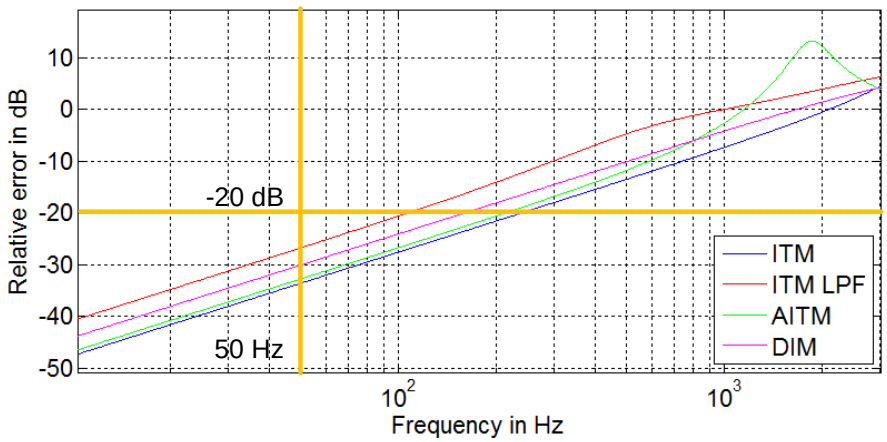



**Figure 3-33; Relative error in frequency domain of different interface methods**

It can be seen in Figure 3-33, the Ideal Transformation Method has the highest accuracy for frequencies under 1000Hz, followed by the Damping Impedance Method, then the Advanced Ideal Transformation Method and Ideal Transformation Method with low pass filter. Since the stability performance of the Ideal Transformation Method is not good enough, considering the requirement of accuracy and stability, the Damping Impedance Method is used as the PHIL interface algorithm in this thesis.

### 3.4.4 Online Impedance Parameter Identification

According to the analyses in chapter 3.4.2, the stability performance of the system is optimal when the damping impedance $Z_D$ exactly equal to the impedance of EUT $Z_{EUT}$.

The EUTs in this thesis are DG systems, which are composed of nonlinear components. Its output characteristic is related by the controller, so its impedance $Z_{EUT}$ is a nonlinear piecewise function due to the control strategy of the DG system. The EUT is a black box for the PHIL test system. Therefore, its impedance cannot be predicted before the PHIL testing. In order to get the exact impedance parameter of the EUT during the PHIL test with Damping Impedance Method, an Online Impedance Parameter Identification (OIPI) is presented in this thesis (Figure 3-34).

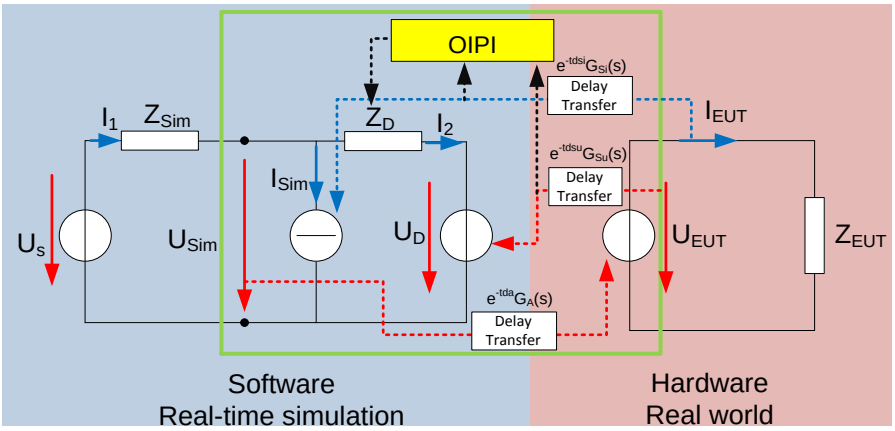



**Figure 3-34; Principle of the online impedance parameter identification**

Due to the output EMC filter in the DG systems (EUT), the impedance of the EUT is generally resistive and inductive.

$$Z_{EUT}(t) = R_{EUT}(t) + j\omega L_{EUT}(t) \qquad \text{Eq. 3-53}$$

The relationship of the voltage and current is given by:

$$\frac{U_{EUT}(t)}{i_{EUT}(t)} = Z_{EUT}(t) \qquad \text{Eq. 3-54}$$

The voltage and current can be represented as complex-valued functions:

$$\begin{cases} U_{EUT}(t) = U_{RMS-EUT}(t)\cos(\omega t + \varphi_u(t)) = U_{RMS-EUT}(t)e^{j(\omega t+\varphi_u(t))} \\ I_{EUT}(t) = I_{RMS-EUT}(t)\cos(\omega t + \varphi_i(t)) = I_{RMS-EUT}(t)e^{j(\omega t+\varphi_i(t))} \end{cases} \qquad \text{Eq. 3-55}$$

Then the left side of Eq.3-54 can be obtained with Eq.3-55:

$$\frac{U_{EUT}(t)}{i_{EUT}(t)} = \frac{U_{RMS-EUT}(t)}{I_{RMS-EUT}(t)} e^{j(\varphi_u(t)-\varphi_i(t))} \qquad \text{Eq. 3-56}$$

Transfer of Eq.3-56 by Euler's formula:

$$\frac{U_{EUT}(t)}{i_{EUT}(t)} = \frac{U_{RMS-EUT}(t)}{I_{RMS-EUT}(t)}(\cos(\varphi_u(t)-\varphi_i(t)) + j\sin(\varphi_u(t)-\varphi_i(t))) \quad \text{Eq. 3-57}$$

By inserting the Eq.3-57 and Eq.3-53 into Eq.3-54:

$$\frac{U_{RMS-EUT}(t)}{I_{RMS-EUT}(t)}(\cos(\varphi_u(t)-\varphi_i(t)) + j\sin(\varphi_u(t)-\varphi_i(t))) = R_{EUT}(t) + j\omega L_{EUT}(t) \quad \text{Eq. 3-58}$$

Equating real and imaginary parts of Eq.3-58, the impedance parameters of the EUT can be obtained:

$$\begin{cases} R_{EUT}(t) = \dfrac{U_{RMS-EUT}(t)}{i_{RMS-EUT}(t)}\cos(\varphi_u(t)-\varphi_i(t)) \\ L_{EUT}(t) = \dfrac{U_{RMS-EUT}(t)}{i_{RMS-EUT}(t)}\dfrac{\sin(\varphi_u(t)-\varphi_i(t))}{\omega} \end{cases} \quad \text{Eq. 3-59}$$

By measuring and calculating the voltage and current of the EUT, the impedance parameters of the EUT can be online identified. The calculation process is shown in Figure 3-35:

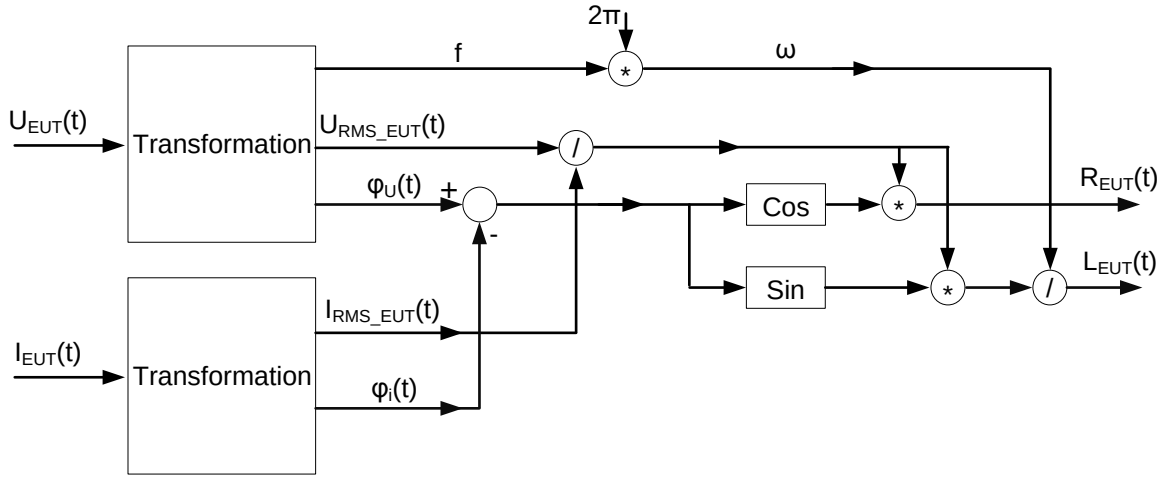



**Figure 3-35; Calculation process of the online impedance parameter identification**

## 3.5 The System Delay Compensation

The response time of a Mega-Watt class power amplifier is usually in the millisecond class, so in the Mega-Watt class PHIL test system, the system delay due to the power amplifier will still reduce the accuracy and stability of the system, even if the Damping Impedance Method is used. Therefore, the compensation of system delay is necessary (Figure 3-36).

The system delay is equivalent to the phase shift in frequency domain. The Pulse Width Modulation (PWM) method is common applied in the Mega-Watt class power amplifier, in order to improve the quality of the output waveform, the high order harmonics of the

switching frequency must be eliminated by a the low pass filter. But the low pass filter causes phase shift, which is also regarded as a system delay.

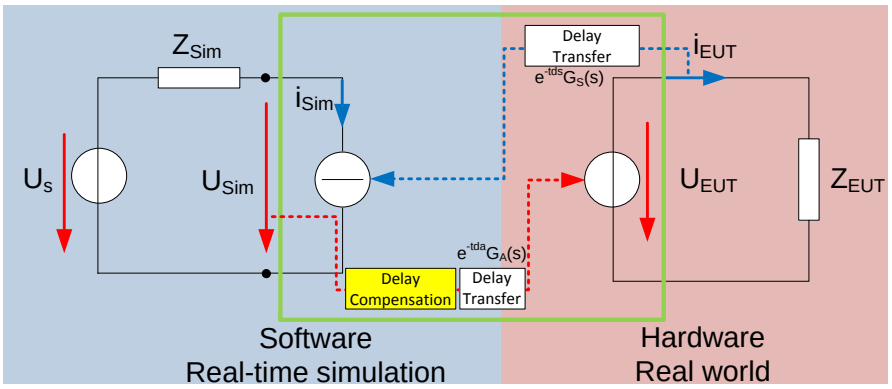



**Figure 3-36; Principle of compensation of system delay in ITM**

The principle of the delay compensation is: the result of real-time simulation $U_{Sim}$ will be transformed to the amplitude, phase and frequency. The system delay, which is equivalent to the phase shift, will be compensated by an opposite phase shift. Then this signal will be reconstructed, as shown in Figure 3-37.

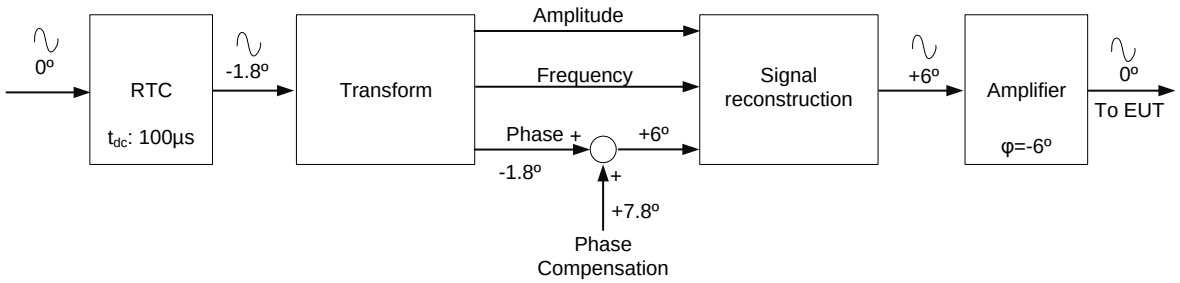



**Figure 3-37; Process of the compensation of system delay**

The opposite phase shift can be a pre-computed phase, which depends on the fixed delay from real-time calculation step and the fixed phase shift from the filter of power amplifier. At a certain frequency, the phase shift caused by power amplifier will be a constant as long as the parameters of the filter are not changed.

In order to get the amplitude, phase and frequency of the original signal, the original signal needs to be transformed. Since this transform serves for the phase compensation, the result of transform must be the instantaneous value of the original signal in real-time. Otherwise, the reconstruction signal will be delayed.

### 3.5.1 Signal Transform based on the Time and Frequency Domain Principle

The common signal transforms based on time and frequency domain are fast Fourier transform [34] and Hilbert-Huang transform [35]. These signal transforms based on time and frequency domain are only suitable for stationary signals. The instantaneous value of the

non-stationary signal cannot be obtained in real-time. For example, the voltage signal from voltage dip is a non-stationary signal. Therefore, the transform, phase compensation and reconstruction with fast Fourier transform (Figure 3-38) or Hilbert-Huang transform (Figure 3-39) will cause the delay and signal distortion.

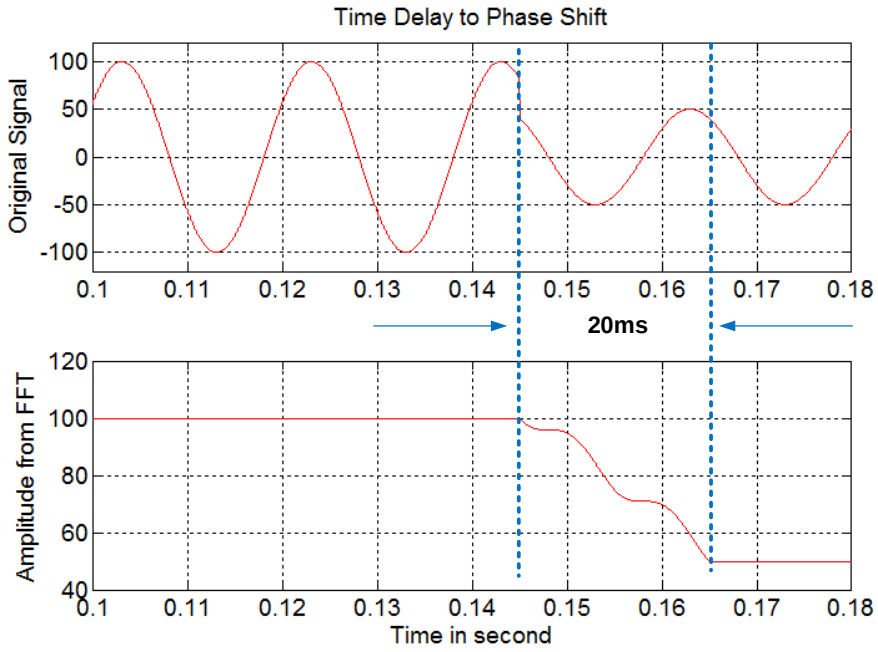



**Figure 3-38; Fast Fourier transform of the voltage dip signal (up: original signal; down: transformed amplitude)**

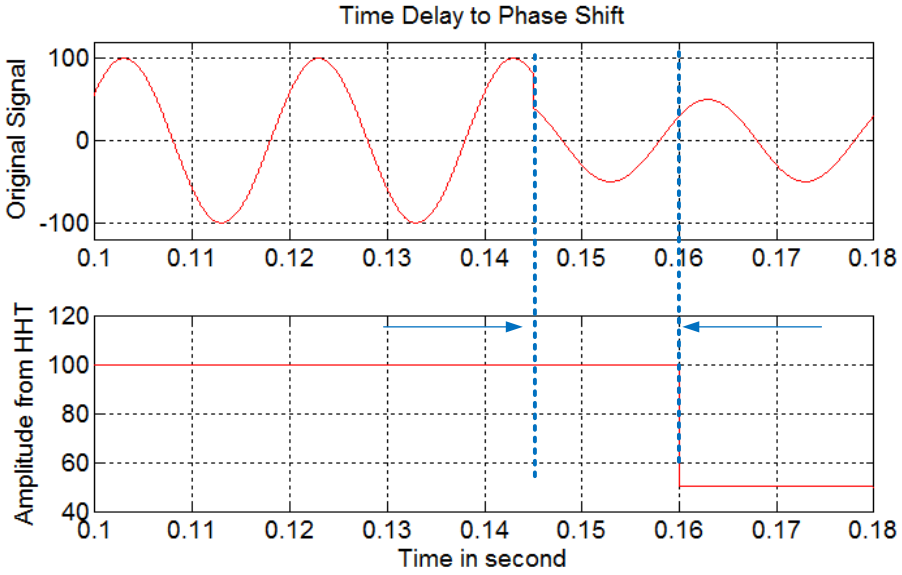



**Figure 3-39; Hilbert-Huang transform of the voltage dip signal (up: original signal; down: transformed amplitude)**

This is shown in Figure 3-38 and Figure 3-39, the signal transform based on time and frequency domain cannot transform the original signal in to instantaneous amplitude values in real-time. The upper figures are the original signal, which a voltage dip occurs at 0.145s. But the transform results of amplitude (the down figures) cannot represent the instantaneous value of the original signal in real-time.

### 3.5.2 Signal Transform based on the Coordinate Transformation Principle

According to the discussion of chapter 3.5.1, the phase compensation based on time and frequency domain cannot be used in non-stationary signals. Therefore, a phase compensation method based on coordinate transformation is presented.

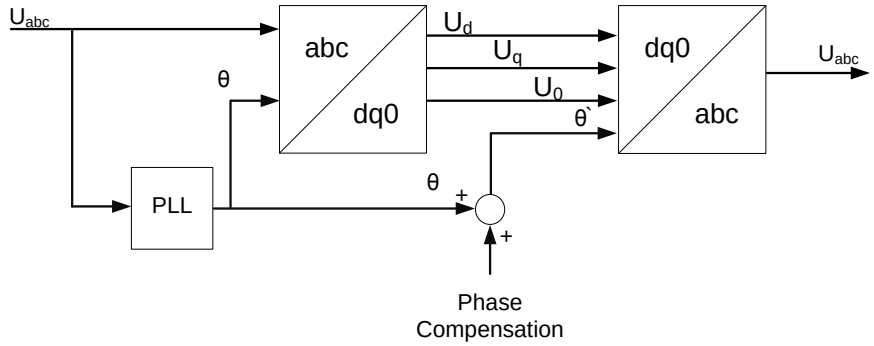



**Figure 3-40; Calculation process of the phase compensation method based on coordinate transformation**

This is shown in Figure 3-40, the three-phase AC voltage ($V_{abc}$) will be transformed into three DC quantities ($U_d$, $U_q$, $U_0$) by the Park's transformation.

$$\begin{vmatrix} u_d(t) \\ u_q(t) \\ u_0(t) \end{vmatrix} = \mathbf{C}_{\mathbf{abc\text{-}dq0}} \begin{vmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{vmatrix} \qquad \text{Eq. 3-60}$$

The transformation matrix $\mathbf{C}_{\mathbf{abc\text{-}dq0}}$ is given by:

$$\mathbf{C}_{\mathbf{abc\text{-}dq0}} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ -\cos(\omega t) & -\cos(\omega t - \frac{2\pi}{3}) & -\cos(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \qquad \text{Eq. 3-61}$$

The phase angle (θ) of three-phase AC voltage is obtained by Phase Locked Loop (PLL) and will be compensated by an opposite phase shift. Then this signal will be reconstructed by the inverse Park's transformation.

$$\begin{bmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{bmatrix} = \mathbf{C}_{\mathbf{dq0\text{-}abc}} \begin{bmatrix} u_d(t) \\ u_q(t) \\ u_0(t) \end{bmatrix} \qquad \text{Eq. 3-62}$$

The inverse transformation matrix $\mathbf{C}_{\mathbf{dq0\text{-}abc}}$ is given by:

$$\mathbf{C}_{\mathbf{dq0\text{-}abc}} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) & 1 \\ \sin(\omega t - \frac{2\pi}{3}) & -\cos(\omega t - \frac{2\pi}{3}) & 1 \\ \sin(\omega t + \frac{2\pi}{3}) & -\cos(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \quad \text{Eq. 3-63}$$

The transform of a signal is based on the method of coordinate transformation, so it is not related to the time and frequency domain, therefore, the transform result is in real-time. An example is shown in Figure 3-41.

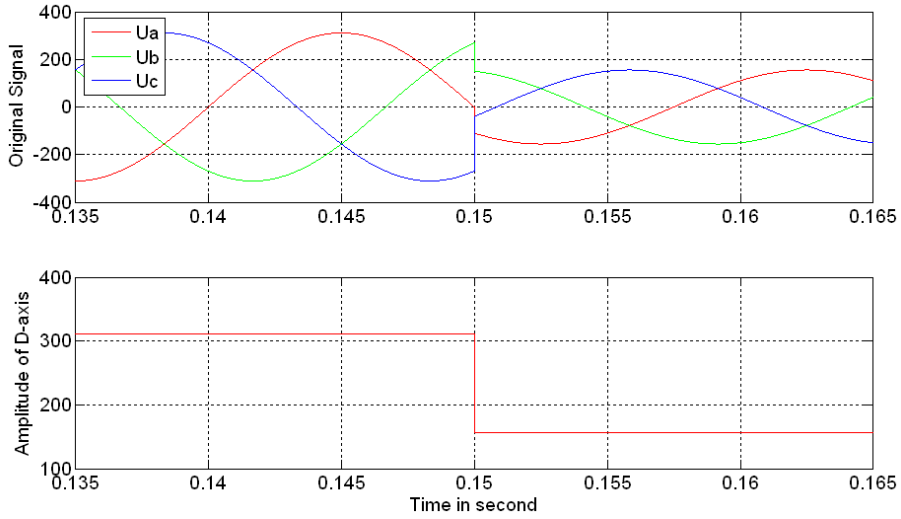



**Figure 3-41; Coordinate transformation of the voltage dip signal (up: original signal; down: transformed amplitude)**

In upper part of Figure 3-41 shows symmetrical voltage dip occurs at 0.15s, and the peak voltage from 311V to 156V and the phase shift is 45 deg. The transform result of amplitude goes the correct value without delay.

Due to the limitation of the delay compensation based on the coordinate transformation, it is suitable for the symmetrical three-phase voltage. Therefore, it can be only used in limited situation, such as the system delay is seriously affected the accuracy.

## 3.6 System Requirements for a Power Hardware-in-the-Loop Test System

In order to let a PHIL test system operates stably and accuracy during the testing on EUT, some requirements needs to be met. The requirement analysis will be carried out in update frequency of the PHIL test system and the power amplifier respectively.

### 3.6.1 Update Frequency of a Power Hardware-in-the-Loop Test System

In order to let the testing waveform of a PHIL test system completely reconstructed in the EUT, the update frequency of the PHIL test system $f_{PHIL}$ and the update frequency of EUT $f_{EUT}$ have to be met the Nyquist sampling criterion:

$$f_{PHIL} \geq 2f_{EUT} \qquad \text{Eq. 3-64}$$

The update frequency of the EUT is its switching frequency. The switching frequency of a Mega-Watt class EUT is usually lower than 5k Hz. Therefore, the lower limit of the update frequency of a PHIL test system $f_{PHIL}$ is 10k Hz. It is also the total delay time of a PHIL test system, here is 100 µs.

According to the design in chapter 3.2.3, the control software of power amplifier and the grid model run in the same real-time simulator, so the running time of control software plus grid model must be smaller than 100 µs.

### 3.6.2 Power Amplifier Requirements

The power amplifier is the actuator of a PHIL test system. Its performance directly affects the performance of the PHIL test system. The cutoff frequency of the output filter of a common DG system is lower than 700 Hz. So the influence from grid side to the DG system, which the frequency is higher than 2000 Hz, is very small. Therefore, the upper limit of the output voltage frequency of the power amplifier of a PHIL test system is 2000 Hz. Other requirements can be seen in the chapter 5.2.

## 3.7 Summary of this Chapter

In this chapter, the overall analysis of the Power Hardware-in-the-Loop test system is carried out. The stability criterion for the operation sequence of a PHIL test system is given: the running time of measuring, sampling and the real-time operation must be greater than or equal to the running time of the power amplifier. On the basis of this, the operation sequence of PHIL test system has been optimized: the real-time simulator is responsible for both the calculation of the grid model and the control software of the power amplifier.

This chapter also goes a detailed study on the PHIL interface algorithm. The accuracy and stability of the two algorithms (Ideal Transformer Method and Damping Impedance Method) are studied systematically. The stability boundaries of various algorithms are given. On the basis of this, several compensation algorithms are presented. Simulation experiments are carried out. According to the simulation results, this thesis chooses the Damping Impedance Method as the PHIL interface algorithm.

Then, in the case of large system delay, the present delay compensation algorithm is analyzed. A delay compensation algorithm based on the principle of coordinate transformation is presented to enhance the accuracy of the system.

Finally, this chapter gives requirements of performance and parameters for a PHIL test system and a power amplifier. This provides performance reference for the following chapters.

# 4 Testing grid environment

The core value of the Power Hardware-in-the-Loop test method is embodied in its testing environment, so the PHIL test system can test the EUT as in a real operation environment. There are two types of the testing environment for the DG systems in PHIL testing: the testing environment of energy sources side and the testing environment of the grid side, as shown in Figure 4-1.

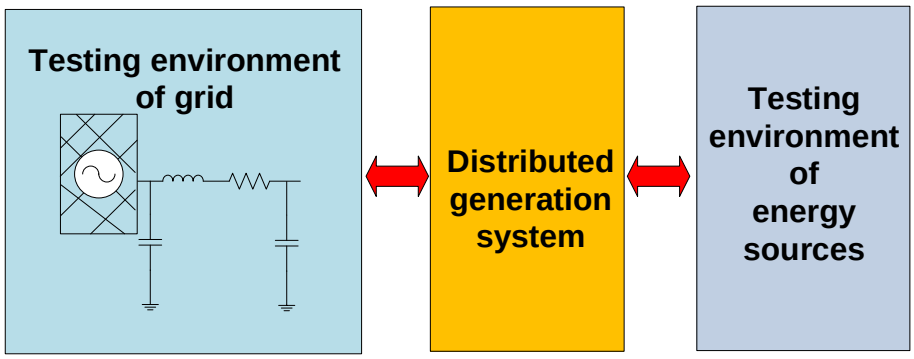



**Figure 4-1; Testing environment of the DG systems**

The testing environment on the energy sources side is different according to the type of DG systems. For the wind turbines, it is the input torque of the generator, which is produced by motor/generator test bench [10]. For a photovoltaic converter, it is the DC input voltage and current, which is generated by PV array simulator [36].

The testing environment on the grid side is the AC grid. The EUT in this thesis are large DG systems. They are usually installed in power plants together with other DG systems. Through the analysis of the chapter 2.2, the grid environment greatly affects the operation of the DG systems. So this chapter carries out the detailed analysis and modeling of the grid environment which contains a large number of DG systems.

Due to the limited computing power of the real-time simulator, the computational complexity of the grid model is limited. When the requirement of accuracy of simulation is taking into account, it is needed to establish a detailed grid model, which with high computational complexity.

In this chapter, the several typical topologies of grid with large DG systems will be analyzed and summarized (chapter 4.1). In order to reduce the computational complexity and ensure the accuracy of the simulation, the universal simplified modeling method of the large DG systems will be presented (chapter 4.2). The equivalent simplified model of the grid with large DG systems will be established based on the above research (chapter 4.3).

## 4.1 Typical Topology of a Grid with Large Distributed Generation Systems

Most of the power plants of large DG systems are established in the remote areas. There is long distance from the power plants to the electricity loads [37]. Therefore, relative to the influence from local electricity loads on DG system, DG systems experience more influence from the grid topology and the neighboring DG systems. The grid model with large DG systems can be divided in two parts: the regional AC grid model and the power plant model.

The regional AC grid model is responsible for the connection of each power plant to the external power grid. The main components of the regional AC grid model are consisting of external power grid, power transmission lines, transformers and power plants, etc.. The power plant model is responsible for connecting the each DG system to regional power grid. The main components of the power plant model are DG system, transmission line, transformer, DC transmission system, static var compensation devices, etc..

### 4.1.1 Topology of a Regional AC Grid

Areas, where the wind and solar resources is quite affluent, are generally far away from residential areas, such as in the desert, mountains and even in the sea [38]. Considering the annual energy production and land price, large wind farms and solar farms are usually established in these areas. These areas are lack large-scale electricity loads, and are located at the outfringes of the power system. Therefore, the connection from these areas to the external power grid has to be carried out through long transmission lines. The topology of the typical regional AC grid with a single power plant is shown in Figure 4-2.

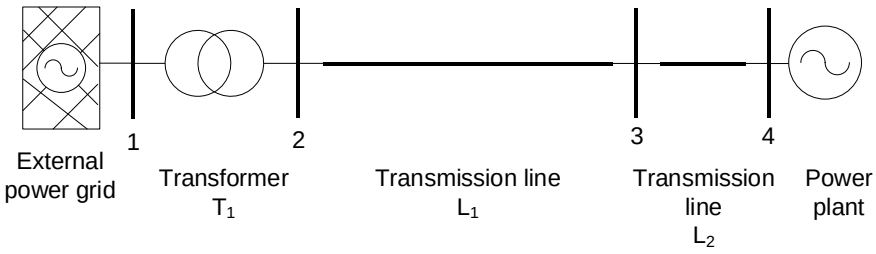



**Figure 4-2; Topology of the typical regional AC grid with a single power plant**

In Figure 4-2, the transmission line $L_2$, the power plant (node 4) is connected to the local collector station (node 3), and then the long transmission line $L_1$, is connected to the collector station for external power grid (node 2). The step-up transformer $T_1$ is connected to the external power grid. The length of long transmission line $L_1$ is usually longer than 30 km and the length of the transmission line $L_2$ is usually less than 10 km [39].

Because the short circuit capacity of external power grid is far greater than the capacity of the power plant, there is only slightly retroactive effect between the external power grid and power plant. In order to reduce the computational complexity, the external network can be equivalent to a constant voltage source.

At the areas, where the wind and solar resources is quite affluent, there are usually several wind or solar power plants. The regional AC grid with multiple power plants as shown in Figure 4-3.

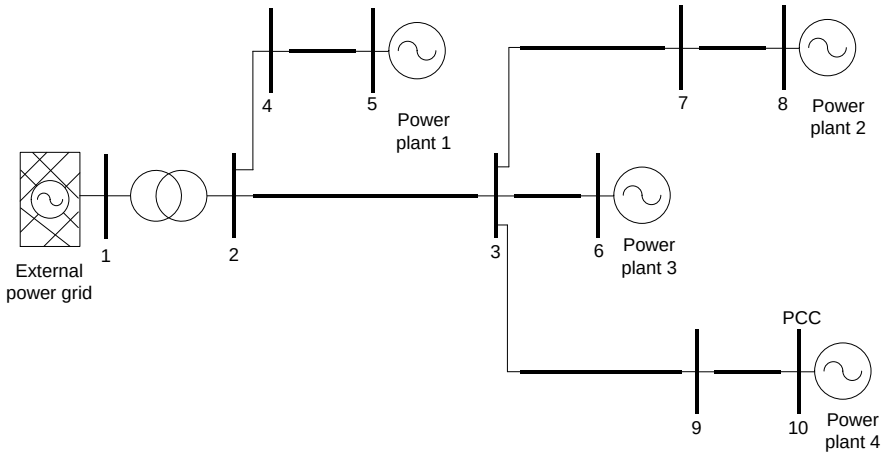



**Figure 4-3; Topology of the typical regional AC grid with multiple power plants**

In Figure 4-3, there are four power plants in the regional AC grid. The distance between each power plant to the collector station for external power grid (node 2) is different, the other characteristics and parameters are similar to the regional AC grid with single power plant.

### 4.1.2 Topology of the Power Plant with Large Distributed Generation Systems

The topology and the power transmission method of wind farm (see Figure 4-4) is representative, it covers most of power plant with large DG systems, such as large PV power stations.

The main electrical connection, the collection system in wind farm and the used HVDC transmission system (see Figure 4-7) will be analyzed and summarized in following chapter.

#### 4.1.2.1 Main Electrical Connection

The main electrical connection of an onshore wind farm is simple. This is shown in Figure 4-4, the voltage level of the collection system is generally 35 kV to reduce the loss. According to the rated power of the wind farm, the connections from the collection bus to the Point of Common Coupling (PCC) are generally made by one or two step-up transformers. The step-up transformer is usually a conventional double winding transformer (YNyn10d). In order to clear any electrical the fault in the wind farm rapidly to avoid tripping of wind turbines, usually the small resistance grounding system is adopted [40] [41] [42] [43] [44] [45]. The static var compensation device can be connected at the medium-voltage (35 kV) collection bus or the high-voltage (110 kV or 220 kV) bus.

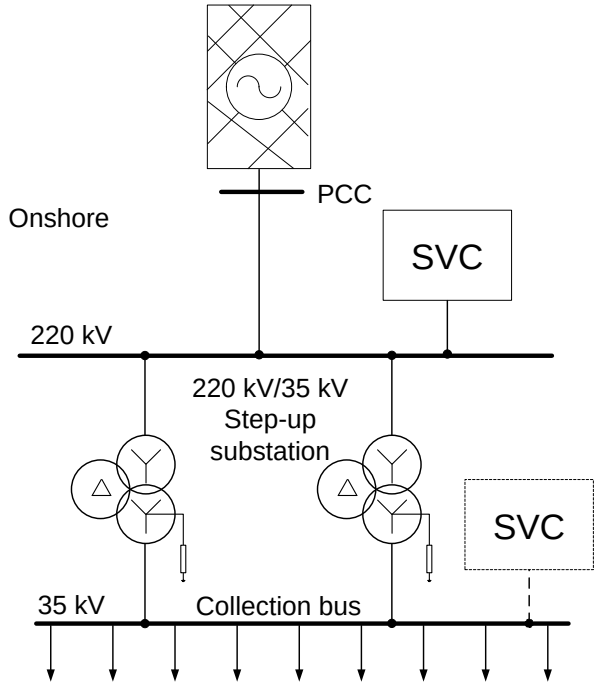



**Figure 4-4; Main electrical connection of an onshore wind farm**

The voltage level of the collection system in an offshore wind farm (see Figure 4-5) is generally 35 kV. The connection between the collection bus and the PCC has to been carried out though the long distance submarine cables. In order to reduce the losses, an offshore step-up substation will be set up. The connection between the collection bus and the PCC will be realized thought one step-up substation and submarine cables (Figure 4-5, left), or by one step-up substation, submarine cables and the second stage of step-up substation (Figure 4-5, right).

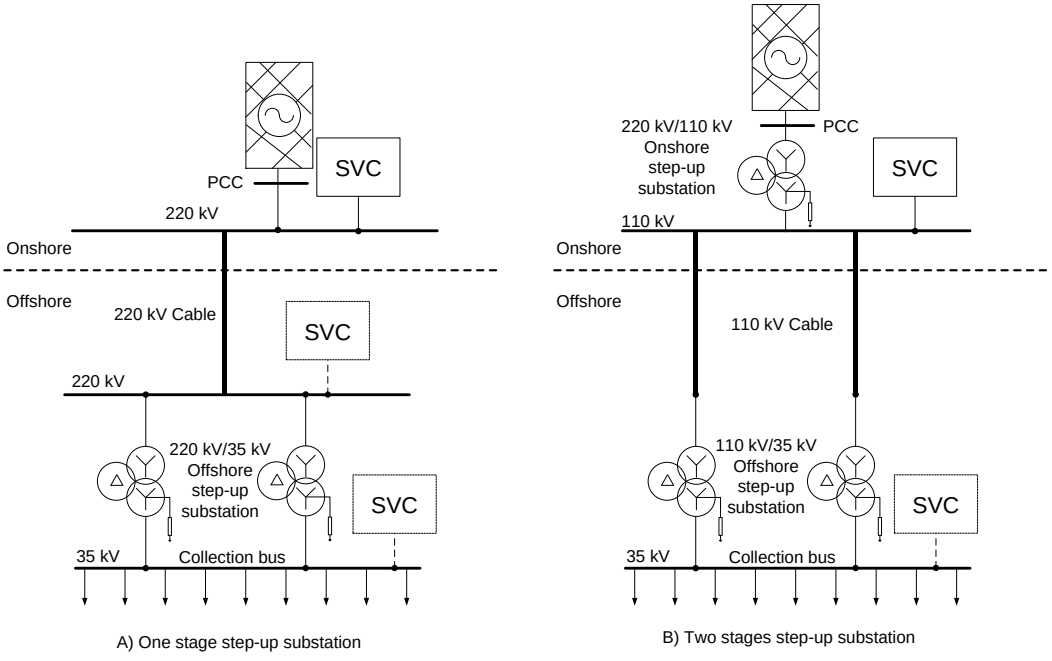



**Figure 4-5; Connection method between the collection bus and the PCC (Offshore wind farm)**

### 4.1.2.2 Collection Systems in Wind Farms

According to the size of wind farm, reliability requirements, there are different topologies of the collection system in wind farm. There are radial topology (Figure 4-6, A), single-sided ring topology (Figure 4-6, B), double-sided ring topology (Figure 4-6, C) and star topology (Figure 4-6, D) [46] [47].

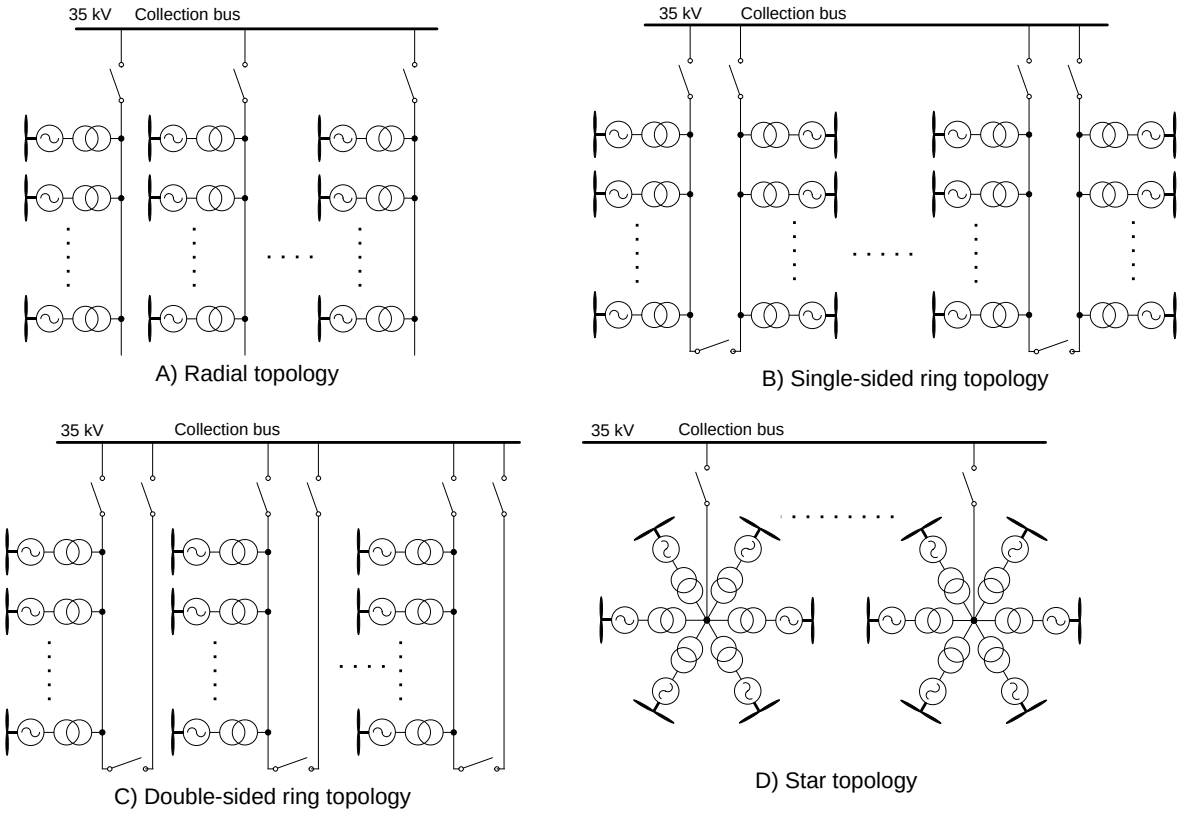



**Figure 4-6; Different topologies of the collection system in wind farm**

This is shown in Figure 4-6, the wind turbines are connected by the collection system with a step-up transformer. Due to the simple structure and less usage of cables, it (type A) is suitable to wind farms whose the rated power is less than 100 MVA. For the large wind farms (>100 MVA), in order to increase the reliability, the ring topology will be applied. The star topology has less reliability than the ring topology and higher costs than radial topology, so there are less wind farms with star topology.

### 4.1.2.3 HVDC Transmission System

The Voltage Source Converter based High Voltage Direct Current (VSC-HVDC) transmission can reduce the transmission losses by HVDC, and also realizes the decoupling control for the active and reactive power to providing dynamic reactive power support. In addition, it can also improve the grid compatibility of wind farm [48] [49].

The typical HVDC transmission system of a wind farm is shown in Figure 4-7. The Wind Farm side Voltage Source Converter (WFVSC) is connected to the collection bus with a

transformer; its output is transmitted to the Grid Side Voltage Source Converter (GSVSC) with DC cables.

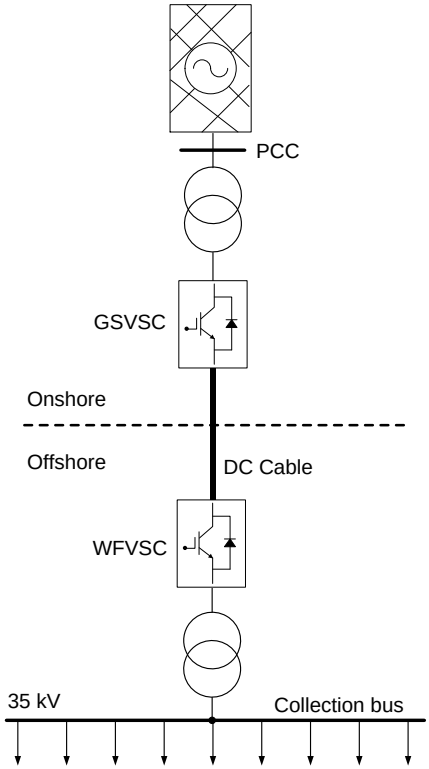



**Figure 4-7; Topology of typical HVDC transmission system of wind farm**

## 4.2 Simplification of Distributed Generation Systems

In order to model the testing grid environment, modeling of the DG systems is also required. There is a lot of research about the detailed electromagnetic transient model of the DG systems [50] [51] [52]. In these researches, the mechanical part, electrical part and control part of the DG system are detailed modeled and simulated. The detailed electromagnetic transient model can accurately reproduce the operating characteristics of DG systems, but it also results in a high computational complexity, which can only be used in off-line simulation. In order to simulate the operating characteristics of DG systems in the real-time simulation of PHIL test system, it is necessary to simplify the model with lower computational complexity.

In this chapter, a detailed electromagnetic transient model of the typical DG system will be analyzed, and then, according to the requirements of PHIL testing, a universal simplifying method will be presented. The validation of the accuracy of this simplified model will be carried out by the comparison between simulation results.

### 4.2.1 Large-scale Grid-connected Photovoltaic Generation System

The detailed electromagnetic transient model of a large-scale grid-connected photovoltaic generation system consists of several sub-models: photovoltaic cells, DC-DC converter, snubber circuit, grid-side inverter, filter and adequate controller, as shown in Figure 4-8.

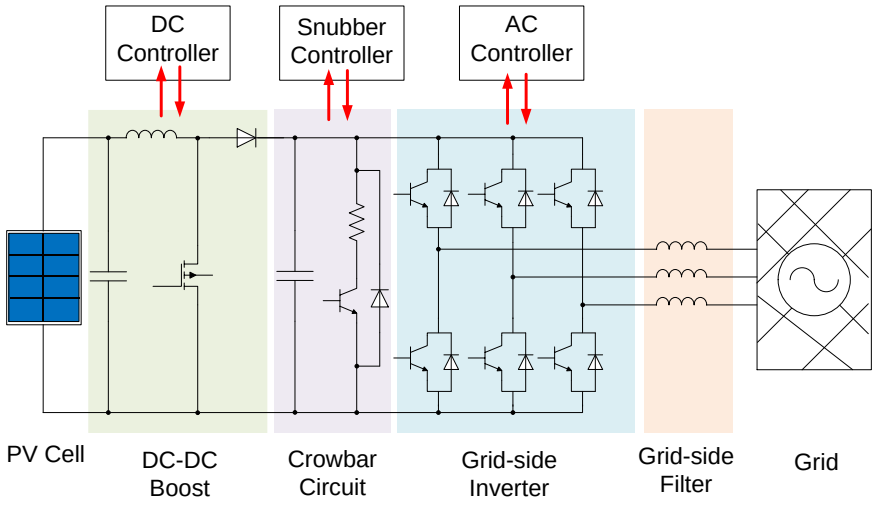



**Figure 4-8; Detailed electromagnetic transient model of a large-scale grid-connected photovoltaic generation system**

#### 4.2.1.1 Photovoltaic Cells

In a large-scale grid-connected photovoltaic generation system, the photovoltaic cells are usually connected in parallel and series as a photovoltaic cell array to raise the DC bus voltage.

The single photovoltaic cell can be equivalent to a photocurrent source and a parallel connected ideal diode [53]. When considering the internal resistance of photovoltaic cell, the equivalent circuit is shown in Figure 4-9.

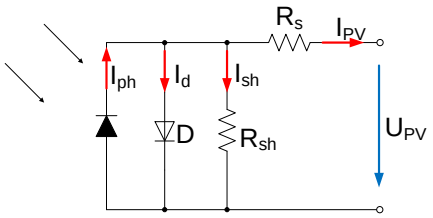



**Figure 4-9; Detailed electromagnetic transient model of a photovoltaic cell**

In Figure 4-9, the $I_{ph}$ is photocurrent, D is the ideal diode, $R_s$ and $R_{sh}$ are the internal resistance of photovoltaic cell, $U_{PV}$ and $I_{PV}$ are the output voltage and current of the PV cell.

The photovoltaic cell can be seen equivalent to a controlled current source. Its output current $I_{PV}$ and voltage $U_{PV}$ are influenced by the light intensity and temperature, and then cause the fluctuation of output power. In order to maximize the usage of solar energy resources, to achieve the maximum power output of PV array, the adjustment of the output voltage $U_{PV}$

according to the light intensity and temperature has to be carried out. This adjustment process is Maximum Power Point Tracking (MPPT) of the PV cells / arrays [54] [55] [56].

### 4.2.1.2 DC-DC Converter

In order to realize the MTTP of PV cell/array, the DC-DC converter is generally used to control the DC bus voltage $U_{PV}$, as shown in Figure 4-10.

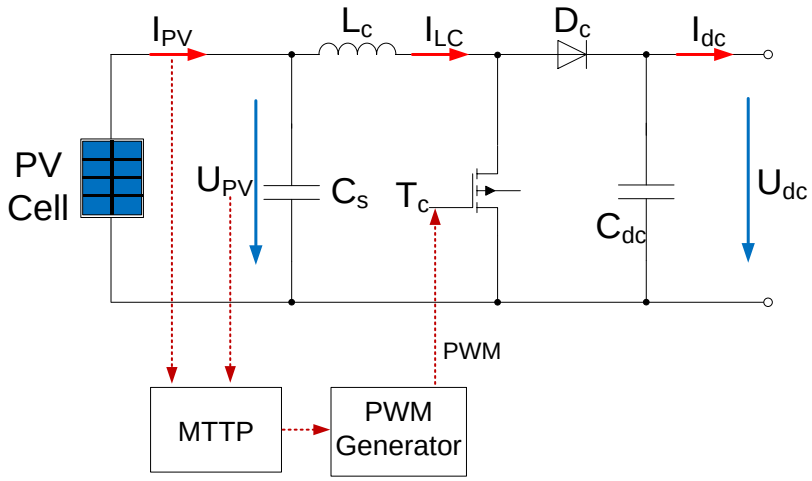



**Figure 4-10; DC-DC boost circuit**

In Figure 4-10, $L_C$ is the boost inductor, $D_c$ is the diode, $C_s$ is the capacitor of the output side of PV cell, $T_c$ is the transistor and the $C_{dc}$ is the capacitor of DC bus. The desired DC voltage can be obtained by controlling the on-off state of the transistor $T_c$.

### 4.2.1.3 Subber Circuit

When a voltage dip occurs, the output power from the grid-side inverter is reduced and the input power from DC side (PV cell and DC-DC converter) keep unchanged, and this causes the power imbalance. In order to balance the input and output power in this system, the subber circuit is needed [57]. When the input power is higher than the output power, the excess energy will be consumed by the crowbar resistance.

Figure 4-11 shows the topology of the DC bus with the snubber circuit. $R_{crowbar}$ is the crowbar resistance, $T_{crowbar}$ is the transistor, $P_{in}$ is the input power from the DC side, $P_{out}$ is the output power to grid-side inverter from DC side, $P_{dc}$ is the consumed power of DC bus. In the steady-state without loss, $P_{dc}$ should be zero.

When the voltage of DC bus higher than the upper threshold, which means the input power is larger than the output power, the crowbar controller will turn the $T_{crowbar}$ on, and the excess energy is consumed by the crowbar resistance. When the voltage of DC bus is lower than the lower threshold, the $T_{crowbar}$ will be turned off.

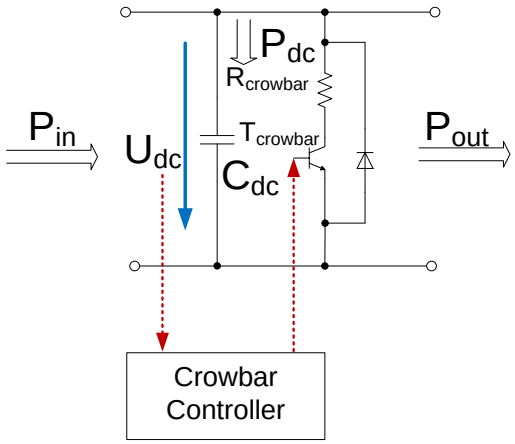



**Figure 4-11; Topology of the DC bus with the snubber circuit**

### 4.2.1.4 Grid-side Inverter

The classical three-phase three-leg structure is usually applied in a large-scale grid-connected photovoltaic generation systems as shown in Figure 4-12. The typical controller structure is also shown in Figure 4-12. The three-phase output current signals ($I_{L1}$, $I_{L2}$, $I_{L3}$) will be transferred into the two quantities ($I_d$, $I_q$) by Park's transformation, and then these two DC quantities will be controlled by two regulators in order to realize the zero steady-error control of the output current. The balance of the input and output power of the inverter is controlled by the DC voltage regulator. So the control reference of $I_d$ is the output from the DC voltage regulator. With the feed-forward voltage compensator, the dynamic performance and the robustness of the control system is enhanced.

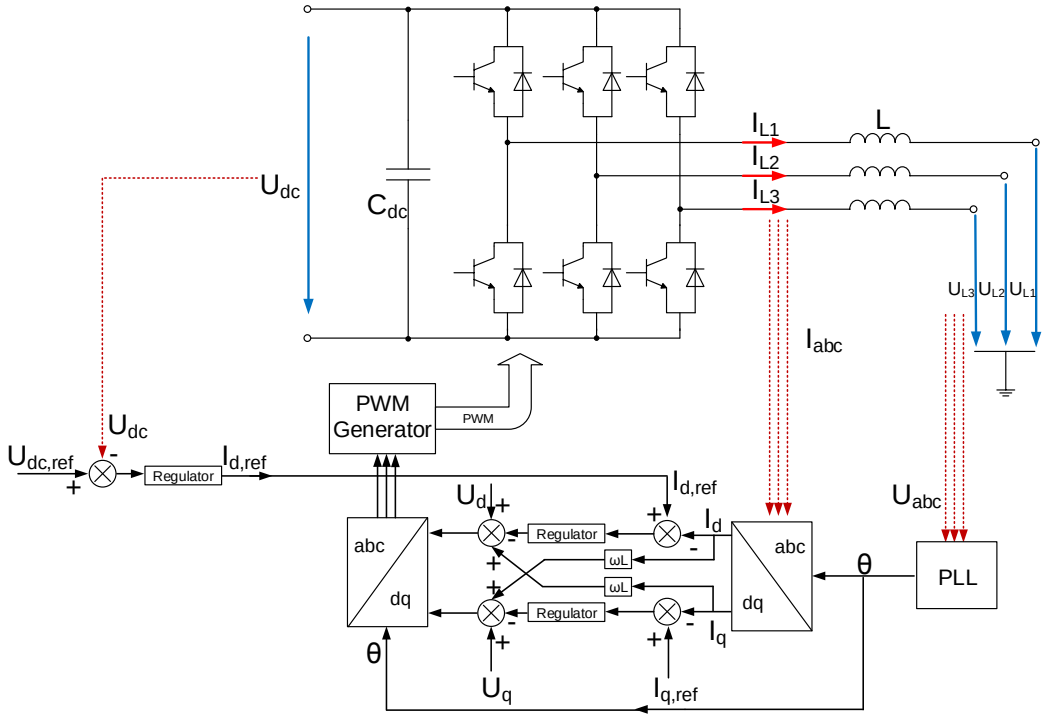



**Figure 4-12; Topology and control structure of the grid-side inverter**

#### 4.2.1.5 Simplification of the Large-scale Grid-connected Photovoltaic Generation System

The light intensity and temperature causes a great impact for the output power of the PV cells, but it has also a slow speed of change, the time constant is usually up to tens of seconds, which is longer than the duration of the PHIL testing process. Hence the light intensity and temperature can be considered as constant during the PHIL testing.

The photovoltaic cell array is operated at the optimum power point, and its output characteristic is approximated as a current source. When the voltage from grid-side changes, it will affect the voltage of DC bus, which will also affect the voltage of the each single photovoltaic cell. But due to the DC capacitor, the voltage of DC bus changes slightly, and this change is shared by each single photovoltaic cell. This reduces the impact for each single photovoltaic cell and keeps the voltage near unchanged.

In summary, in the real-time simulation of PHIL testing, the DC side (PV cell and DC-DC converter) of a large-scale photovoltaic power generation system can be simplified as a controlled current source with constant output power.

The switching frequency of the large-scale grid-side inverter is usually around 3000 Hz. In order to carry out the transient state process of the power electronic equipment in the inverter, the simulation step must be far more than 3000 Hz, such as 1 MHz ~ 50 MHz [58]. According to the requirements of the PHIL testing system in the chapter 3.6.1, the update frequency of PHIL test system is 10 kHz, so the transient state process, which is higher than 1 MHz, does not need to be reproduced in the PHIL testing. Hence, under the precondition of ignoring the transient state process of the power electronic equipment, the grid-side inverter can be simplified as a controlled source.

The simplification of a large-scale grid-connected photovoltaic generation system is shown in Figure 4-13.

In Figure 4-13, the $I_{PV}$ is the output current of the PV array, $C_{dc}$ is the capacitor of DC bus, $R_{crowbar}$ is the crowbar resistance, S is an ideal switch, which is controlled by the crowbar controller. $U_{dc}$ is the voltage of DC bus, $I_{dc}$ is the output current of the DC side. $P_{in}$ is the input power from the DC side. $P_{out}$ is the output power to grid-side inverter from DC side. $L_1$, $L_2$, $L_3$ are the filter inductors, $U_{L1}$, $U_{L2}$, $U_{L3}$ are the output voltage of grid-side inverter, which are controlled by the AC controller.

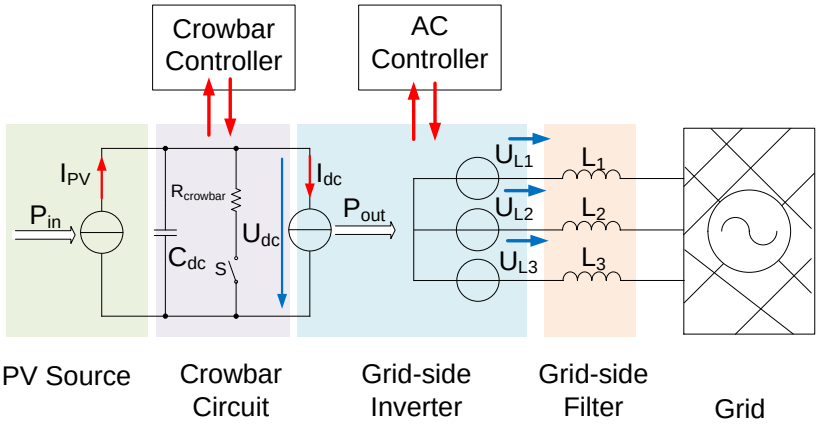



**Figure 4-13; Simplification of a large-scale grid-connected photovoltaic generation system**

The function of the output current of the PV array $I_{PV}$ and the output current of the DC side $I_{dc}$ is presented:

$$\begin{cases} I_{PV} = \dfrac{P_{in}}{U_{dc}} \\ I_{dc} = \dfrac{P_{out}}{U_{dc}} \end{cases} \qquad \text{Eq. 4-1}$$

The input power of the PV array should be set as a constant during the real-time simulation. The output power of the DC side can be calculated by the output current and voltage of the grid-side inverter.

With this simplification method, the switching components and non-linear components in a PV generation system can be simplified as ideal controlled source, the computational complexity of the simplified model is greatly reduced, and the transient response of the photovoltaic power generation is still retains.

### 4.2.2 Direct-drive Permanent Magnet Synchronous Generator

The detailed electromagnetic transient model of the Direct-drive Permanent Magnet Synchronous Generator (D-PMSG) consists of several sub-models: wind blades, shaft system, permanent magnet synchronous generator, generator-side converter, snubber circuit, grid-side inverter and filters, as shown in Figure 4-14.

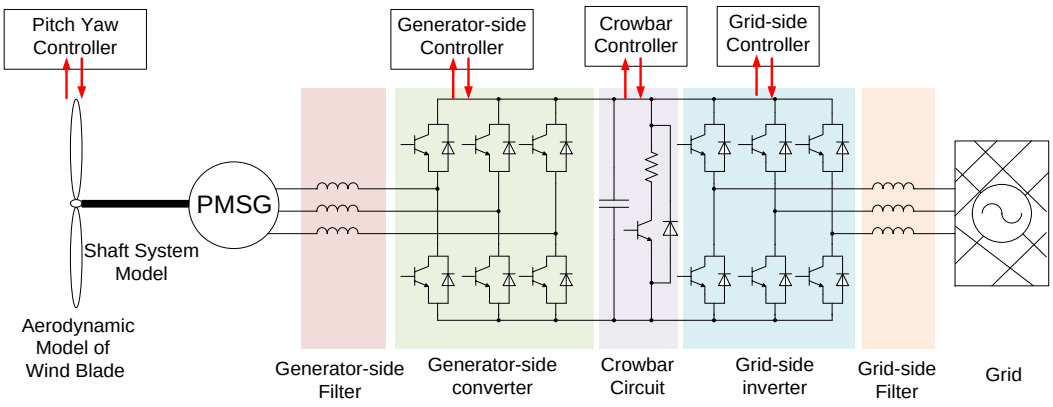



**Figure 4-14; Detailed electromagnetic transient model of D-PMSG**

### 4.2.2.1 Wind Blades, Shaft System and PMSG

The output torque of the wind blades $T_m$ depends on the wind power captured by the wind blades. The captured wind power is closely related to the wind speed, rotational speed of the wind blades, structure of the wind blades and the air density [59]. The captured wind power and the input torque can be presented as:

$$\begin{cases} P_{wind} = \frac{1}{2}\rho c_p(\lambda,\beta)\pi R^2 V_{wind}^3 \\ T_m = \frac{P_{wind}}{\omega_r} \\ c_p(\lambda,\beta) = 0.22\left(\frac{116}{\lambda_i} - 0.4\beta - 5\right)e^{-\frac{12.5}{\lambda_i}} \\ \lambda_i = \frac{1}{\frac{1}{\lambda + 0.08\beta} - \frac{0.035}{1+\beta^3}} \end{cases} \quad \text{Eq. 4-2}$$

$P_{wind}$… Wind power captured by the wind blades;

$T_m$… Output torque of the wind blades;

$\rho$… Air density;

$c_p$… Power coefficient of the wind blades;

R… Length of the wind blade;

$V_{wind}$… Wind speed;

$\omega_r$… Rotational speed of the wind blades

$\lambda$… Tip speed ratio;

$\beta$… Pitch angle of the wind blades.

There are also fluctuations of wind power, so MPPT of D-PMSG is also required. The MPPT of D-PMSG is carried out by the pitch yaw control of the wind blades and control of the generator.

The stator currents of the permanent magnet synchronous generator in d-q axis are presented as:

$$\begin{cases} \dfrac{dI_d}{dt} = \dfrac{1}{L_d}U_d - \dfrac{R}{L_d}I_d + \dfrac{L_q}{L_d}p\omega_r I_q \\ \dfrac{dI_q}{dt} = \dfrac{1}{L_q}U_q - \dfrac{R}{L_q}I_q - \dfrac{L_q}{L_d}p\omega_r I_d - \dfrac{1}{L_q}\lambda p\omega_r \end{cases}$$ Eq. 4-3

$L_d$, $L_q$… Equivalent inductance of the stator windings in d-axis and q-axis;

R… Resistance of the stator windings;

$I_d$, $I_q$… d-axis and q-axis component of stator current;

$U_d$, $U_q$… d-axis and q-axis component of stator voltage;

$\omega_t$… Rotational speed of the generator;

$\lambda$… Magnetic flux of the stator windings;

p… Number of pole pairs.

The electromagnetic torque of the PMSG is presented as:

$$T_{em} = 1.5p(\lambda I_q + (L_d - L_q)I_d I_q)$$ Eq. 4-4

The wind blades, shaft system and PMSG are connected to the grid with a back-to-back converter. This structure isolates the influence of the grid to the generator, the inertia of the generator cannot be seen from the grid side. Therefore, the simplified equation (Eq.4-5) can be used to simulate the dynamics of the mechanical part (wind blades, shaft system and PMSG), which is regarded as a rigid body, the dynamics behaviors between each other are ignored.

$$J_T \frac{d\omega_t}{dt} = T_{em} - T_m$$ Eq. 4-5

$J_T$… Total inertia of mechanical part (wind blades, shaft system and PMSG);

$\omega_t$… Rotational speed of the generator;

$T_m$… Mechanical torque;

$T_{em}$… Electromagnetic torque.

### 4.2.2.2 Back-to-back Converter

The back-to-back converter of D-PSMG consists of a generator-side converter, snubber circuit and a grid-side inverter. The snubber circuit and grid-side inverter are same as in grid-connected photovoltaic generation, so here the focus on the generator-side converter. This is shown in Figure 4-15, the generator-side converter consists of three-leg IGBT bridges, generator-side filter inductors. The stator of PMSG is connected to the input of the generator-side converter.

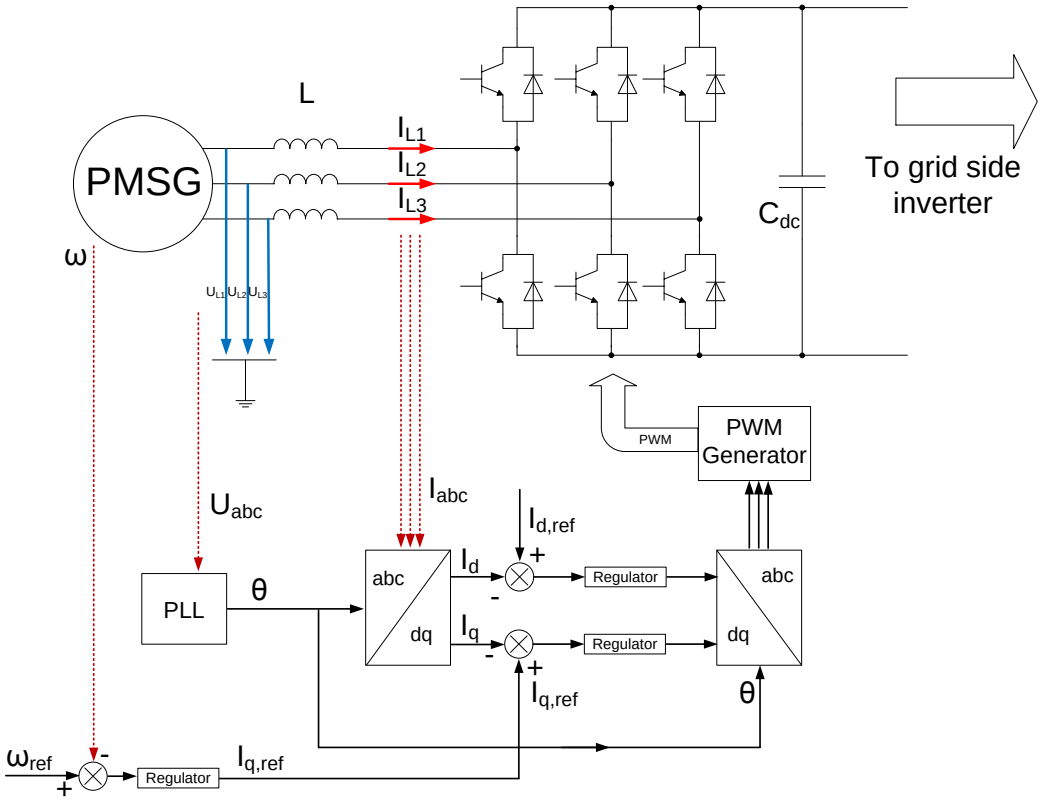



**Figure 4-15; Topology and control structure of the generator-side converter**

The dual closed loop control is applied in generator-side converter. The outer loop is the rotational speed of the generator control, the input of the regulator is the error of rotational speed, the output of regulator is the reference of the q-axis component of current $I_{q,ref}$. The control variables of inner loop regulator are the d-axis and q-axis component of current. The output of the inner loop regulator will go thought the inverse Park's transformation to the PWM generator, in order to control the IGBT bridges.

### 4.2.2.3 Simplification of the Direct-drive Permanent Magnet Synchronous Generator

Because of the wind speed is a time-varying function, the output power of the D-PMSG is also a time-varying function. But the wind speed can be considered as constant during the PHIL testing.

The back-to-back converter isolates the influence of grid to the generator, so the D-PMSG can keep the original operation state when the short-term (seconds class) variation of grid voltage occurs. Additionally, the time constant of large-scale PMSG is usually 2-6s [60] [61], the rotational speed of the PMSG will almost not change during the short-term variation of grid voltage. Therefore, the wind blades, shaft system, PMSG and the generator-side converter can be simplified as a current source with constant output power. Then the simplification of the D-PMSG can also use the simplification of a large-scale grid-connected photovoltaic generation system in Figure 4-13.

Therefore, the simplified model in Figure 4-13 is a universal simplified model for the inverter based grid-connected DG system, which is suitable in PHIL testing.

### 4.2.3 Validation of the Simplified Method by Simulation

In order to verify the accuracy of the simplified model of a DG system in this chapter, a detailed electromagnetic transient model and a simplified model of a 1 MVA grid-connected photovoltaic generation system are set up in Matlab/Simulink. The simulation step of the detailed model will be set to 1 μs, the simulation step of the simplified model will be set to 100 μs.

The parameters of the detailed electromagnetic transient model are presented in Table 4-1.

| Parameter Name | Value |
|---|---|
| Rated power | 1 MVA |
| Rated output voltage | 690 V |
| Switching frequency of grid-side inverter | 3000 Hz |
| Rated voltage of DC bus | 1300 V |
| Capacitor of DC bus | 6.25 mF |
| Crowbar resistance | 2 Ω |
| Upper threshold of DC bus voltage | 1360 V |
| Lower threshold of DC bus voltage | 1310 V |
| Inductance of filter | 0.594 mH |
| Equivalent resistance of filter | 0.01 Ω |

**Table 4-1; Parameters of the grid-connected photovoltaic generation system**

The validation will be carried out by comparison of the simulation result of the detailed model and simplified model in different voltage dips situation. When the residual voltage is reduced to 0.88 p.u. and the duration of the voltage dip is 0.5 s, the comparison of the simulation result of the detailed model and simplified model are shown in Figure 4-16, Figure 4-17 and Figure 4-18.

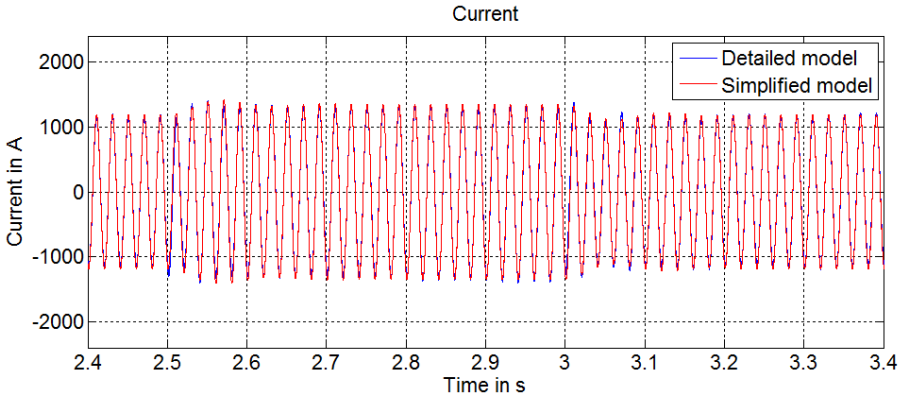



**Figure 4-16; Output current of phase L2 with 0.88 p.u residual voltage**

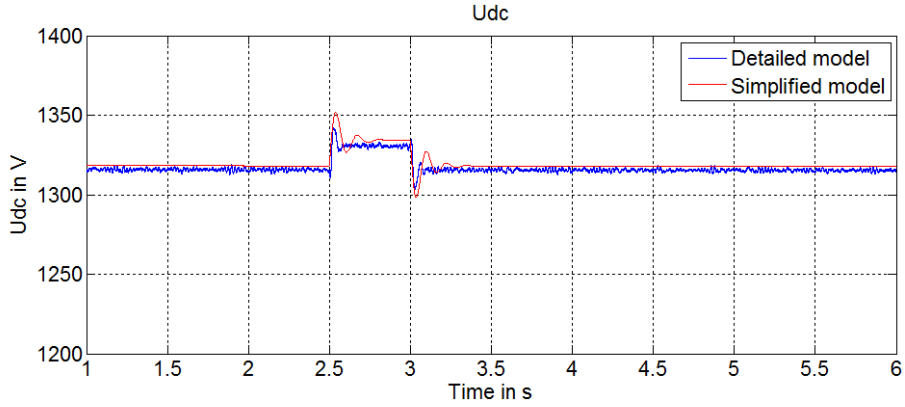



**Figure 4-17; Voltage of the DC bus with 0.88 p.u residual voltage**

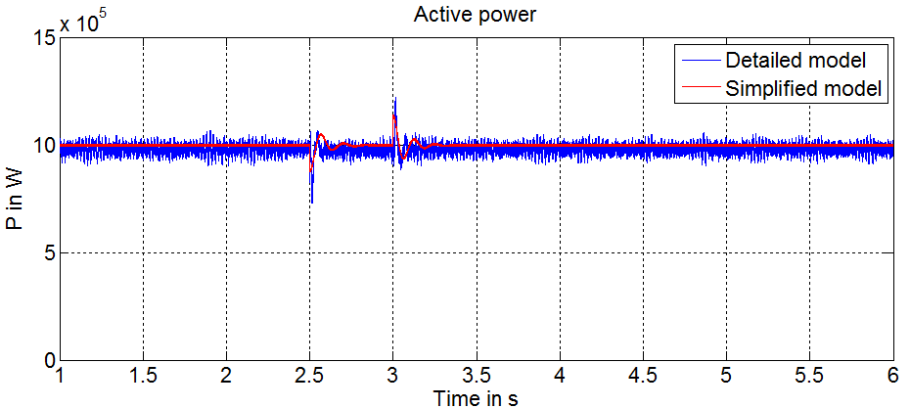



**Figure 4-18; Output active power with 0.88 p.u residual voltage**

This is shown in Figure 4-16, Figure 4-17 and Figure 4-18, the simulation results of the simplified model and the detailed model are approximately coincident. When the voltage dip occurs, the grid-side inverter increases the output current (Figure 4-16) in order to balance the power transferred in DC bus. Due to the large residual grid voltage, the voltage of the DC bus is not exceed the upper threshold, so the snubber circuit is not trigged (Figure 4-17). Therefore, the output active power remains constant during the voltage dip.

When the residual voltage is 0.50 p.u. and the duration of the voltage dip is 0.5 s, the comparison of the simulation result of the detailed model and simplified model are shown in Figure 4-19, Figure 4-20 and Figure 4-21.

As shown in Figure 4-19, Figure 4-20 and Figure 4-21, the simulation results of the simplified model and the detailed model are approximately coincident, even if the simulation step of the simplified model is far bigger than in the detailed model.

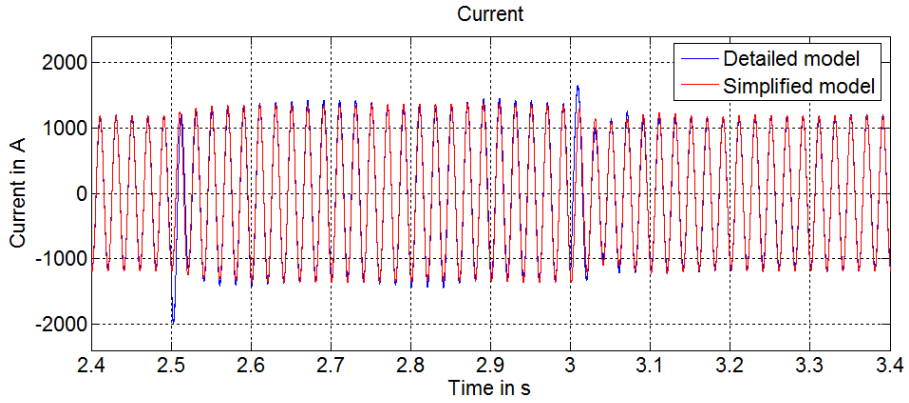



**Figure 4-19; Output current of phase L2 with 0.50 p.u residual voltage**

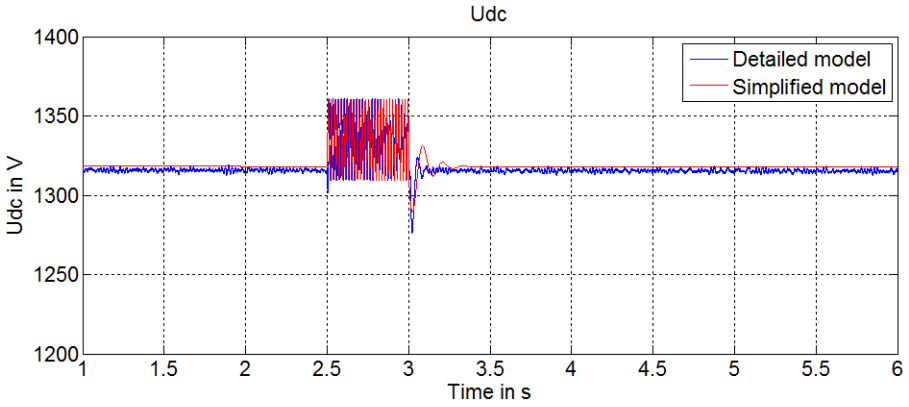



**Figure 4-20; Voltage of the DC bus with 0.50 p.u residual voltage**

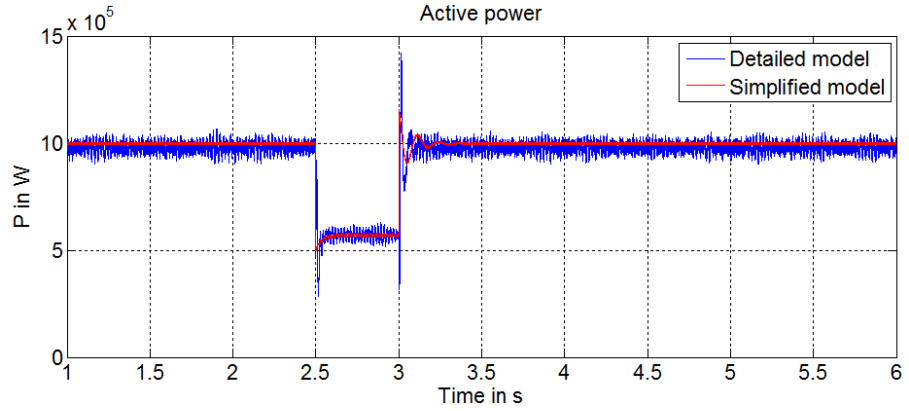



**Figure 4-21; Output active power with 0.50 p.u residual voltage**

When the voltage dip occurs, the grid-side inverter increases the output current (Figure 4-19) in order to balance the power transferred in DC bus, but due to the limitation of the output current of the grid-side inverter, a part of the input power from the DC side will be stored into the DC capacitor, resulting in an increase of the DC bus voltage and also trigger the snubber circuit (Figure 4-20). Because the snubber circuit consumes the extra power, during the voltage dip, the output active power of the grid-side inverter will be reduced (Figure 4-21).

When the residual voltage is 0.15 p.u. and the duration of the voltage dip is 0.5 s, the comparison of the simulation result of the detailed model and simplified model are shown in Figure 4-22, Figure 4-23 and Figure 4-24.

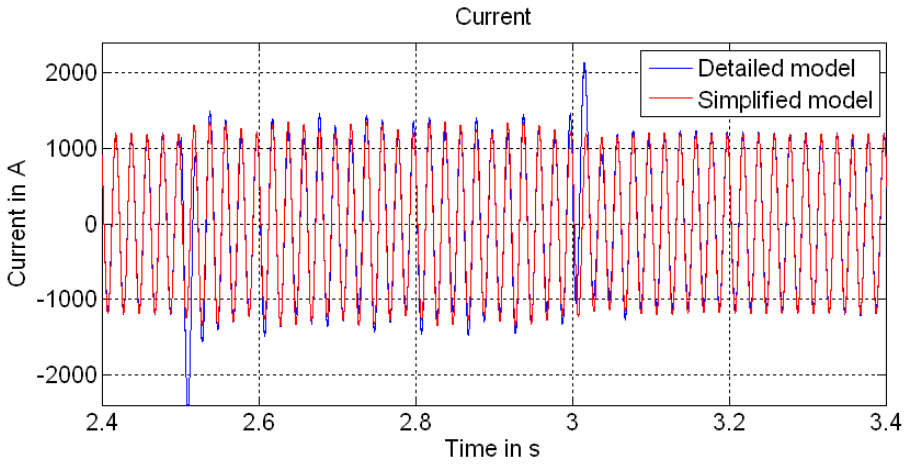



**Figure 4-22; Output current of phase L2 with 0.15 p.u residual voltage**

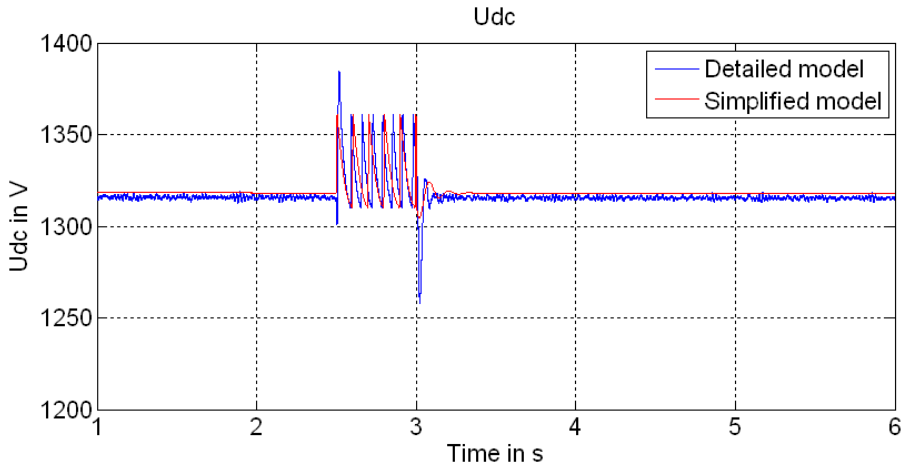



**Figure 4-23; Voltage of the DC bus with 0.15 p.u residual voltage**

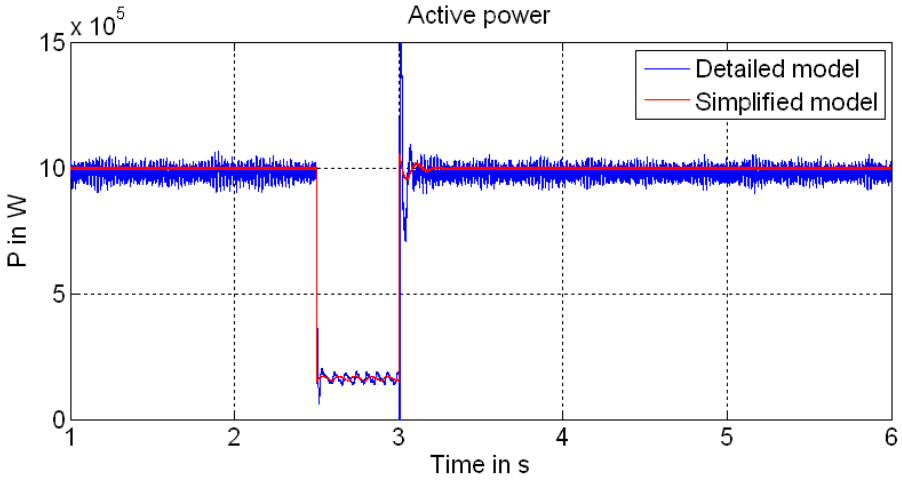



**Figure 4-24; Output active power with 0.15 p.u residual voltage**

The simulation results show that the dynamic response of the detailed electromagnetic transient model and the simplified model are approximately coincident in different voltage

dips situation. The accuracy of the simplified model is verified. Due to the simplification, the simulation efficiency is greatly improved. In the real-time simulator (dSpace) with 2.8 GHz CPU frequency, the duration of each simulation period of this simplified model is only 1.7 μs, which the total simulation step in 100 μs. Such a simplified model can fully meet the real-time requirements of real-time computing.

## 4.3 Equivalent Simplification of Power Plants

Typically power plants contain dozens of DG systems, if each DG system and the collection system are detailed modeled, it will lead to the sharp increase of the computational complexity. Therefore, the equivalent simplification of the group of DG systems and the collection system is necessary.

In this chapter, the equivalent simplification of the group of DG systems will be carried out, based on the simplification of the single DG system (chapter 4.2). Then, on the basis of the summary of the topology of the collection system (chapter 4.1), the equivalent simplification of the collection system will be also carried out. Finally, the accuracy of the equivalent simplification will be verified by the simulation of a real offshore wind farm.

### 4.3.1 Equivalent Simplification of the Group of Distributed Generation System based on the Power Electronics Devices

The equivalent simplification methods for the synchronous and asynchronous generator are presented in lot of literatures [62] [63] [64]. The dynamic characteristics of the DG systems based on power electronics are more related to its control algorithm, rather than the parameters of its hardware. Therefore, the equivalent simplification methods for the synchronous and asynchronous generator cannot be applied in power electronics based on DG systems. This chapter will present an equivalent simplification method for these SG systems.

The topology of the equivalent simplification for DG systems based on the power electronics devices is shown in Figure 4-25. It consists of the equivalent transformer and equivalent grid-connected inverter. The voltage of PCC is U´, the output current is I´, and the input power to the inverter is P´. It is assumed that, during the dynamic processes of the power systems, the voltages of grid connection point of each DG systems are the same, all hardware parameters and the control parameters are equal in each DG systems, and the input power P´ is constant.

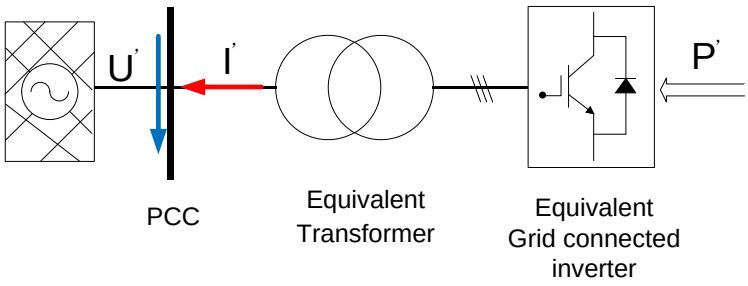



**Figure 4-25; Topology of the equivalent simplification for DG systems based on the power electronics devices**

The output power of the equivalent simplification model is the sum of each DG system, and then the following equations can be obtained:

$$\begin{cases} U' = U \\ P' = nP \\ I' = nI \end{cases} \quad \text{Eq. 4-6}$$

U…Voltage of grid connection point of single DG system;

I…Output current to the grid connection point of single DG system;

n… Number of DG systems.

According to the topology and control structure of the grid-side inverter in Figure 4-12 and the simplified model in Figure 4-13, the equations group of the single inverter with Proportional-Integral (PI) regulator can be obtained:

$$\begin{cases} \dfrac{1}{C_{dc}}\int (I_{PV} - I_{dc})dt = U_{dc} \\ (U_{dc} - U_{dc,ref})(k_{P,dc} + \dfrac{k_{I,dc}}{s}) = I_{d,ref} \\ (I_{d,ref} - I_d)(k_{P,ac} + \dfrac{k_{I,ac}}{s}) + U_d - \omega L I_q = U_{d,ref} \\ (I_{q,ref} - I_q)(k_{P,ac} + \dfrac{k_{I,ac}}{s}) + U_q - \omega L I_d = U_{q,ref} \end{cases} \quad \text{Eq. 4-7}$$

$k_{P,dc}$… Proportional coefficient of the DC side control;

$k_{I,dc}$… Integral coefficient of the DC side control;

$k_{P,ac}$… Proportional coefficient of the AC side control;

$k_{I,ac}$… Integral coefficient of the AC side control.

The equivalent simplification model of the inverter has the same structure as the single inverter. Therefore, the equations group of the equivalent simplification model of the inverter can be obtained with Eq.4-7:

$$\begin{cases} \frac{1}{C_{dc}^{'}}\int(I_{PV}^{'}-I_{dc}^{'})dt=U_{dc}^{'} \\ (U_{dc}^{'}-U_{dc,ref}^{'})(k_{P,dc}^{'}+\frac{k_{I,dc}^{'}}{s})=I_{d,ref}^{'} \\ (I_{d,ref}^{'}-I_{d}^{'})(k_{P,ac}^{'}+\frac{k_{I,ac}^{'}}{s})+U_{d}^{'}-\omega LI_{q}^{'}=U_{d,ref}^{'} \\ (I_{q,ref}^{'}-I_{q}^{'})(k_{P,ac}^{'}+\frac{k_{I,ac}^{'}}{s})+U_{q}^{'}-\omega LI_{d}^{'}=U_{q,ref}^{'} \end{cases}$$ Eq. 4-8

According to the Eq.4-8, and the topology in Figure 4-12 and Figure 4-13, the relationship of the control variables can be obtained:

$$\begin{cases} I_{PV}^{'}=nI_{PV} \\ I_{dc}^{'}=nI_{dc} \\ U_{dc}^{'}=U_{dc} \\ U_{dc,ref}^{'}=U_{dc,ref} \\ I_{d}^{'}=nI_{d} \\ I_{q}^{'}=nI_{q} \\ I_{d,ref}^{'}=nI_{d,ref} \\ I_{q,ref}^{'}=nI_{q,ref} \end{cases}$$ Eq. 4-9

By inserting the Eq.4-9 into Eq.4-8, the relationship between the equivalent simplification model and single inverter model is presented:

$$\begin{cases} C_{dc}^{'}=nC_{dc} \\ L^{'}=\frac{L}{n} \\ k_{P,dc}^{'}=nk_{P,dc} \\ k_{I,dc}^{'}=nk_{I,dc} \\ k_{P,ac}^{'}=\frac{k_{P,ac}}{n} \\ k_{I,ac}^{'}=\frac{k_{I,ac}}{n} \end{cases}$$ Eq. 4-10

It is also assumed that, the voltage drop and the power loss of the each transformer are the same, then the equivalent impedance of the equivalent transformer is presented as:

$$Z_{T}^{'}=\frac{Z_{T}}{n}$$ Eq. 4-11

$Z_T$… Impedance of the single transformer.

The equations Eq.4-10 and Eq.4-11 are the universal equivalent simplification method for the DG systems based on power electronics.

### 4.3.2 Equivalent Simplification of the Collection System

According to the analysis of the collection system in power plants (chapter 4.1), the distances between the DG systems increase with the increment of the scale of power plant. In wind farms, in order to reduce the wake interaction between the wind turbines, the distances of each wind turbine are usually longer than 1km. Therefore, the influence of the transmission lines between DG systems cannot be ignored in the equivalent simplification of the collection system.

The basic connection mode in the collection system can be divided in series connections (Figure 4-26) and parallel connections (Figure 4-27).

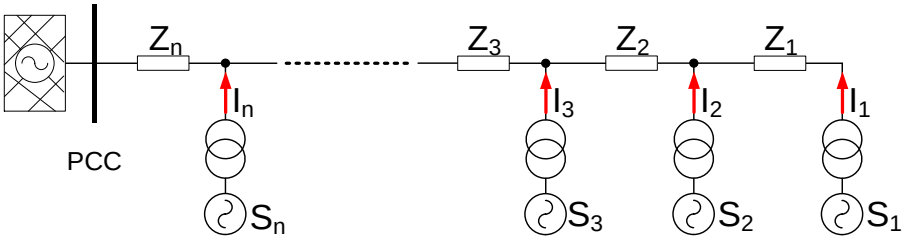



**Figure 4-26; Series connection mode of the collection system**

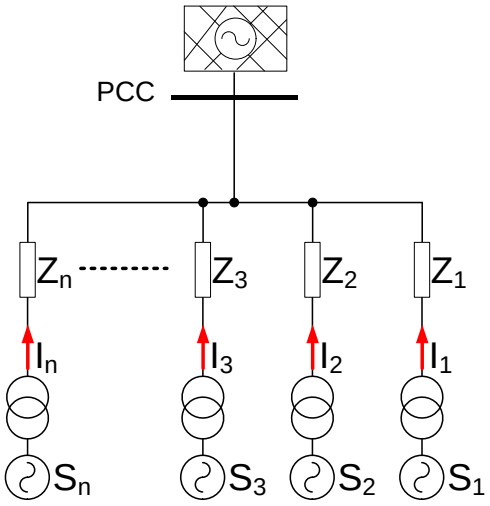



**Figure 4-27; Parallel connection mode of the collection system**

This is shown in Figure 4-26, the number of DG systems is n, the output power of each DG system are $S_1$, $S_2$, $S_3$, … $S_n$. The output current of each DG system are $I_1$, $I_2$, $I_3$, … $I_n$. The impedance of transmission line between two DG systems are $Z_1$, $Z_2$, $Z_3$, … $Z_n$. It is assumed that, the DG system and its transformer can be simplified to one current source. It is also assumed that, the output power of each DG system is same, then the output current of each DG system is also same, as shown in the following equation.

$$\begin{cases} S_1 = S_2 = S_3 = \cdots = S_n = S \\ I_1 = I_2 = I_3 = \cdots = I_n = I \end{cases} \qquad \text{Eq. 4-12}$$

The loss of transmission line between two DG systems are:

$$\begin{cases} P_{loss,Z1} = I_1^2 Z_1 = I^2 Z_1 \\ P_{loss,Z2} = (I_1 + I_2)^2 Z_2 = 2^2 I^2 Z_2 \\ P_{loss,Z3} = (I_1 + I_2 + I_3)^2 Z_3 = 3^2 I^2 Z_3 \\ \vdots \\ P_{loss,Zn} = (I_1 + I_2 + I_3 + \cdots I_n)^2 Z_n = n^2 I^2 Z_n \end{cases} \quad \text{Eq. 4-13}$$

The total loss of the all transmission line is:

$$\sum_{k=1}^{n} P_{loss,Zk} = I^2 (Z_1 + 2^2 Z_2 + 3^2 Z_3 + \cdots n^2 Z_n) \quad \text{Eq. 4-14}$$

Eq.4-14 can be simplified into:

$$\sum_{k=1}^{n} P_{loss,Zk} = I^2 \sum_{k=1}^{n} k^2 Z_k \quad \text{Eq. 4-15}$$

The equivalent simplification of the collection system is shown in Figure 4-28. Z´ is the equivalent impedance of the all transmission line. I´ is the current, which is flowing through this equivalent impedance. S´ is the output power of all DG systems.


**Figure 4-28; Equivalent simplification of the collection system**

According to the Eq.4-12, the current and power of the equivalent simplification model can be presented:

$$\begin{cases} S' = \sum_{k=1}^{n} S_k = S_1 + S_2 + S_3 + \cdots + S_n = nS \\ I' = \sum_{k=1}^{n} I_k = I_1 + I_2 + I_3 + \cdots I_n = nI \end{cases} \quad \text{Eq. 4-16}$$

The loss of the equivalent simplification of the collection system is:

$$P_{loss,Z'} = I'^2 Z' \quad \text{Eq. 4-17}$$

By inserting the Eq.4-15 and Eq.4-16 into Eq.4-17, the equivalent impedance of the series connection mode of the collection system is:

$$Z' = \frac{1}{n^2}\sum_{k=1}^{n} k^2 Z_k \qquad \text{Eq. 4-18}$$

In the same way, the equivalent impedance of the parallel connection mode of the collection system is:

$$Z' = \frac{1}{n^2}\sum_{k=1}^{n} Z_k \qquad \text{Eq. 4-19}$$

The topology of the equivalent transmission line is the π model, as shown in Figure 4-29. The C´ is the equivalent capacitance of the total transmission lines. The reactive power is proportional to the square of the voltage on the capacitor. It is assumed that, the voltage of the collection system is constant. Therefore, the equivalent capacitance of the all transmission line is the sum of all capacitance of each transmission line in the collection system, which is presented:

$$C' = \sum_{k=1}^{n} C_k \qquad \text{Eq. 4-20}$$

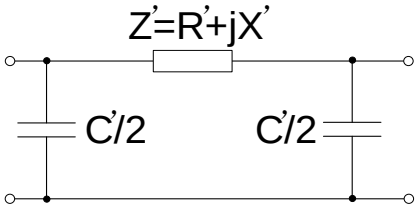



**Figure 4-29; Topology of the equivalent transmission line**

The equations Eq.4-18, Eq.4-19 and Eq.4-20 are the equivalent simplification method of the collection system.

### 4.3.3 Validation of the Equivalent Simplified Method by Simulation

In order to verify the accuracy of the equivalent simplification method of the collection system in this chapter, a real offshore wind farm will be modeled in detailed and its equivalent simplification modeling will be also carried out. Both the detailed model and the simplified model are set up in Matlab/Simulink. The simulation step of the detailed model will be set to 1 μs, the simulation step of the equivalent simplification model will be set to 100 μs.

#### 4.3.3.1 Description of the Offshore Wind Farm

The cable routing of the example offshore wind farm is shown in Figure 4-30. There are 28 wind turbines in this wind farm, which are connected to the onshore step-up transformer with 4 x 35 kV-cables. The site #2 (yellow point) is the EUT, is also the observation point of this simulation.

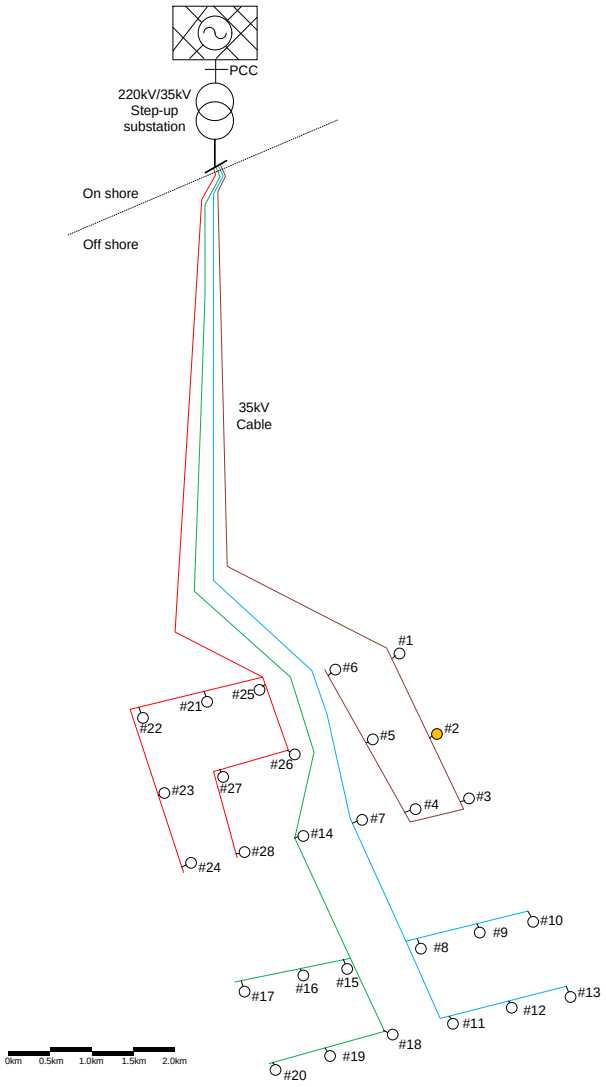



**Figure 4-30; Cable routing of the example offshore wind farm**

The single diagram is shown in Figure 4-31. The wind turbines in this wind farm are all D-PMSG, the parameters are already shown in Table 4-1. The parameters of cables and transformers in the wind farm are shown in Table 4-2, Table 4-3 and Table 4-4.

| Parameter Name | Value |
|---|---|
| Voltage level | 35 kV |
| Sectional area | 185 $mm^2$ |
| Specific resistance | 0.0991 Ω/km |
| Specific inductance | 0.62 mH/km |
| Specific capacity | 190 nF/km |

**Table 4-2; Parameters of the cable in wind farm**

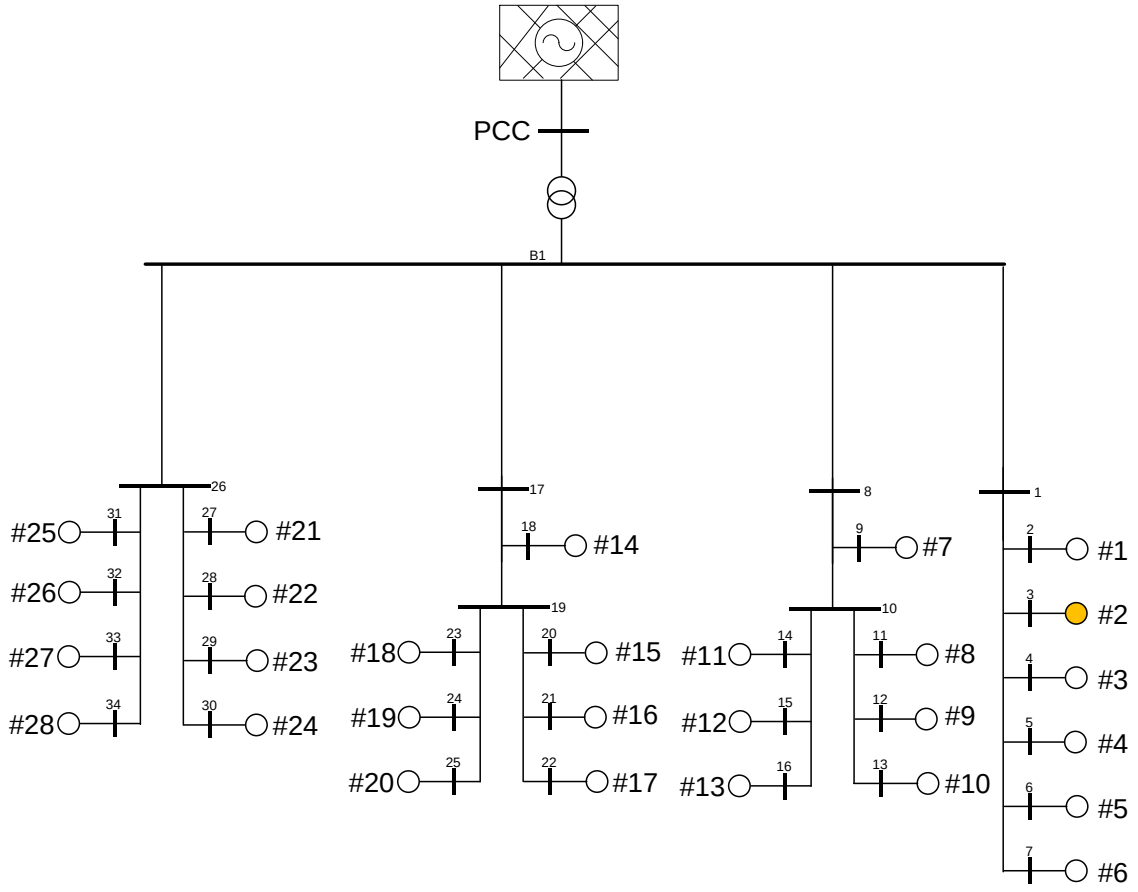



**Figure 4-31; Single line diagram of the example offshore wind farm**

| Parameter Name | Value |
|---|---|
| Rated power | 63 MVA |
| Primary side voltage | 220 kV |
| Secondary side voltage | 35 kV |
| Connection type | Star connected in secondary side |
| Grounding mode | low resistance neutral grounding in secondary side |
| Grounding resistance | 40 Ω |
| Impedance voltage Uk | 10.5% |

**Table 4-3; Parameters of onshore transformer**

| Parameter Name | Value |
|---|---|
| Rated power | 1 MVA |
| Primary side voltage | 35 kV |
| Secondary side voltage | 0.69 kV |
| Connection type | Dyn |
| Impedance voltage Uk | 6.5% |

**Table 4-4; Parameters of the output transformer of wind turbines**

### 4.3.3.2 Equivalent simplification model of the offshore wind farm

In order to meet the different requirements of the simulation, two different equivalent simplification models are established. The equivalent simplification model of the internal of the wind farm is used to reproduce the interaction with the neighboring wind turbines (Figure

4-32). The equivalent simplification model of the whole wind farm is used to reproduce the interaction with the other wind farms (Figure 4-33).

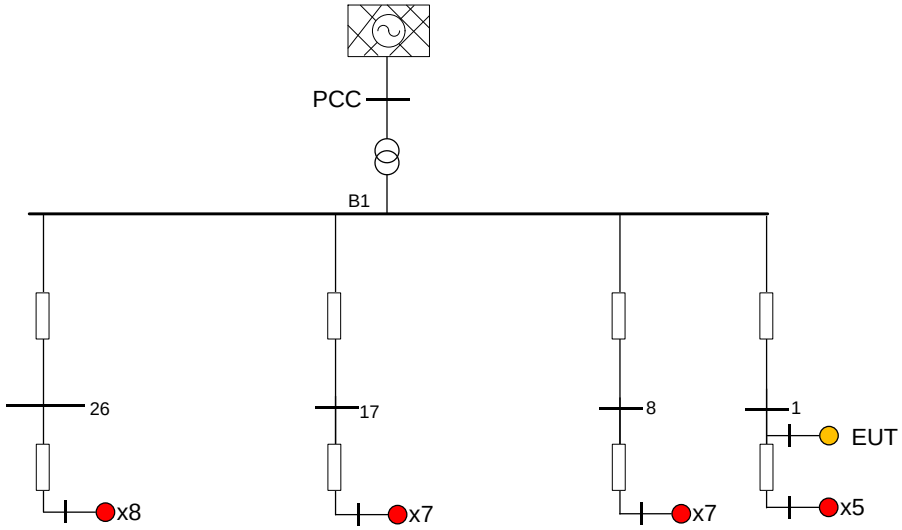



**Figure 4-32; Equivalent simplification model of the internal of the wind farm**

In Figure 4-32, the wind turbines and cables in the same branch are equivalent to one wind turbine and one cable. The red point is the equivalent simplification model of wind turbines, the number with x is the number of the equivalent wind turbines.

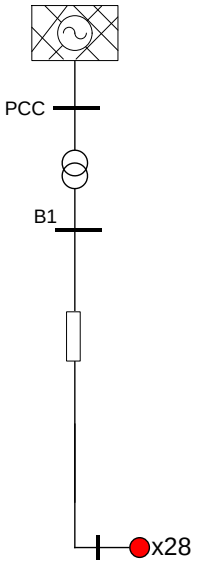



**Figure 4-33; Equivalent simplification model of the whole wind farm**

In Figure 4-33, the whole collection system is equivalent to one wind turbine and one cable, in order to maximum reduce the computational complexity with a maximum degree.

### 4.3.3.3 Comparison of the Simulation Results

The voltage of the EUT (observation point) and the voltage of the collection bus (B1) of the equivalent simplification model of the internal of the wind farm are chosen to be compared. Because there is no EUT (observation point) in equivalent simplification model of the whole wind farm, only the voltages and currents of collection bus will be chosen to be compared

When the voltage dip occur, the residual voltage at the PCC is 0.88 p.u. and the duration of the voltage dip is 0.2 s, the simulation results is shown in Figure 4-34 and Figure 4-35.

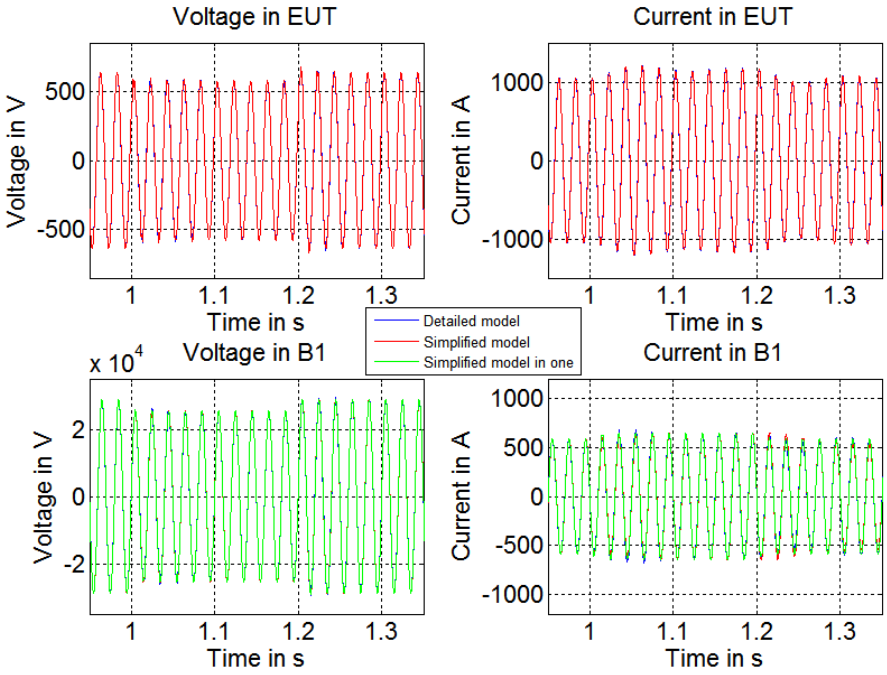



**Figure 4-34; Phase voltage and current of the EUT and collection bus with a 0.88 p.u residual voltage**

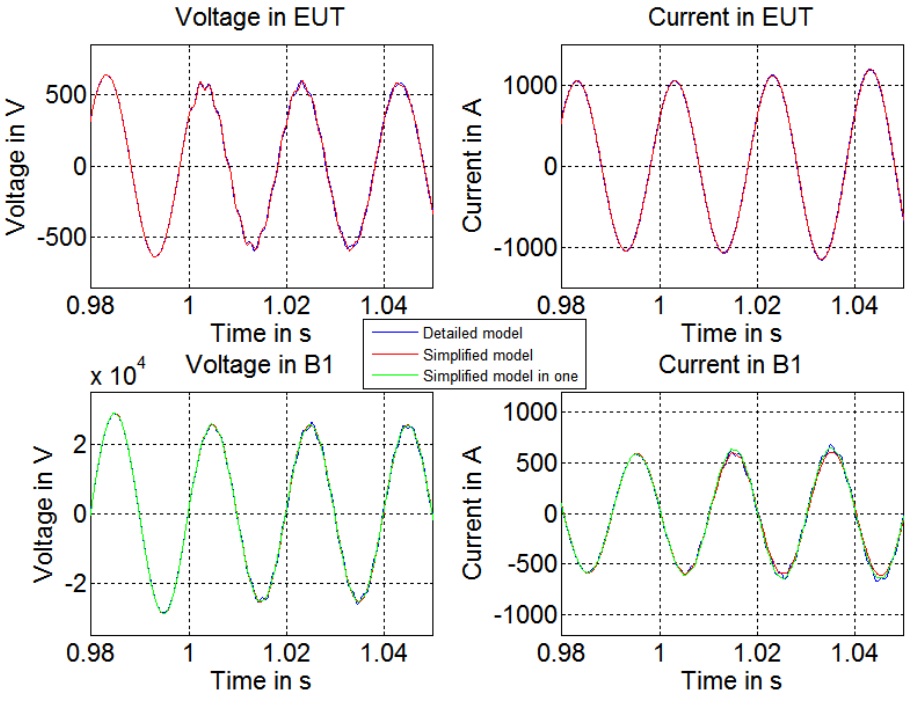



**Figure 4-35; Phase voltage and current of the EUT and collection bus with a 0.88 p.u residual voltage (enlarged)**

This is shown in Figure 4-34 and Figure 4-35, the blue curve is the simulation results of the detailed model, the red curve represent the simulation results of the equivalent simplification model of the internal of the wind farm, the green curve is the simulation results of the

equivalent simplification model of the whole wind farm. These three curves are basically overlapping in the above figures.

When the voltage dip occurs, with a residual voltage at the PCC of 0.50 p.u. and a duration 0.2 s, the simulation results is shown in Figure 4-36 and Figure 4-37.

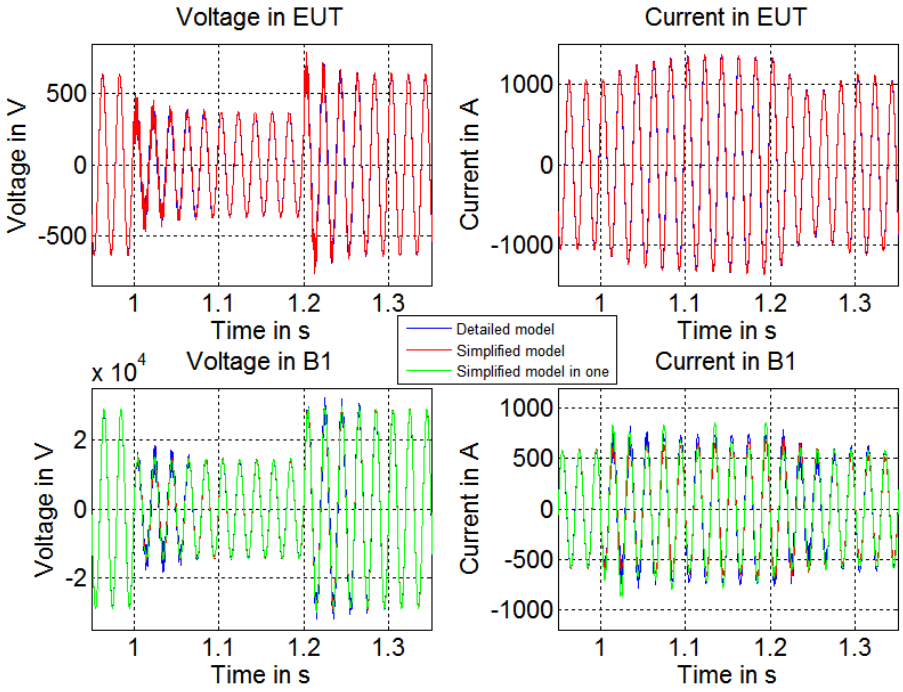



**Figure 4-36; Phase voltage and current of the EUT and collection bus with a 0.50 p.u residual voltage**

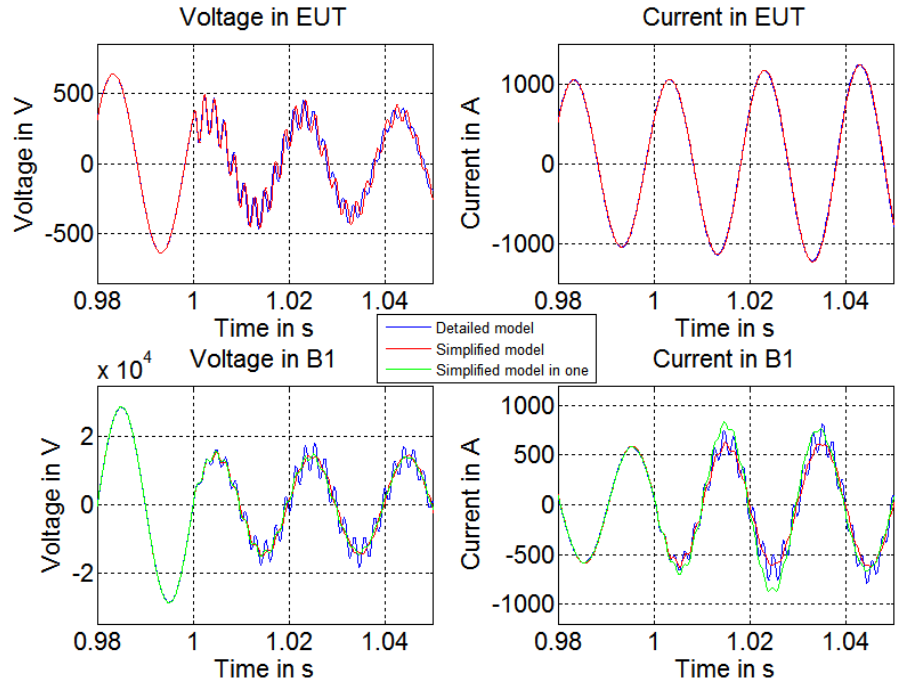



**Figure 4-37; Phase voltage and current of the EUT and collection bus with a 0.50 p.u residual voltage (enlarged)**

This is shown in Figure 4-36 and Figure 4-37, the voltage and current curves are basically overlapped in the figures.

In these simulation results, the dynamic response of the equivalent simplification model of wind farm is basically the same as detailed model, which proves the correctness of the presented equivalent simplification method. Due to this simplification method, the computational complexity is greatly reduced. In the real-time simulator (dSpace), the duration of each simulation period of this simplified model (Figure 4-32) is only 4.8 μs, which is below the limited of the 100μs (total simulation time in real-time-calculator).

## 4.4 Summary of this Chapter

In this chapter, the typical grid environment with the large DG systems is analyzed and summarized, including the regional AC grid and the collection system in power plants. The references of the testing grid environment for the PHIL testing are provided.

The principle of the typical DG systems is analyzed, and the detailed numerical simulation model of typical DG systems is built. Based on the analysis of the dynamic behavior of the DG systems during the variation of grid voltage, and the basic principle of the inverter, the universal simplification method of DG systems based on power electronics is presented. The collection system in power plants is also be analyzed, based on this analysis, the universal equivalent simplification method of the power plants is presented. Through the simulation results with different test conditions, the simplified model of the DG system and the power plant has a good accuracy in low computational complexity, which also with large simulation step.

# 5 High Power Amplifier

In a Power Hardware-in-the-Loop test system, the power amplifier is responsible for the transfer the calculated result of the grid model software from the real-time simulator to the hardware EUT. According to the system requirement analysis in chapter 3.6, the basic requirement of the power amplifier in high power class PHIL test system is high power, high accuracy and fast response speed. These three requirements are often contradictory, as shown in Figure 5-1.

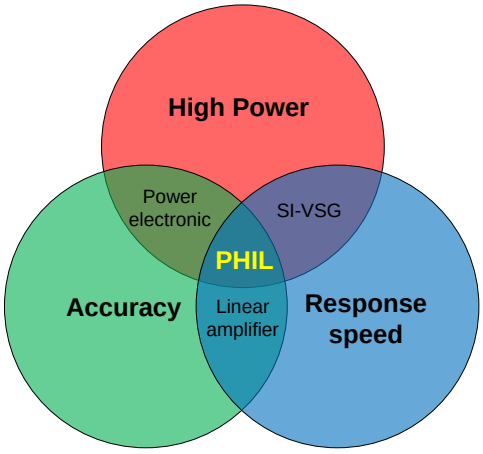



**Figure 5-1 Requirements and contradictory of power amplifier in PHIL test system**

The most commonly used test generator of grid compatibility testing are shunt impedance based voltage sags generators [65], linear power amplifiers and switched mode power amplifiers [66].

The shunt impedance based voltage sags generator has a simple structure. It can produce a sharp drop and rise of voltage in the high power situation. Therefore, it is widely applied in the Low Voltage Ride Thought testing. But due to the limitation of system impedances (chapter 2.4), the credibility of testing will be weakened.

The linear power amplifier has a series of advantages, such as, high accuracy, fast response speed and also wide operation bandwidth. Because of the limitation of the hardware, the power capacity of the linear power amplifier is usually smaller than 100 kVA. It is only suitable for testing of small PV generation systems.

The switched mode power amplifier can output the high accuracy testing waveform with high power. But the response speed and operation bandwidth is limited by the hardware and the control strategy. Therefore, the response speed and operation bandwidth of the common commercial switched mode power amplifiers cannot meet the requirements of PHIL test system.

Therefore, this thesis will develop a switched mode power amplifier which can meet the requirements of the high power PHIL test. In this chapter, the detailed requirements of such a

power amplifier will be presented based on the performance of PHIL testing (chapter 5.1). According to the given requirements, the design of the hardware circuit topology will be presented (chapter 5.2), the Proportional-Resonant (PR) regulator will be designed (chapter 5.3). Finally, the design and performance of the switched mode power amplifier will be verified by simulation testing in the real world (chapter 5.4).

## 5.1 The Power Amplifier Requirements in PHIL Test System

The EUT in this thesis are the grid-connected equipment of large DG systems, with a power capacity is not larger than 500 kVA. According to the engineering experiences, during the LVRT testing, the EUT will produce a transient current, which is not larger than 1.5 times rated current. Therefore, the power amplifier should also be able to withstand not less than 1.5 times rated current of EUT in the transient state. So the rated power of the power amplifier in the PHIL test system in this thesis is 800 kVA.

In order to cover most of the test conditions, the rated output line voltage of the power amplifier is 400V. Since overvoltage occurs in the real power systems, then the PHIL test system also needs to reproduce this phenomenon. The overvoltage tolerance of the EUT in the testing standards [67] [68] [69] is 120% of the rated voltage. Taking into account the transient overvoltage situation in the real-time simulation, the output voltage range of the power amplifier can be appropriately increased. The output voltage range of the power amplifier in the PHIL test system is 0%-135% rated voltage, which is 0V-540V phase voltage.

During the grid compatibility testing of a DG systems, the DG system will transfer the power to the power amplifier. In order to save energy, four-quadrant rectifier is applied in the power amplifier, which provides the bi-directional energy transfer ability for the PHIL test system. The rated power of EUT in this thesis is 500 kVA, considering the variations of output power of EUT, the rated power of the four-quadrant rectifier is also 800 kVA.

The response time, accuracy and expected harmonic frequency range are already described in chapter 3.6. The detailed requirements are shown in Table 5-1. These are also the universal requirements of power amplifier in PHIL test system.

| Parameter Name | Value |
|---|---|
| Rated phase voltage $U_N$ | 400 V |
| Voltage range | 0%-135% $U_N$ |
| Rated frequency $f_N$ | 50/60 Hz |
| Frequency range | 47 Hz – 63 Hz |
| Expected harmonic frequency range | <2000 Hz |
| Accuracy of voltage | <±0.3% $U_N$ |
| Accuracy of frequency | <0.3% $f_N$ |
| Response time | ≤100 μs |
| THD (<50th) | <1% |

**Table 5-1; Requirements of power amplifier in PHIL test system**

## 5.2 Hardware Design

### 5.2.1 Hardware Topology

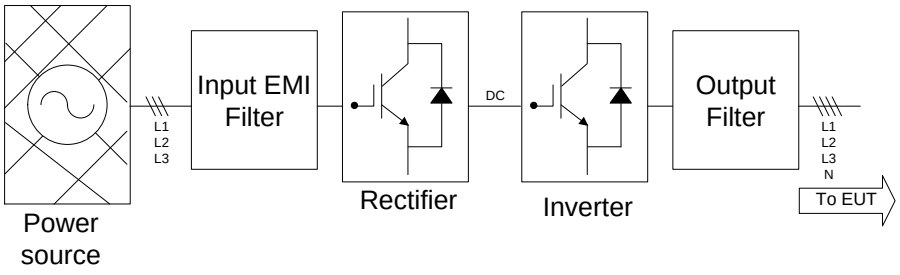



**Figure 5-2; General topology of the switched mode power amplifier**

The general topology of the switched mode power amplifier is shown in Figure 5-2, from left is the input EMI (electromagnetic interference) filter, the rectifier, DC bus, inverter, output filter. Both of the filters are responsible for reducing the unwanted output harmonics. The bi-directional energy transfer ability is required in PHIL testing. Therefore the rectifier has to be a four-quadrant rectifier, in order to transfer the power from the DG system to the external power source. The inverter produces the testing waveform.

Because the output function of the power amplifier is realized by the inverter, the hardware topology of the inverter is studied in this chapter. The commercial three-phase three-wire three-leg structure of the inverters is often used for the power amplifiers in PHIL testing [70] [71] [72] [73] [74]. The three-phase three-leg inverter cannot produce the waveform with zero sequence components. Therefore it cannot simulate the grid situation such as single-phase voltage dips. In order to produce the testing waveform with zero sequence components, literatures [75] [76] gave the inverter with three-phase four-wire four-leg structure. But the harmonic components of each phase cannot be adjusted independently. The most appropriate topology of the inverter is three sets of independent single-phase inverters [66] [77], as shown in Figure 5-3. This topology can realize the independent output of three-phase testing waveform and harmonic components. It fully meets the output requirements of the PHIL test system. Other topologies of inverters, such as matrix converter structure [78] or the two coupled three-phase three-leg inverter structure [79], also cannot meet the requirements of PHIL testing.

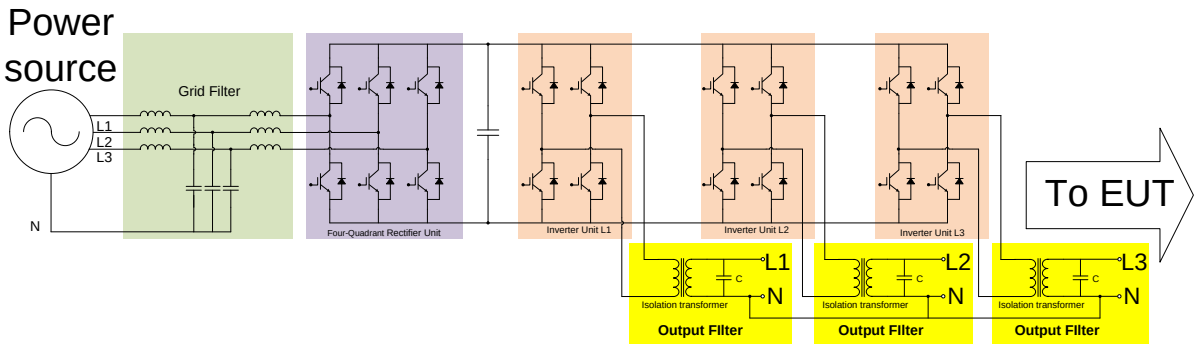



**Figure 5-3; Topology of the power amplifier in PHIL test system**

This is shown in Figure 5-3, the power amplifier is composed of a rectifier unit and the inverter units. The rectifier unit has a three-phase LCL filter and a three-phase four-quadrant rectifier. The inverter unit has three sets of independent single phase inverter units.

In order to increase the current-carrying capability of invert units, the paralleled power modules will be applied in the inverter. Several power modules are connected in parallel in each leg of inverter unit. The output current of the inverter is divided into paralleled power module, which reduces the current of each power modules. This method can increase the upper limit of the allowable switching frequency of each power module, and also increase the response speed and the operation bandwidth. In Figure 5-3, the each power module (IGBT unit) is represented by four paralleled power modules, with a rated current of each power module of 300 A. Therefore, during the PHIL testing, the switching frequency can be set to 10 kHz.

Each output LC filter is composed of a capacitor and an isolating transformer with leakage inductance, in order to solve the short circuit problem of the DC side [80]..

### 5.2.2 Output Filter Design

The output of the inverters is realized by the pulse width modulation, the inverter convert the DC voltage from rectifier unit to the AC voltage waveform. This output waveform contains a large number of harmonics of the switching frequency. Therefore, the low pass filters have to be installed in order to eliminate the unwanted harmonics. The LC low pass filter is applied in this power amplifier. The filter inductor is replaced by the leakage inductance of the isolating transformer, as shown in Figure 5-4.

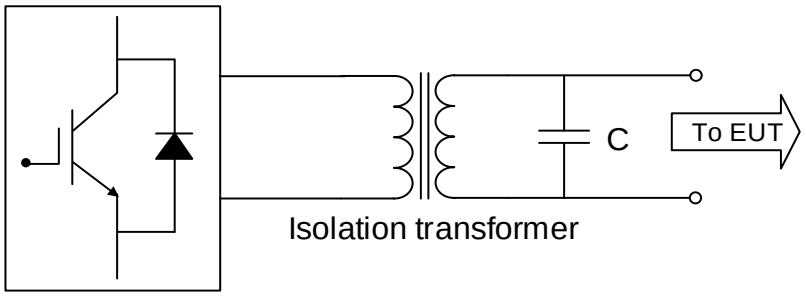



**Figure 5-4; Topology of filter of power amplifier**

According to the requirements in Table 5-1, the expected harmonic frequency range is up to 2000 Hz. Therefore the cutoff frequency of this filter is set to 2500 Hz.

The determination of the inductance of the filter is related to the allowed ripple current, according to the engineering experiences, the allowed ripple current should be smaller than 15%~30% rated current. Due to the high accuracy requirement in PHIL testing, here the allowed ripple current is set to 10% rated current. The relationship between the inductance and allowed ripple current is presented:

$$\Delta I_{\max} = 10\% \frac{S}{U_N} \qquad \text{Eq. 5-1}$$

$$\Delta I_L = \frac{U_{DC} - U_N}{L} \frac{D(t)}{f_s} \qquad \text{Eq. 5-2}$$

$\Delta I_{MAX}$… Maximum ripple current;

S… Rated power;

$U_N$ … Rated output voltage;

$U_{DC}$ … Rated DC bus voltage;

L… Filter inductance;

D(t) … Duty cycle;

$f_s$… Switching frequency.

The relationship between the output voltage and DC bus voltage is:

$$U_N = D(t) U_{DC} \qquad \text{Eq. 5-3}$$

By inserting the Eq.5-3 into Eq.5-2:

$$\Delta I_L = \frac{(U_{DC} - U_N)U_N}{Lf_s U_{DC}} \quad \text{Eq. 5-4}$$

In order to get the maximum ΔIL, the Eq.5-5 has to be met, and the maximum ripple current is given in Eq.5-6:

$$U_N = \frac{U_{DC}}{2} \quad \text{Eq. 5-5}$$

$$\Delta I_{\max} = \frac{U_{DC}}{4Lf_s} \quad \text{Eq. 5-6}$$

From Eq.5-6 the inductance should med the requirement:

$$L \geq \frac{U_{DC}}{4\Delta I_{\max} f_s} \quad \text{Eq. 5-7}$$

With the parameter in Table 5-1, the inductance should be 0.1415 mH. So the leakage inductance of isolated transformer is set to 0.14 mH.

The cutoff frequency of the LC low pass filter is presented as:

$$f_{cut} = \frac{1}{2\pi\sqrt{LC}} \quad \text{Eq. 5-8}$$

From the Eq.5-8, the capacitance of this filter can be calculated by:

$$C = \frac{1}{4\pi^2 f_{cut}^2 L} \quad \text{Eq. 5-9}$$

The cutoff frequency in this filter is 2500 Hz. Therefore the calculated capacitance is 28.63 μF. In this thesis, the capacitance is set to 30 μF.

## 5.3 Control Strategy

### 5.3.1 Review of the Control Strategy of the Inverter in Power Hardware-in-the-Loop Test Systems

The control strategy directly affects the accuracy and the response speed and other performances. According to the design of the hardware in chapter 5.2, this thesis uses three sets of independent single-phase inverters to generate three-phase signal. Therefore, the control strategy for a single phase inverter is studied.

The most commonly used control strategy in the commercial high power inverters is the periodic feedback control. Due to its simplicity and robustness, low demands on sensors,

ADC and signal processor, it has been widely applied. The periodic control for utility frequency (50/60 Hz) is the RMS feedback control [81], for high frequency it is the FFT feedback control [82] [83]. In PHIL testing, the reference signals of the amplifier comes from the real-time calculated results from the grid model, it have to cost a plurality of periods to get the effective value (RMS feedback control) or amplitude and phase (FFT feedback control) of this reference signals from real-time simulation. Then the requirement of the response speed cannot be met..

The literature [84] applied the single loop Proportional-Integral (PI) control in a single phase inverter of the PHIL test system. It has good robust performance. But the steady-state error cannot be eliminated, and the dynamic behavior is also not ideal.

The literature [85] applied the PI control based on the Park`s transformation. In order to apply the Park`s transformation to a single phase inverter of the PHIL test system, the single phase single is delayed for 1/4 period to get a orthogonal signal. Due to the delay of 1/4 period, the requirement of the response speed also cannot be met.

The literature [86] applied the discrete-time Linear Quadratic Regulator (LQR) for single phase inverters of the PHIL test system. The LQR has small overshoot, fast response speed and small steady-state error, but its robustness is not ideal.

Since the understanding of the requirements of the PHIL test system of above literatures is not comprehensive, those control strategies of the power amplifier cannot meet the requirements for the complete PHIL testing. In the following chapter, the control strategy of the power amplifier in PHIL test system will be designed based on the requirements of the PHIL test system in chapter 3.6 and chapter 5.1.

### 5.3.2 Modeling of the Inverter

In order to design the control strategy, the modeling of the single phase inverter is required, as shown in Figure 5-5.

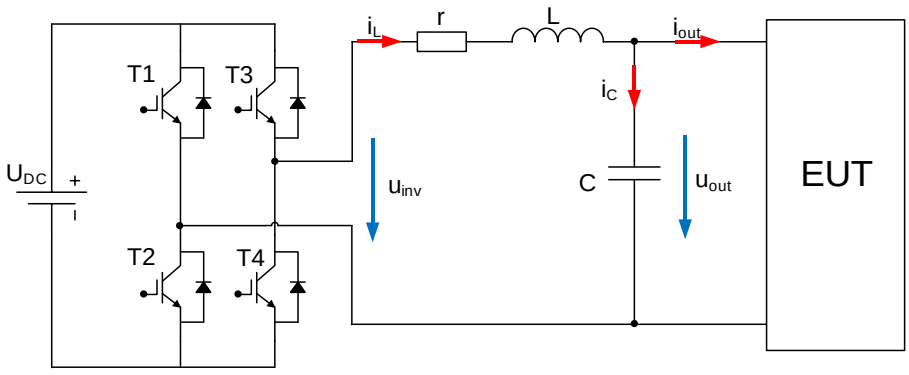



**Figure 5-5; Topology of the single phase inverter with filter**

This is shown in Figure 5-5, the $U_{DC}$ is the voltage of the DC bus. T1, T2, T3 and T4 are the four IGBTs. The filter consists of the filter inductance L, the filter capacitance C and also the equivalent resistance r. $U_{inv}$ is the output voltage of the inverter bridge, $U_{out}$ is the output voltage of the filter. $i_L$ is the current of the filter inductor, the $i_{out}$ is the output current. In PHIL test system, the output current is related to the EUT, so it can be seen as an external disturbance. The inverter is composed of two parts, which are piecewise linear and nonlinear system. According to the engineering experiences, the state-space averaging technique is often used to solve this problem. The inductor current $i_L$ and the output voltage $U_{out}$ are chosen to be state variables, the state-space matrix is presented as:

$$\begin{bmatrix} \dot{u}_{out}(t) \\ \dot{i}_L(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & -\frac{r}{L} \end{bmatrix} \cdot \begin{bmatrix} u_{out}(t) \\ i_L(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C} \\ \frac{1}{L} & 0 \end{bmatrix} \cdot \begin{bmatrix} u_{inv}(t) \\ i_{out}(t) \end{bmatrix} \qquad \text{Eq. 5-10}$$

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} u_{out}(t) \\ i_L(t) \end{bmatrix}$$

The transfer function can be obtained by Eq.5-10:

$$U_{out}(s) = \frac{U_{inv}(s)}{LCs^2 + rCs + 1} - \frac{Ls + r}{LCs^2 + rCs + 1} I_{out}(s) \qquad \text{Eq. 5-11}$$

The unipolar Sinusoidal Pulse Width Modulation (SPWM) will be applied in this power amplifier. The unipolar SPWM can double the equivalent output switching frequency [87]. When the switching frequency is far higher than the expected output frequency, the inverter bridge can be considered as a linear amplifier. The block diagram is shown in Figure 5-6.

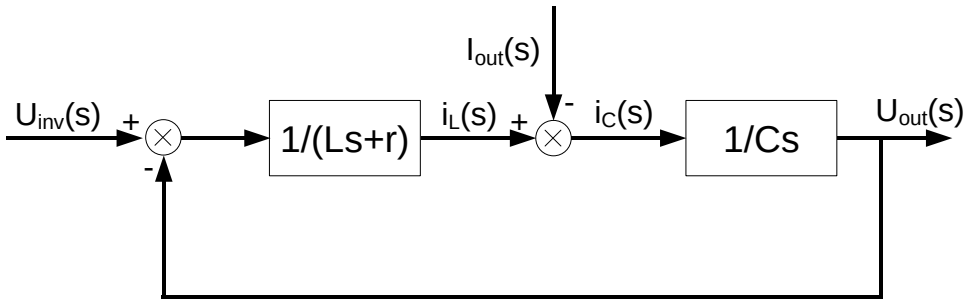



**Figure 5-6; Block diagram of the single phase inverter with filter**

### 5.3.3 Structure of the Control Strategy

In order to ensure the high accuracy, fast response speed and good robust performance, this thesis applies the dual loop feedback control. The inner loop regulator controls current signal to increase the dynamical behavior. The outer loop regulator controls the voltage to reduce the steady-state error.

The block diagram of the inverter with regulators is shown in Figure 5-7.

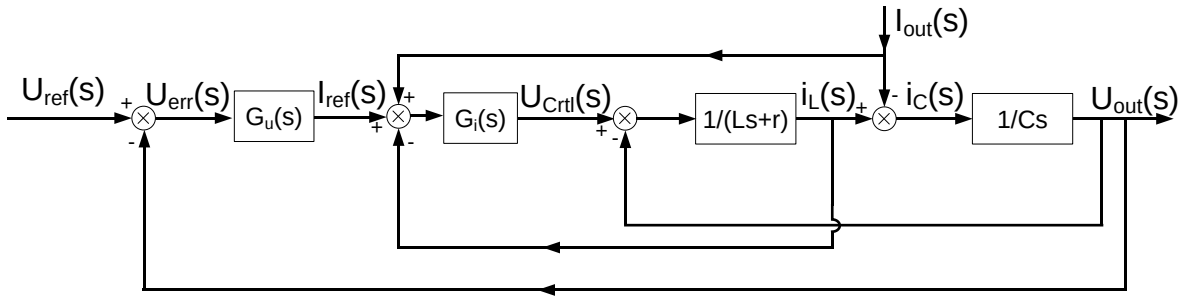



**Figure 5-7; Block diagram of the inverter with regulator**

In Figure 5-7, the error $U_{err}(s)$ between the reference voltage $U_{ref}(s)$ and output $U_{out}(s)$ is the input into the voltage regulator $G_u(s)$. Its output is the reference current $I_{ref}(s)$. With the difference of the output current $I_{out}(s)$ and the inductor current $I_L(s)$, the current regulator $G_i(s)$ produces the control signal $U_{Ctrl}(s)$.

From the block diagram in Figure 5-7, the transfer function of the system can be obtained:

$$U_{out}(s) = G_V(s)U_{ref}(s) + G_Z(s)I_{out}(s) \qquad \text{Eq. 5-12}$$

Which:

$$\begin{cases} G_V(s) = \dfrac{G_u(s)G_i(s)}{CLs^2 + C(G_i(s)+r)s + G_u(s)G_i(s) + 1} \\ G_Z(s) = -\dfrac{Ls + r}{CLs^2 + C(G_i(s)+r)s + G_u(s)G_i(s) + 1} \end{cases} \qquad \text{Eq. 5-13}$$

$G_V(s)$ is the closed loop transfer function from the output voltage to the reference voltage. In ideal situation, the output voltage should follow the reference voltage, that means that in this case the gain of the $G_V(s)$ is 1, error is 0. $G_Z(s)$ is the closed loop transfer function from the output voltage to output current, which is also the equivalent the output impedance of the inverter. In an ideal situation, this should be 0. The design of the regulator should enhance the tracking performance, and also reduce the influence of the equivalent output impedance $G_Z(s)$ to suppress the disturbances from EUT.

The differential of the output voltage $U_{out}(s)$ corresponds to the capacitor current $I_C(s)$. Therefore the control of the capacitor current in the inner loop can also increases the response speed of the output voltage and the suppression of disturbances. But the output current and the inductor current cannot control the capacitor current. Therefore, the protection of the over current cannot be carried out in the digital controller. So in this thesis, the different of the output current and the inductor current is used to replace the capacitor current, in order to increase the response speed and realize the protection of the over current in the digital controller.

### 5.3.4 Proportional-Resonant Regulator

Firstly, the Proportional-Integral regulator is analyzed to introduce the concept of Proportional-Resonant regulator. The transfer function of PI regulator is presented as:

$$G_{PI}(s) = k_P + \frac{k_I}{s} \qquad \text{Eq. 5-14}$$

$k_P$… Proportional coefficient;

$k_I$… Integral coefficient.

The PI regulator is equivalent to the system with one additional pole and one additional zero. The pole is located in the origin of the coordinates, and improves the steady performance of the system. The zero is located on the axis of the left half plane, improves the damping of the system.

But the PI regulator cannot follow the AC signal without steady-state error. In order to reduce this steady-state error, the integral coefficient has to be enlarged, but then the phase shift between the reference and the output is also increased. When the proportional coefficient is enlarged, this can cause a system oscillation. In the frequency domain, the PI regulator is equivalent to a low pass filter. The high frequency signal will be attenuated by the PI regulator. Hence the requirement for the operation bandwidth cannot be met. A new control strategy is needed, which can achieve the tracking of the AC signal without steady-state error, has a good dynamic performance, and meets the requirements of operation bandwidth.

Aiming at requirements above, the Proportional-Resonant (PR) regulator is presented:

$$G_{PR}(s) = k_P + \frac{2k_R s}{s^2 + \omega_0^2} \qquad \text{Eq. 5-15}$$

$K_P$… Proportional coefficient;

$K_R$… Resonant coefficient;

$\omega_0$…Selected resonant frequency.

The PR regulator is equivalent to a band pass filter in the frequency domain. The signal of the selected frequency will be increased, and the signal in the non-selected frequency bands will be attenuated.

The PR regulator is also equivalent to the PI regulator with two additional closed loop poles, which are located in the origin of jω-axis. The gain in this frequency will be increased, which is caused by the resonant. The PR regulator is able to follow the AC signal for each frequency without steady-state error.

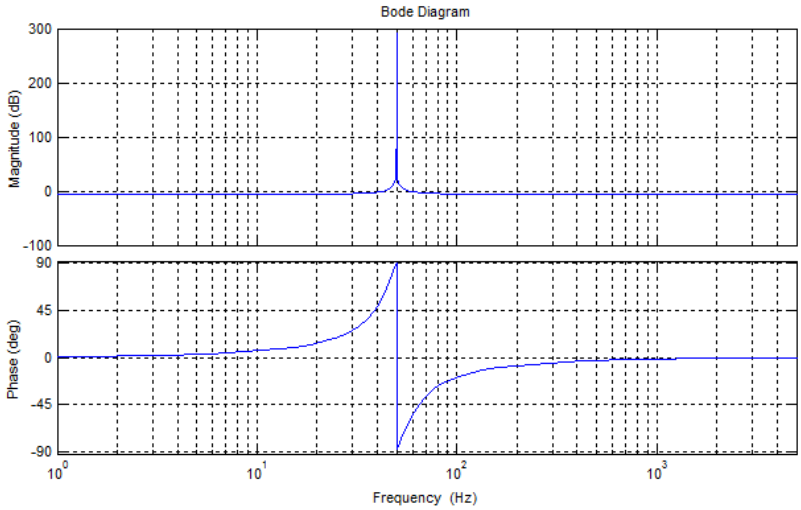



**Figure 5-8; Bode diagram of the PR regulator**

In Figure 5-8 shows the Bode diagram of the PR regulator, where $k_p$ is 0.5, $k_r$ is 40 and$\omega_0$ is 2π50 rad/s. When the s= j$\omega_0$, the gain is infinite. That realizes the tracking of the AC signal without steady-state error.

Because the gain at other frequencies is near to zero, it can only follow the AC signal just in this selected frequency. When the reference voltage from the real-time calculation is not exactly equal to the selected frequency, the gain will be attenuated. In order to meet the requirements of PHIL testing, the quasi Proportional-Resonant regulator is presented:

$$G_{PR}(s) = k_P + \frac{2k_R\omega_C s}{s^2 + 2\omega_C s + \omega_0^2} \qquad \text{Eq. 5-16}$$

$\omega_C$… Cutoff frequency.

In Figure 5-9 shows the Bode diagram of the quasi PR regulator, which $k_p$ is 0.5, $k_r$ is 40, $\omega_C$ is 5 rad/s and $\omega_0$ is 2π50 rad/s for example. There is larger bandwidth near $\omega_0$ and the gain is not infinite, when the s= j$\omega_0$.That enhance the performance of the system.

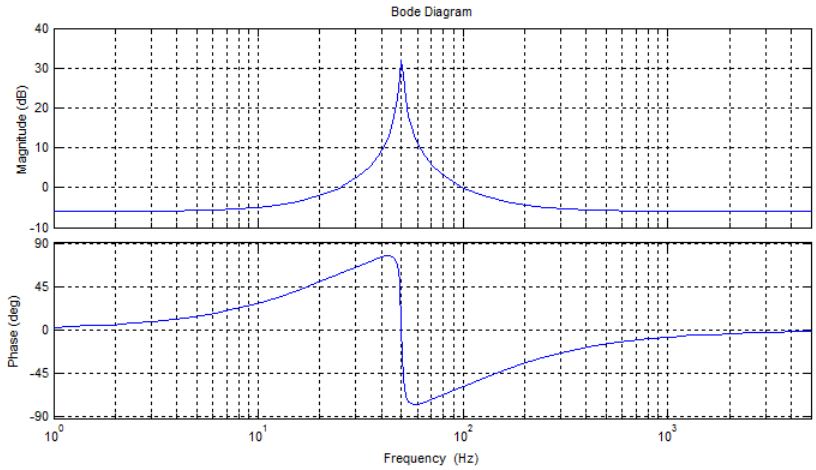



**Figure 5-9; Bode diagram of the quasi PR regulator**

The output frequency of the inverter of the PHIL test system is not only at 50 Hz or 60 Hz, the waveform less than 2000 Hz will also be controlled. In order to control multiple frequencies, the a.m. quasi PR regulator has to be modified. The multiple resonant parts are added in Eq.5-16:

$$G_{PR}(s) = k_P + \frac{2k_{R1}\omega_{C1}s}{s^2 + 2\omega_{C1}s + \omega_{01}^2} + \sum_{h=2}^{n} \frac{2k_{Rh}\omega_{Ch}s}{s^2 + 2\omega_{Ch}s + \omega_{0h}^2} \qquad \text{Eq. 5-17}$$

$\omega_{01}$…Utility frequency;

$\omega_{0h}$…Expected harmonic frequency.

The block diagram of the modified quasi PR regulator is shown in Figure 5-10.

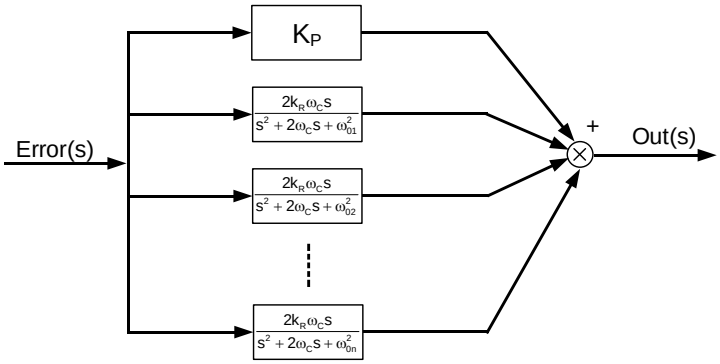



**Figure 5-10; Block diagram of the modified quasi PR regulator**

In Figure 5-11 shows the Bode diagram of the modified quasi PR regulator where the expected utility frequency is 50 Hz, and 7$^{th}$ order harmonic, 15$^{th}$ order harmonic and 25$^{th}$ order harmonics are expected for example, which $k_p$ is 0.5, $k_{r1}$ is 40, $\omega_{C1}$ is 5 rad/s and $\omega_{C0}$ is 1 rad/s. There are large gains in each selected frequency, so the modified quasi PR regulator can follow the AC signal without steady-state error at each expected frequency (fundamental and harmonics).

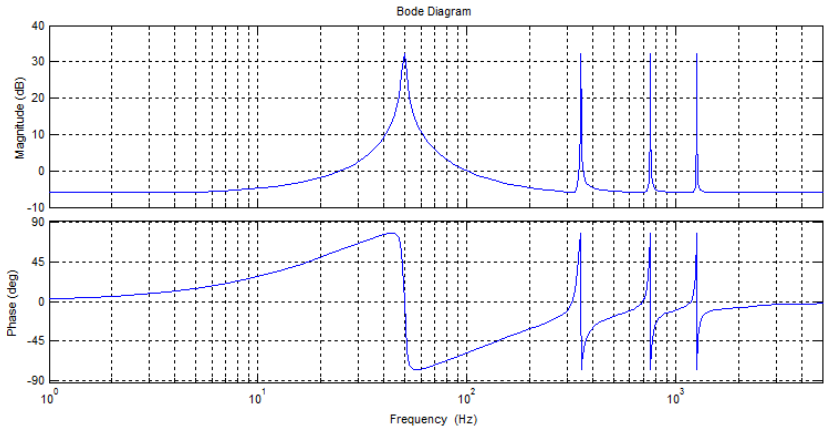



**Figure 5-11; Bode diagram of the modified quasi PR regulator**

In the dual loop control, the voltage outer loop is controlled by the PR regulator so that the output voltage can be well controlled at each frequency (fundamental and harmonics). A Proportional (P) regulator or PR regulator can be applied in the current inner loop. With the PR regulator of the voltage outer loop, they result in a PR-P regulator or PR-PR regulator. Due to the switching frequency of inverter, the inductor current changes fast. Therefore, the P regulator is suitable for this situation, which has also a fast response speed. So the PR-P regulator is applied in this thesis, where the voltage outer loop is controlled by the PR regulator and the current inner loop is controlled by the P regulator.

### 5.3.5 Determination of Regulator Parameters

In the system with dual loop control, the response speed of current inner loop is faster than voltage outer loop, so the determine of regulator parameters should be carried out from inner to outer.

#### 5.3.5.1 Determination of the Regulator Parameters of the Current Inner Loop

The open loop transfer function can be obtained from the Figure 5-7, when it is assumed here that, the influence from the output current can be ignored. The open loop transfer function of the current inner loop with P regulator is presented as:

$$G_{I-OL}(s) = \frac{K_{iP}Cs}{CLs^2 + Crs + 1} \qquad \text{Eq. 5-18}$$

The closed loop transfer function is

$$G_{I-CL}(s) = \frac{K_{iP}Cs}{CLs^2 + (Cr + CK_{iP})s + 1} \qquad \text{Eq. 5-19}$$

$K_{iP}$… Proportional coefficient of the current inner loop.

The operation bandwidth of current inner loop is directly determined the proportional coefficient $K_{iP}$. Considering the requirements of the response speed and operation bandwidth, the cutoff frequency of the inner loop is set to the 1/3 of the equivalent switching frequency, which is 6500 Hz. By inserting this cutoff frequency into Eq.5-20, the proportional coefficient is calculated:

$$\left|G_{I-OL}(j\omega)\right| = \left|\frac{K_{iP}Cj\omega}{CL(j\omega)^2 + Crj\omega + 1}\right|_{\omega=2\pi f_{cut}} = 1 \qquad \text{Eq. 5-20}$$

$f_{cut}$… Cutoff frequency of the inner loop.

According to the parameters of the filter in chapter 5.2.2, when the filter inductance is 0.14 mH, the filter capacitance is 30 µF and the equivalent resistance is set to 0.1 Ω with the

engineering experience. The proportional coefficient of current inner loop $K_{iP}$ is 4.9 according to the Eq.5-20.

There is delay in this system caused by the digital control. The delay transfer function is presented as:

$$G_d(s) = e^{-st_d} \qquad \text{Eq. 5-21}$$

The gain of this delay is 1, so the gain of the system will be not affected, but it will cause a phase shift of the system. When there is no delay in the system, the proportional coefficient of current inner loop $K_{iP}$ does not influence the stability of the system, and the closed-loop poles of the system located in the left half plane. When there is delay in the system, the delay can bring one additional pole and one additional, and the closed-loop poles maybe relocated in the right left half plane, then the system may not be stable. Therefore, the pole-zero diagram is used to judge whether this system is stable or not. Figure 5-12 is the pole-zero diagram of the current inner loop, which the system delay td is 100 µs.

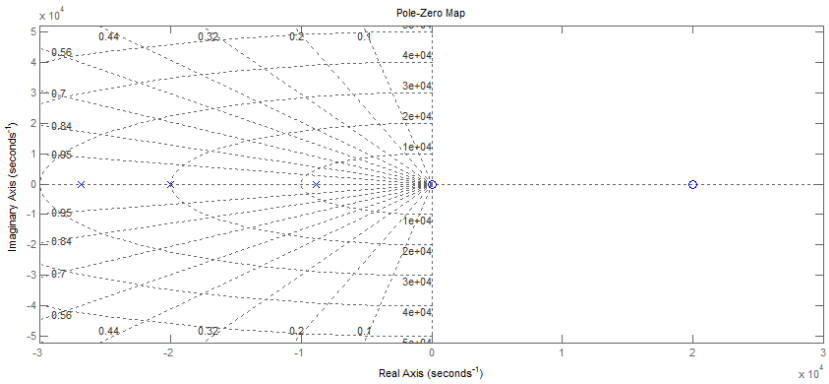



**Figure 5-12; Pole-zero diagram of the current inner loop with $t_d$ is100 µs (x is pole, o is zero)**

This is shown in Figure 5-12, all of the three closed-loop poles are located in the left half plane, so this system is stable with this proportional coefficient.

### 5.3.5.2 Determination of the Regulator Parameters of the Voltage Outer Loop

The PR regulator of the voltage outer loop contains three parts, a proportional regulator, a resonant regulator for the utility frequency and a set of resonant regulators for each harmonics, as shown in Eq.5-17 and Figure 5-10.

The regulator parameter of the P regulator is determined first. The open loop transfer function can be obtained from the Figure 5-7. The same the assumptions which the influence from the output current can be ignored. The open loop transfer function of the PR regulator of the voltage outer loop with a P regulator in the inner loop is presented as:

$$G_{U-OL}(s) = \frac{K_{iP}G_u(s)}{CLs^2 + (Cr + CK_{iP})s + 1} \qquad \text{Eq. 5-22}$$

With the same analyzing method as in chapter 5.2.5.1, the proportional coefficient $K_{uP}$ is be determined. Considering that, the response speed of outer loop is slower than the inner loop, the cutoff frequency of the outer loop is set to the 4500 Hz, and the proportional coefficient $K_{uP}$ is 1.

The pole-zero diagram of the voltage outer loop with 100 µs calculation time is shown in Figure 5-13.

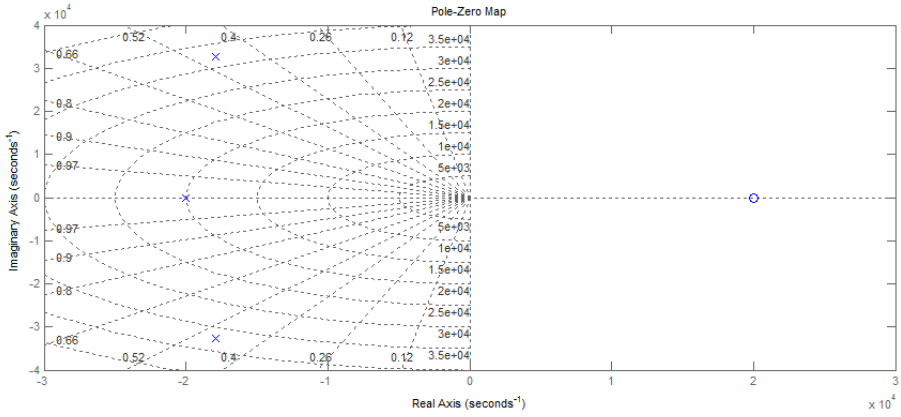



**Figure 5-13; Pole-zero diagram of the voltage outer loop with $t_d$ is100 µs (x is pole, o is zero)**

As shown in Figure 5-13: all of the three closed-loop poles are located in the left half plane, so this system is stable with this proportional coefficient.

After the determination the proportional coefficient, the design of the resonant regulators can be carried out. The transfer function of the resonant regulator for utility frequency is:

$$G_{PR1}(s) = k_{uP} + \frac{2k_{R1}\omega_{C1}s}{s^2 + 2\omega_{C1}s + \omega_{01}^2} \qquad \text{Eq. 5-23}$$

The operation bandwidth of this regulator is presented as:

$$f_{Band} = \frac{\omega_C}{\pi} \qquad \text{Eq. 5-24}$$

Considering the usual frequency deviation, the operation bandwidth is set to 4 Hz. For example, when the given utility frequency is 50 Hz, the reference signal with 48 Hz to 52 Hz, which is according to the Chinese standards, can be effectively controlled. The operation bandwidth of resonant regulators for each harmonics is set to 1 Hz.

Figure 5-14 shows the Bode diagram of the PR regulator, whose the selected frequency is 350 Hz, $k_{Rh}$ is 10 (blue curve), 20(green curve) and 40(red curve). The regulator with the

largest resonant coefficient has the largest gain in selected frequency, that means the regulator with $k_{Rh}$ is 40 has the smallest steady-state error.

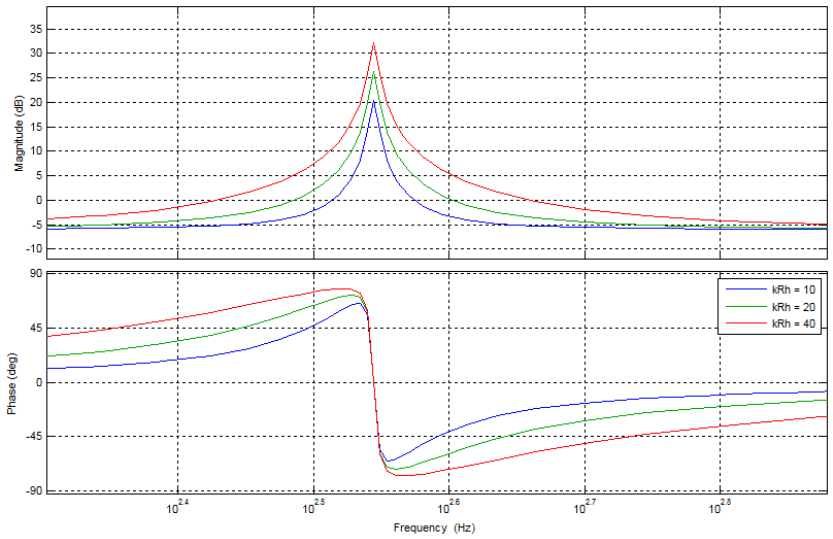



**Figure 5-14; Bode diagram of the quasi PR regulator with different $k_{Rh}$**

In consideration of both the accuracy and stable performance, the resonant coefficient of utility frequency $k_{R1}$ is set to 40 and the resonant coefficient of harmonics $k_{Rh}$ is set to 40.

In summary, the control of the inverter of the power amplifier in PHIL test system is a PR-P regulator, where the voltage outer loop is a proportional-resonant regulator and the current inner loop is a proportional regulator. The regulator parameters are shown in Table 5-2.

| Parameter Name | Value |
|---|---|
| $K_{uP}$ | 1 |
| $K_{R1}$ | 40 |
| $\omega_{C1}$ | 4π rad/s |
| $K_{Rh}$ | 40 |
| $\omega_{Ch}$ | π rad/s |
| $K_{iP}$ | 4.9 |

**Table 5-2; Regulator parameters**

### 5.3.6 Realization of the Proportional-Resonant Regulator in Digital Control

For the realization of the PR regulator in the real-time simulator of PHIL test system, the discretization is required. The transfer function of the resonant regulator is:

$$G_R(s) = \frac{2k_R\omega_C s}{s^2 + 2\omega_C s + \omega_0^2} \qquad \text{Eq. 5-25}$$

The pole–zero mapping method [88] is applied, the Z-domain transfer function of the resonant regulator is presented as:

$$G_R(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \qquad \text{Eq. 5-26}$$

The calculation process of the resonant regulator is shown in Figure 5-15, where the e(k) is the input error signal and the u(k) is the output signal.

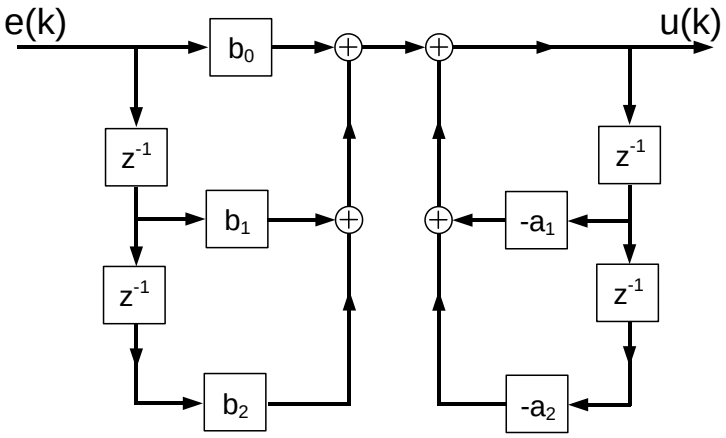



**Figure 5-15; Calculation process of the resonant regulator with pole–zero mapping method**

In such a high calculation step (100 μs), due to the limitations of the length in bytes and the truncation error in the real-time simulator, this discretization may deteriorate the performance of the PR regulator. So the delta operator [89] is applied. The transformation equation from the Z operator to delta operator is presented in Eq.5-27 and the block diagram is shown in Figure 5-16.

$$\delta^{-1} = \frac{\Delta z^{-1}}{1 - z^{-1}} \qquad \text{Eq. 5-27}$$

$\delta^{-1}$… Delta operator;

$\Delta$… Calculation step.

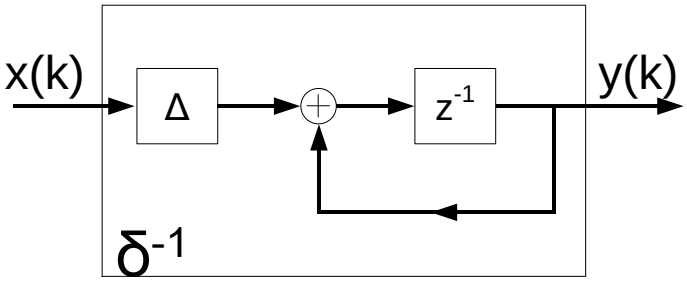



**Figure 5-16; Block diagram of the delta operator $\delta^{-1}$**

By inserting the Eq.5-27 in to Eq.5-26:

$$G_R(\delta) = \frac{\beta_0 + \beta_1 \delta^{-1} + \beta_2 \delta^{-2}}{\alpha_0 + \alpha_1 \delta^{-1} + \alpha_2 \delta^{-2}} \qquad \text{Eq. 5-28}$$

The relationship between the parameters is:

$$\begin{cases} \beta_0 = b_0 \\ \beta_1 = \dfrac{2b_0 + b_1}{\Delta} \\ \beta_2 = \dfrac{b_0 + b_1 + b_2}{\Delta^2} \end{cases}$$ Eq. 5-29

$$\begin{cases} \alpha_0 = 1 \\ \alpha_1 = \dfrac{2 + a_1}{\Delta} \\ \alpha_2 = \dfrac{1 + a_1 + a_2}{\Delta^2} \end{cases}$$ Eq. 5-30

Then, the calculation process of the resonant regulator is shown in Figure 5-17.

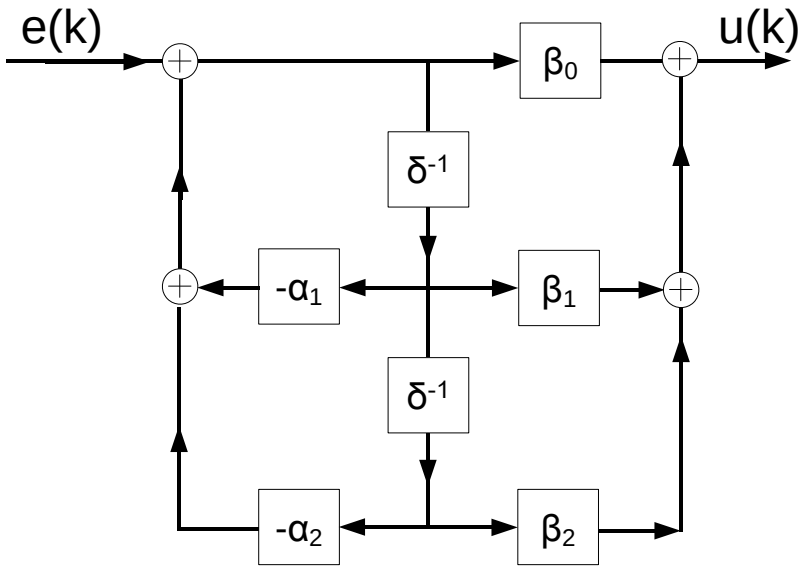



**Figure 5-17; Calculation process of the resonant regulator with delta operator**

## 5.4 Validation of the Power Amplifier by Simulation

In order to verify the design of the hardware and the control strategy in this chapter, a 800 kVA power amplifier is modeled and simulated in Matlab/Simulink. The regulator parameters are shown in Table 5-2 and hardware parameters are shown in Table 5-3.

| Parameter Name | Value |
|---|---|
| Switching frequency | 10 kHz |
| Filter capacitance | 30 μF |
| Filter inductance | 0.14 mH |
| DC bus voltage | 540 V |
| Output power | 800 kVA |

**Table 5-3; Hardware parameters of the inverter**

The output voltage of a single phase is set to 230 $V_{RMS}$ and the fundamental frequency to 50 Hz. The expected harmonics are set to 3rd, 5th and 7th. The voltage dip occurs at 0.205 s, the residual voltage is 0.33 p.u. The simulation result is shown in Figure 5-18.

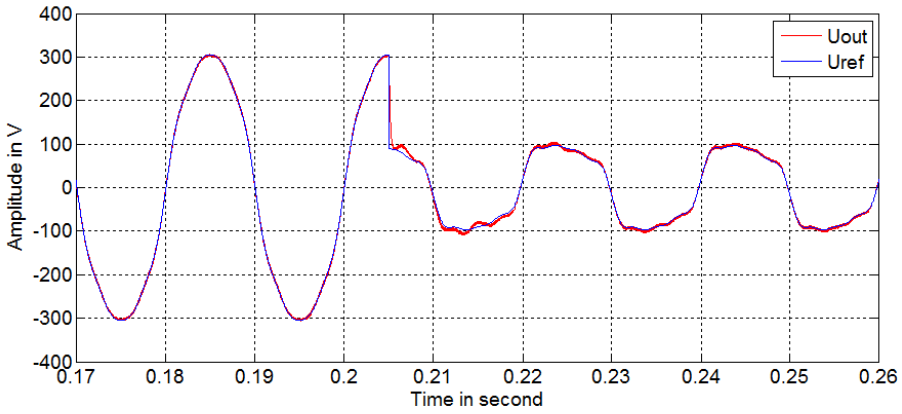



**Figure 5-18; Simulation result of the output voltage with 3rd, 5th and 7th harmonics**

In Figure 5-18, the blue curve presents the reference signal, the red curve is the output voltage waveform. When the voltage dip occurs, the output voltage follows the reference signal.

The expected harmonics are now set to 23th, 25th and 27th. The voltage dip occurs at 0.205 s, the residual voltage is 0.33 p.u again, the simulation result is shown in Figure 5-19.

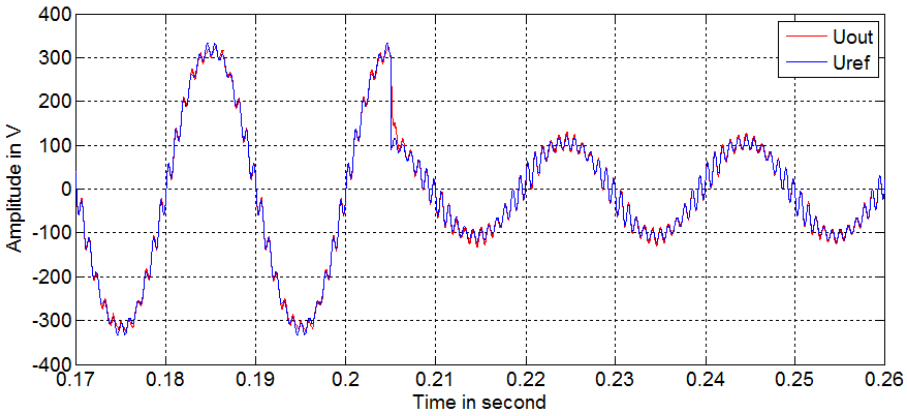



**Figure 5-19; Simulation result of the output voltage with 23th, 25th and 27th harmonics**

In Figure 5-19, the inverter has also good tracking performance with 23th, 25th and 27th harmonics. The related voltage error of this simulation is smaller than 0.3% in 50 Hz and less than 3% in each harmonics.

The experiments of the actual power amplifier are carried out in chapter 6.1.

## 5.5 Summary of this Chapter

This chapter presents a universal requirement analyzing method of the power amplifier based on the requirements of the PHIL testing and related testing standards. The detailed

requirements of the power amplifier are given, it should be able to produce the voltage in healthy power systems and abnormal situations such as frequency deviations, unbalance voltage, harmonics and voltage dips. The response time should be 100 µs.

The topology and the parameters of the power amplifier hardware are designed and determined according to the requirements. Three sets of independent single-phase inverters are used to produce unbalanced voltage. The four-quadrant rectifier is used to transfer the power from the DG system to the external power source.

In order to meet the requirements of the accuracy, response speed and the operation band width, the PR-P regulator is presented, where the voltage outer loop is controlled by the PR regulator and the current inner loop is controlled by the P regulator. The regulator parameters are determined.

Through simulation of the 800 kVA power amplifier, the effectiveness of the presented hardware and control strategy are verified. The simulation test of the different harmonics and voltage dips is carried out. The simulation results fit the theoretical analysis, which verifies the rationality of the theoretical analysis.

# 6 Realization and Experiments

## 6.1 Power Amplifier

### 6.1.1 Realization of the Power Amplifier

An 800 kVA power amplifier of the PHIL test system is build based on the design in chapter 5. The rectifier unit contains of two sets of parallel connected three-phase four-quadrant rectifiers. The inverter unit contains of three sets of independent single-phase inverters. The photos of the power amplifier are shown in Figure 6-1 and Figure 6-2.

**Figure 6-1; Front of the power amplifier**

Figure 6-1 shows the front side of the power amplifier, it contains eight cabinets. From left to right are: switchgear cabinet, rectifier cabinet 1 & 2, inverter cabinet 1, 2, 3 and the controller cabinet. In Figure 6-2 shows the back side of the power amplifier without the cover plates.

**Figure 6-2; Back of the power amplifier (Remove cover plates)**

The control of the inverter is carried out in the real-time simulator (dSpace), the control block diagram is shown in Figure 6-3. When the calculation step is 100 µs, the average running time of one period of this controller is 2µs.

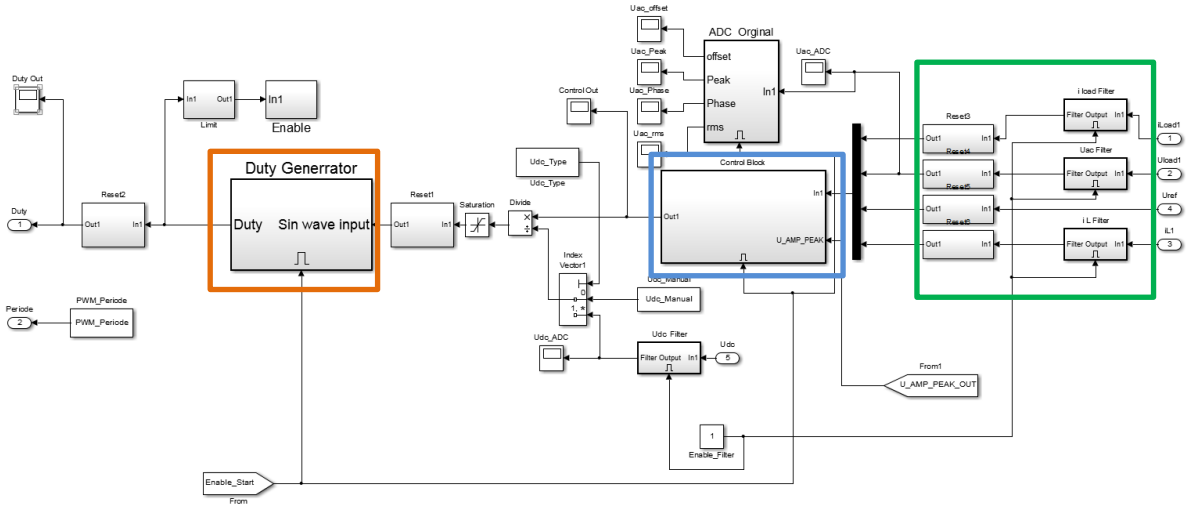



**Figure 6-3; Control block diagram in dSpace**

In Figure 6-3, the orange box is the duty cycle generator for PWM. The blue box is the PR-P regulator. The green box is the digital filter. The user interface of the power amplifier is shown in the Figure 6-4.

**Figure 6-4; User interface of the power amplifier**

## 6.1.2 Experiments of the Power Amplifier

In order to verify the topology of hardware and the PR-P regulator, the experiments of the power amplifier will be carried out. The following experiments are all with a three-phase 100 kW resistive load.

### 6.1.2.1 Steady Performance Experiments

The influence of proportional coefficient of the current inner loop $K_{iP}$, which is mentioned in chapter 5.3.5.1, is analyzed in the experiment. The reference voltage is set to 220 $V_{RMS}$,

frequency is set to 50 Hz. The proportional coefficient in Figure 6-5 is 1.56, which the expected cutoff frequency of the inner loop is 3500 Hz. When the expected cutoff frequency of the inner loop is 6500 Hz, the proportional coefficient $K_{ip}$ is 4.9 as the calculation result in chapter 5.3.5.1, the output voltage is shown in Figure 6-6.

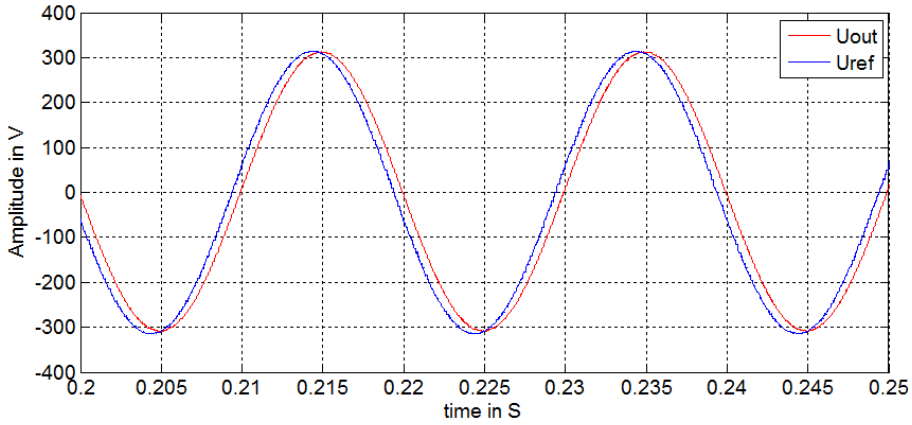



**Figure 6-5; Output vs. reference voltage in 50 Hz, $K_{iP}$ = 0.126**

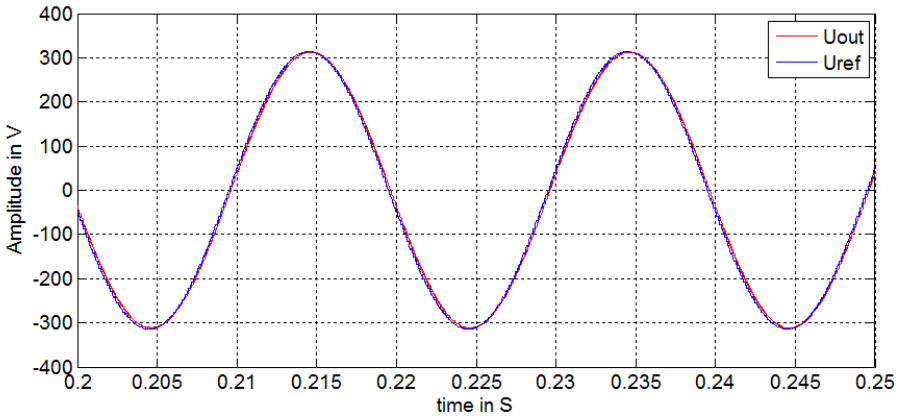



**Figure 6-6; Output vs. reference voltage in 50 Hz, $K_{iP}$ = 4.9**

It can be seen from the Figure 6-5 and Figure 6-6 that, the waveform quality of the both output voltages is good. The Total Harmonic Distortion (THD) value less than 5000 Hz of the output voltages are both around 0.5%, as shown in Figure 6-8. But there is a significant phase shift between the reference (blue curve) and output voltage (red curve) in Figure 6-5 with phase shift of 9°. This shows the output voltage cannot well follow the reference, when $K_{iP}$ = 1.56. The phase shift in Figure 6-6 is 1.8° (100µs), which is just the calculation step of the real-time simulator. This shows the response speed becomes faster when $K_{iP}$ = 4.9. Therefore, the proportional coefficient of the current inner loop will strongly affect the response speed of the inverter. The Figure 6-7 shows the screenshot of the oscilloscope, which the green curve is the reference signal and the yellow curve presents the output voltage.

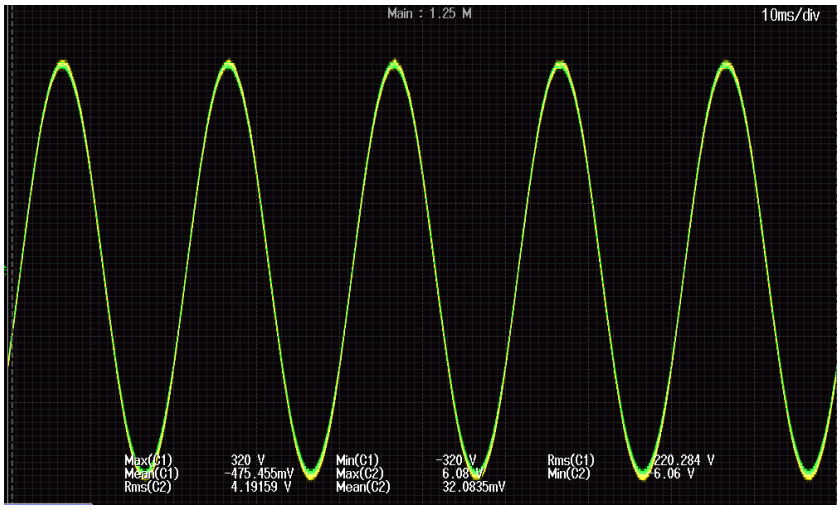



**Figure 6-7; Output vs. reference voltage in 50 Hz, $K_{iP}$ = 4.9, screenshot of oscilloscope**


**Figure 6-8; THD of the output voltage in 50 Hz, $K_{iP}$ = 4.9, screenshot of power analyzer**

In order to verify the output ability of the voltage unbalance, the power amplifier will produce the balanced three-phase voltage (Figure 6-9) and an unbalanced three-phase voltage (Figure 6-10).

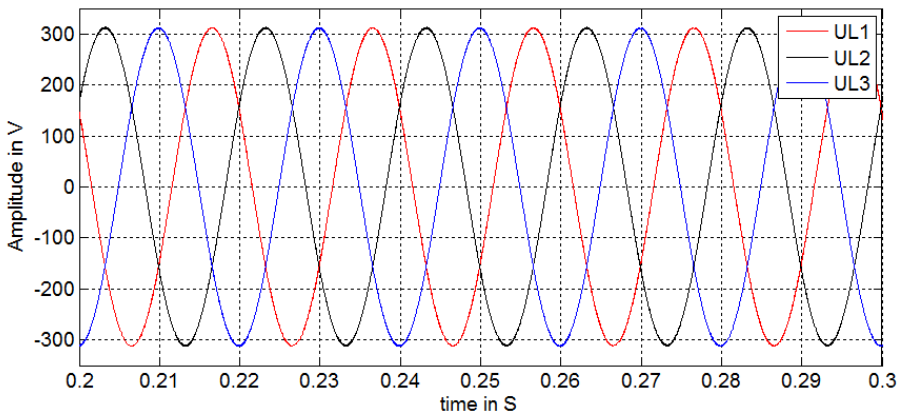



**Figure 6-9; Balanced three-phase voltage**

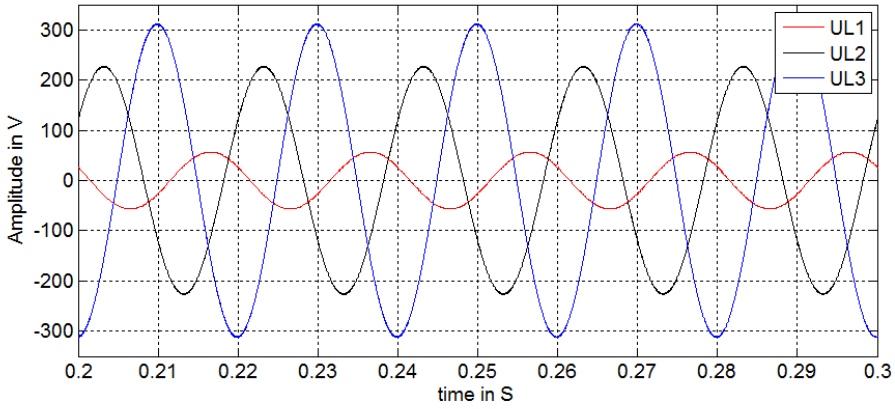



**Figure 6-10; Unbalanced three-phase voltage**

This is shown in Figure 6-10: the voltages of three phases are respectively set to 40 $V_{RMS}$, 160 $V_{RMS}$ and 220 $V_{RMS}$. The test result shows that, this power amplifier can produce a voltage unbalance.

One of the advantages of the PR-P regulator is the precise control of the each selected frequency. In order to observe the influence of resonant coefficient of voltage outer loop, which is mentioned in chapter 5.3.5.2, an experiment of producing harmonics is carried out. The voltage in 50 Hz is set to 220 $V_{RMS}$, the expected harmonics will be 3$^{rd}$, 5$^{th}$ and 7$^{th}$ with an amplitude of 30 V per harmonic. The resonant coefficients of the harmonics $K_{Rh}$ will be set to 10 (Figure 6-11), 20 (Figure 6-12) and 40 (Figure 6-13).

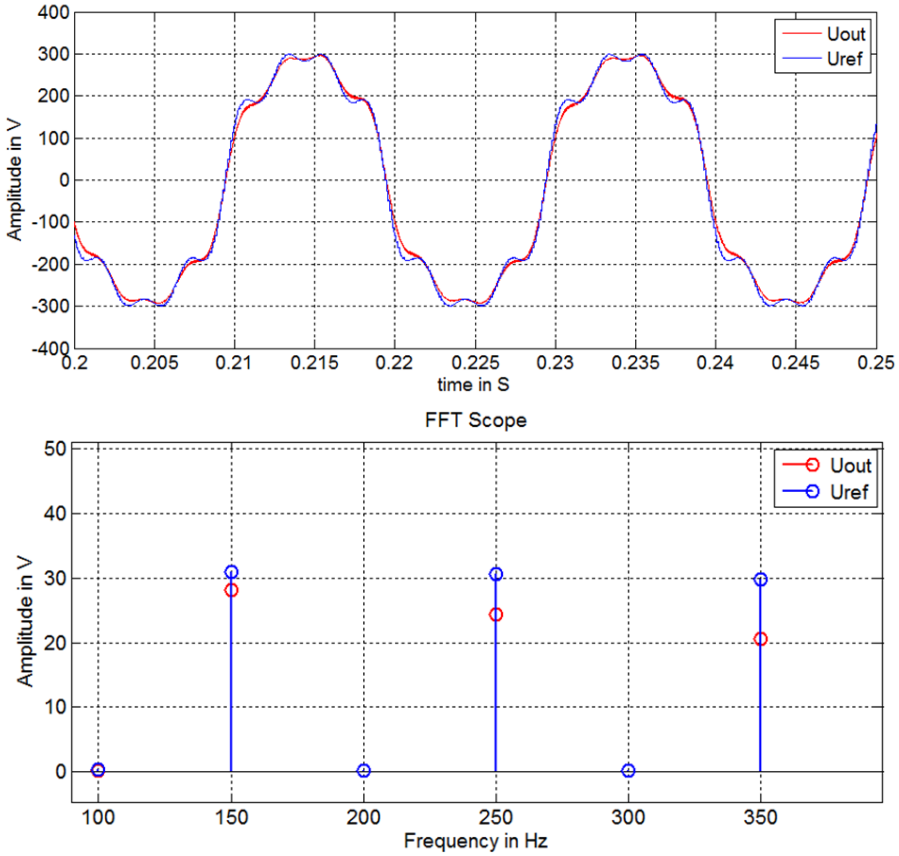



**Figure 6-11; Output voltage vs. reference (Up: waveform; Down: Amplitude spectrum), $K_{Rh}$=10**

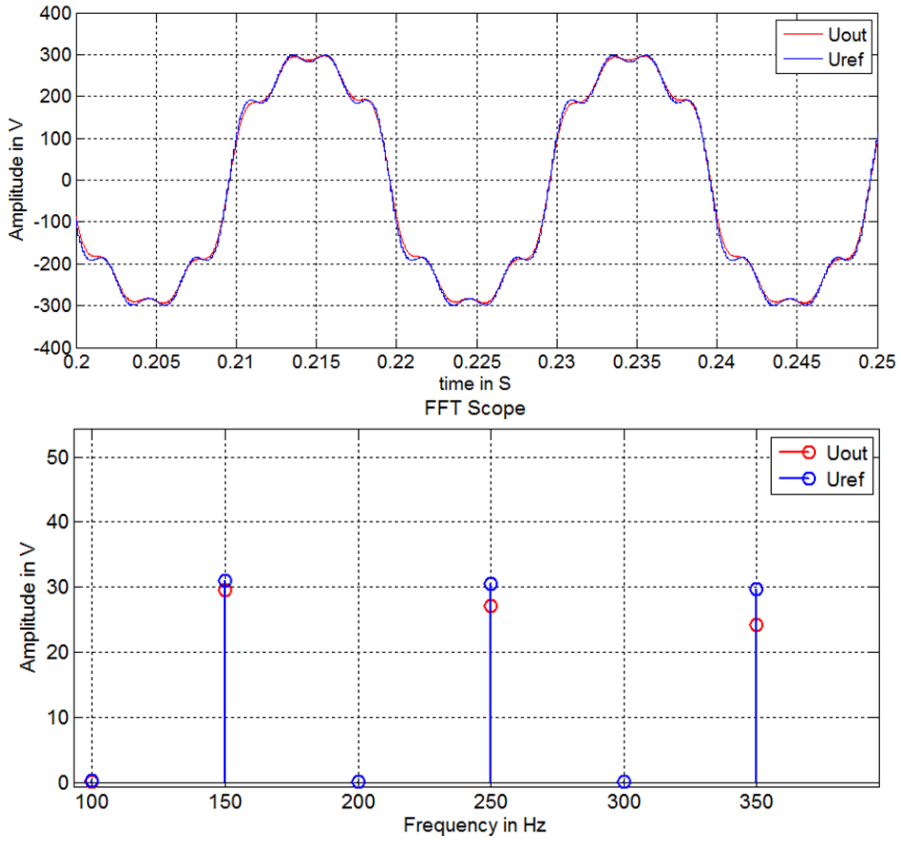



**Figure 6-12; Output voltage vs. reference (Up: waveform; Down: Amplitude spectrum), $K_{Rh}$=20**

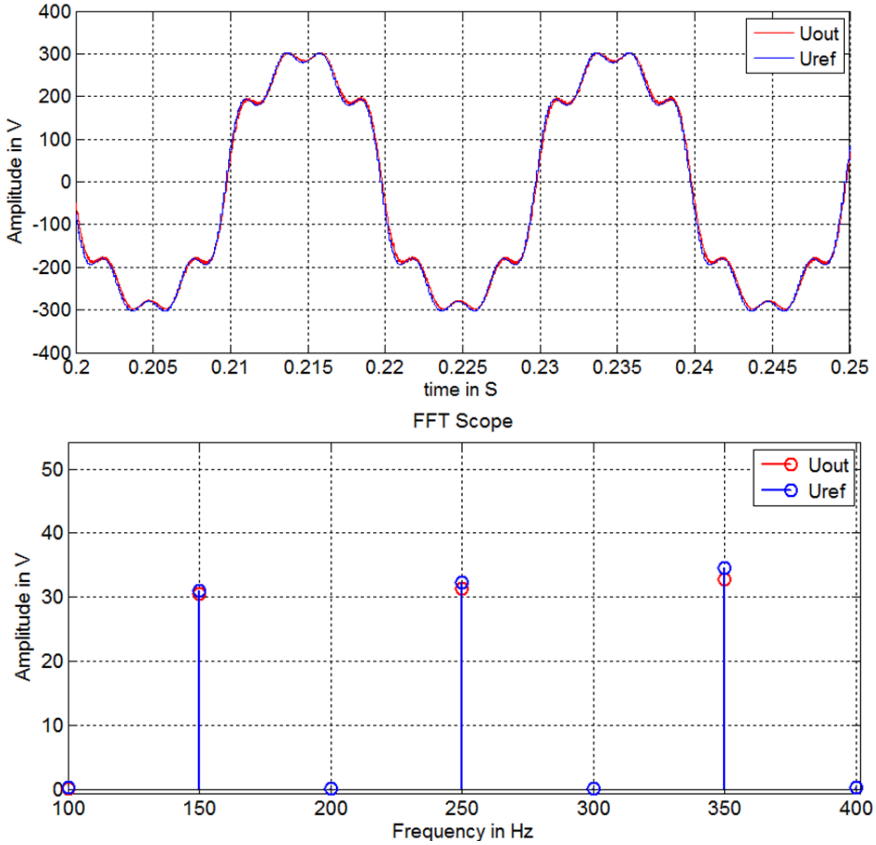



**Figure 6-13; Output voltage vs. reference (Up: waveform; Down: Amplitude spectrum), $K_{Rh}$=40**

As shown in Figure 6-11, Figure 6-12 and Figure 6-13, the resonant coefficient $K_{Rh}$ affects the steady-state error of the harmonics. When the resonant coefficient for harmonics is 10 (Figure 6-11), the gain in selected frequency is the smallest as already shown in Figure 5-14, then it has the largest steady-state error in selected frequency. In Figure 6-13, the largest resonant coefficient has the smallest steady-state error in selected frequency. The theoretical analysis in chapter 5.3.5.2 is verified.

Figure 6-14 shows the output voltage with the $k_{Rh}$=40, when the reference voltage (50 Hz) is set to 220 $V_{RMS}$, the expected harmonics will be 15$^{th}$, 17$^{th}$ and 19$^{th}$ with the amplitude is 30 V, 35V and 20V. This shows that, the steady-state error around 1000 Hz is also very small.

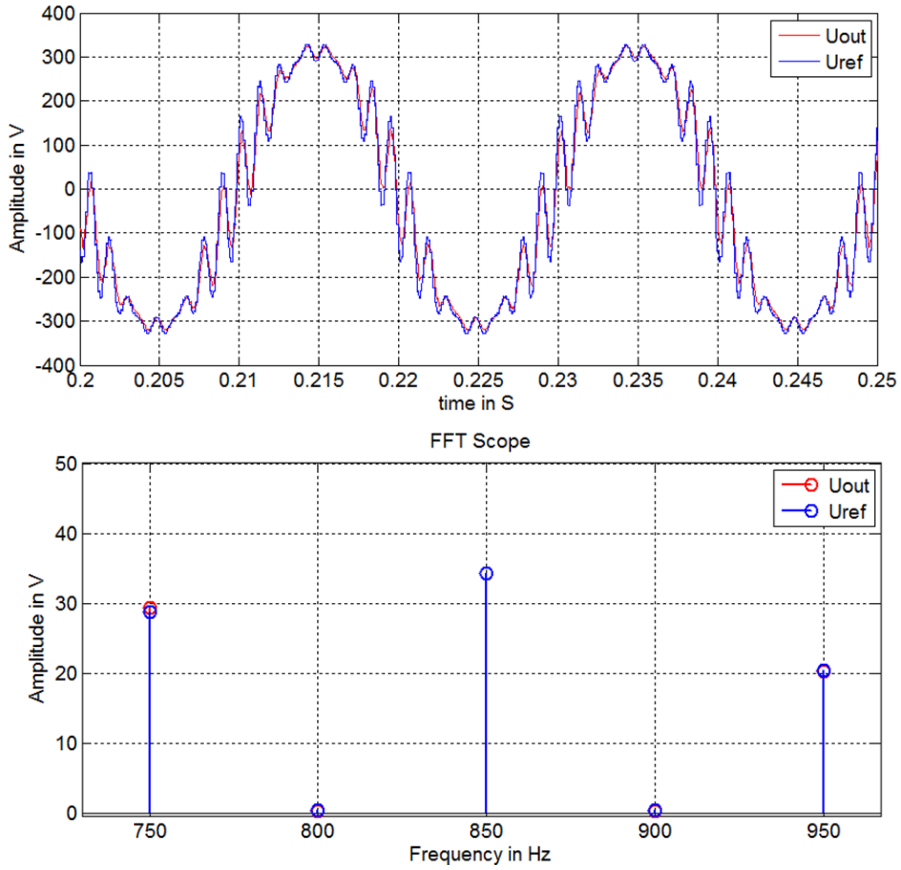



**Figure 6-14; Output voltage vs. reference with 15$^{th}$, 17$^{th}$ and 19$^{th}$ harmonics (Up: waveform; Down: Amplitude spectrum),**

In Figure 6-15, Figure 6-16 and Figure 6-17 show the output voltage with the $k_{Rh}$=40, when the expected harmonics will be 30$^{th}$, 35$^{th}$ and 40$^{th}$ and an amplitude for each harmonic is 16 V. These figures show the power amplifier can well follow the reference signal until frequencies up to 2000 Hz.

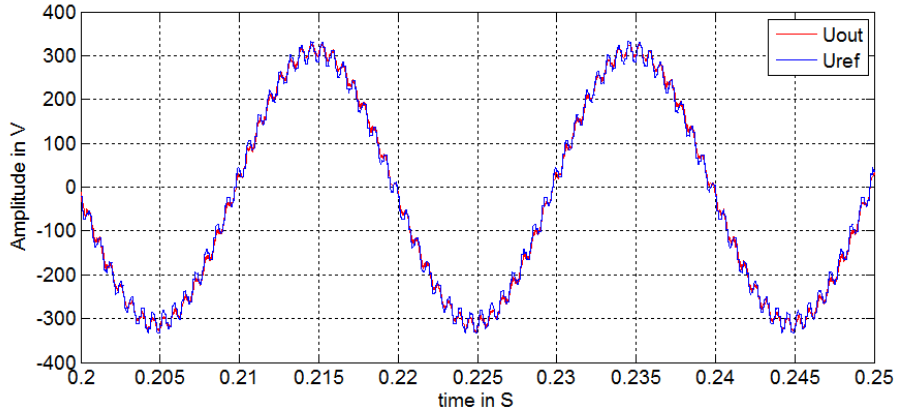



**Figure 6-15; Output voltage vs. reference with 30th harmonics**

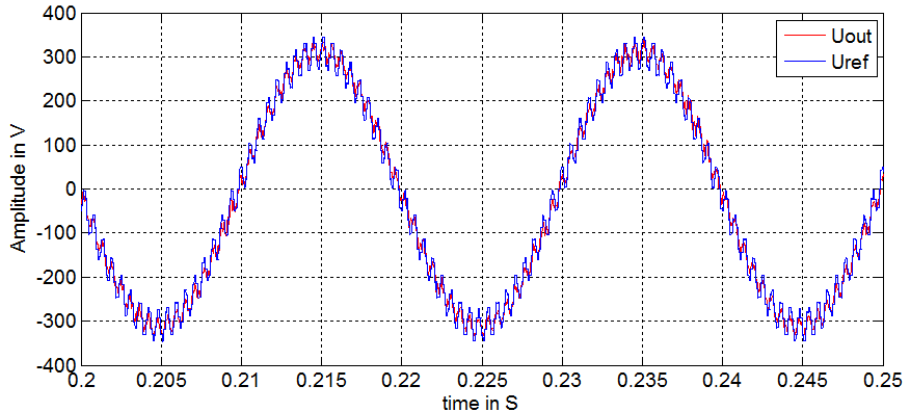



**Figure 6-16; Output voltage vs. reference with 35th harmonics**

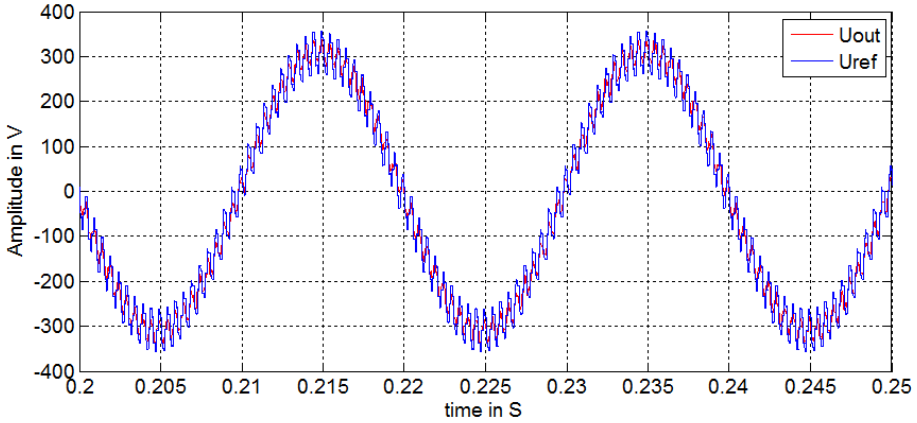



**Figure 6-17; Output voltage vs. reference with 40th harmonics**

### 6.1.2.2 Dynamic Performance Experiments

The dynamic response performance of the power amplifier is largely affected by the proportional coefficient of the current inner loop $K_{iP}$. Therefore, the influence of the proportional coefficient $K_{iP}$ to the dynamic performance will be analyzed with the voltage dips experiment. The reference voltage (50 Hz) is set to 220 $V_{RMS}$, voltage dip occur with arbitrary phase, the residual voltage is 55 $V_{RMS}$. In Figure 6-18, Figure 6-19 and Figure 6-20 show the experiments results.

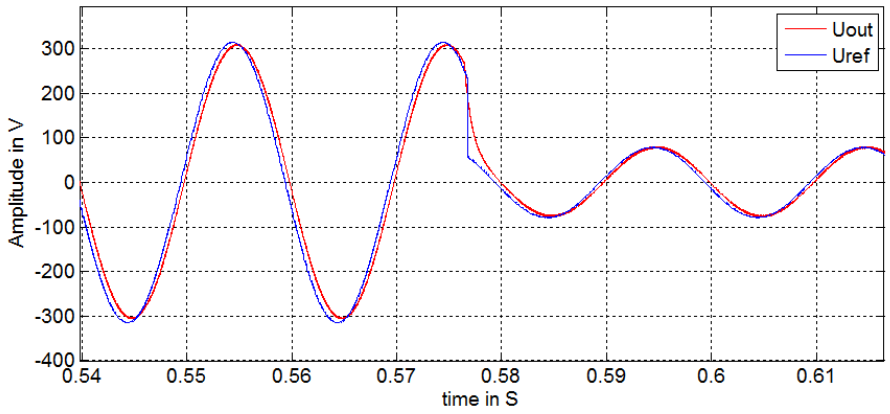



**Figure 6-18; Output voltage vs. reference of voltage dip with $K_{iP}$=0.87**

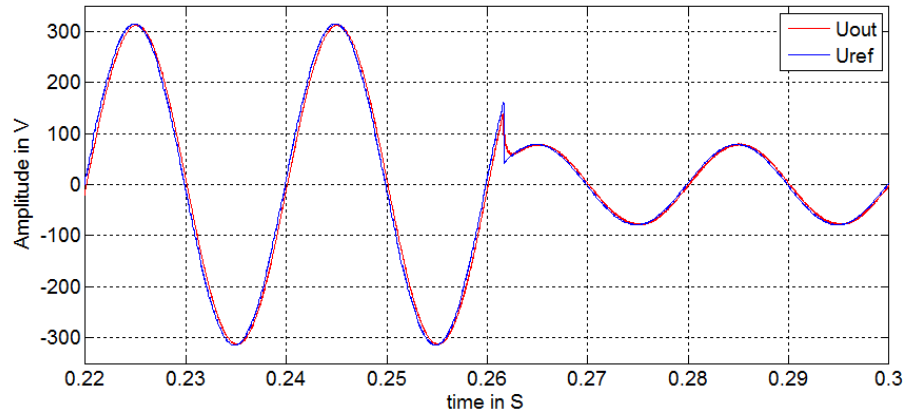



**Figure 6-19; Output voltage vs. reference of voltage dip with $K_{iP}$=4.9**

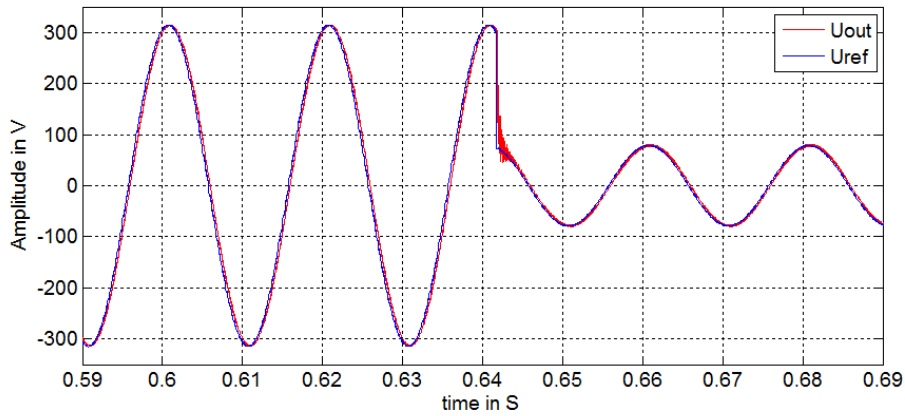



**Figure 6-20; Output voltage vs. reference of voltage dip with $K_{iP}$=8.3**

The $K_{iP}$ is set to 0.87 (Figure 6-18), to 4.9 (Figure 6-19) and to 8.3 (Figure 6-20), and the cutoff frequency of the current inner loop is set to 3000 Hz, 6500 Hz and 10000 Hz, respectively.

It can be seen in Figure 6-18, with the smallest $K_{iP}$, the output voltage waveform slowly goes down, the response speed is the slowest. In Figure 6-20, the output voltage waveform sharply goes down, and even has an unexpected oscillation. The output voltage waveform in Figure 6-19 goes down faster than in Figure 6-18, and there is no unexpected oscillation.

The theoretical analysis in chapter 5.3.5.1 is verified, this proportional coefficient of the current inner loop ($K_{iP}$=4.9) is able to meet the requirements of response speed of power amplifier.

## 6.2 Power Hardware-in-the-Loop Interface Algorithm

### 6.2.1 Set up of the Experiments

Based on the design in chapter 3, a complete PHIL test system has been built. In this chapter, the accuracy and the stable performance of different PHIL interface algorithm is compared. In order to facilitate the system observation and analysis of the results, the characteristic of EUT should be known. A fixed value resistor will be viewed as the EUT of the hardware side, a variable resistor will be viewed as the grid impedance of the software side. The configuration diagram of the PHIL test system is shown in Figure 6-21.

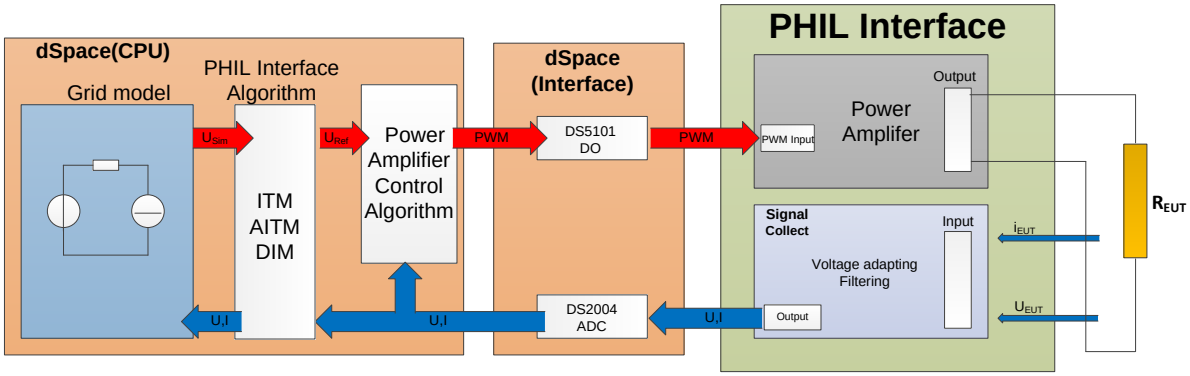



**Figure 6-21; Configuration diagram of the PHIL test system**

This is shown in Figure 6-21, the hardware of the real-time simulator includes a processor board of the type “dSpace DS1006”, several digital waveform output boards of the type “dSpace DS5101” and several A/D boards of the type “dSpace DS2004”. The processor of the dSpace is a quad-core AMD Opteron, on the grid model, the PHIL interface algorithm and the control strategy of the power amplifier are running. The digital waveform output boards are responded to produce the PWM signals to power amplifier. The photo of the real-time simulator is shown in Figure 6-22.

The rated power of the AC power amplifier is 800 kVA, the detailed configuration is already presented in chapter 6.1. The photo of both the AC and DC power amplifier is shown in Figure 6-23. The signal collecting board is responded to convert and filter the signals from voltage and current sensors to the A/D boards of real-time simulator, the photo is shown in Figure 6-24.

**Figure 6-22; Real-time simulator (left) and the Host PC (right)**

**Figure 6-23; DC power amplifier (left) and the AC power amplifier (right)**

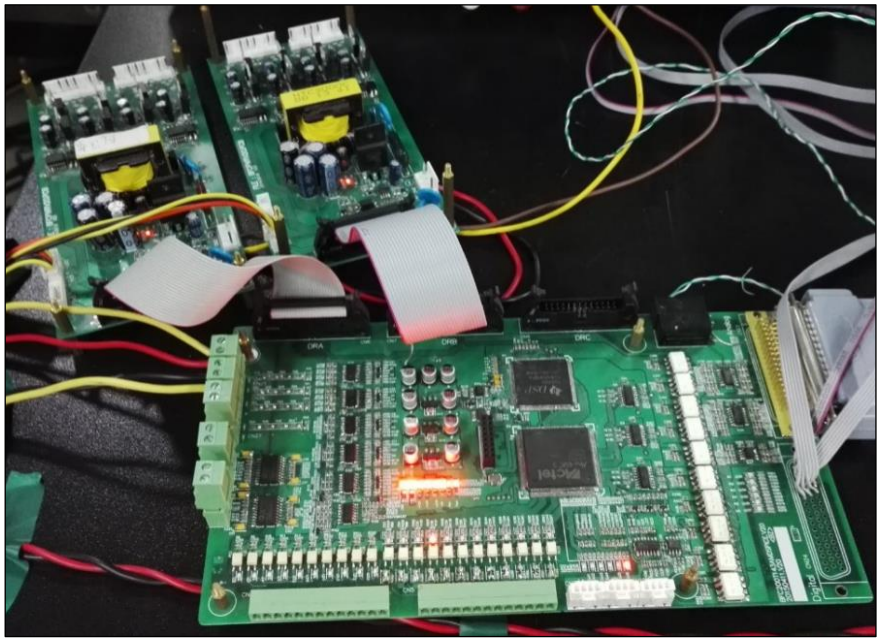


**Figure 6-24; Signal collecting board**

The calculation step of the real-time simulator is 100 µs. The delay times caused by the DS2004 and DS5101 is smaller than 1µs, so these delays will be ignored. Therefore the system delay $t_d$ of this PHIL test system will be considered as 100 µs in the following analysis.

The equivalent circuit of the software side and hardware side is shown in Figure 6-25. $R_{Sim}$ is the variable resistor in software side, the range of this variable resistor is set from 1 Ω to 120 Ω in this experiment. $R_{EUT}$ is the fixed value resistor on the hardware side, whose resistance is 12 Ω. During this experiment, the voltage of the $U_s$ is 100 $V_{RMS}$ in 50 Hz.

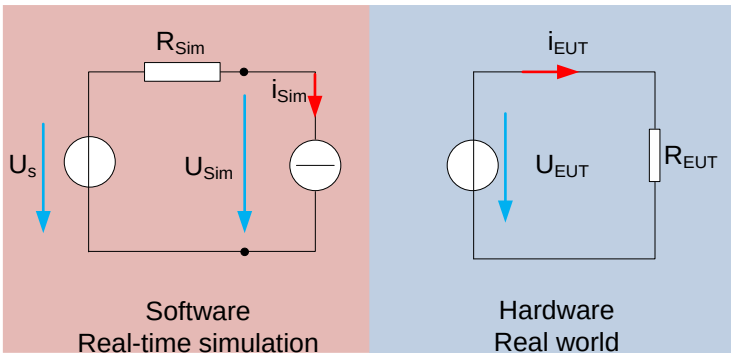



**Figure 6-25; Equivalent circuit of the software side and hardware side**

### 6.2.2 Experiments' Results and Analysis

The experiments for the Ideal Transformer Method and its compensation methods are carried out. The experiments procedures are as follows: In the case of an unchanged impedance on hardware side, the resistance of the software side $R_{Sim}$ is gradually increased, in order to change the ratio of the impedance between the software side and the hardware side. The steady state output voltage amplitude and the phase angle are recorded and compared with the theoretical values. The relative voltage error and the phase error are obtained, as shown in Figure 6-26. The equation of the relative voltage amplitude error $\eta_m$ is presented as:

$$\eta_m = \frac{U_{theoretical} - U_{experiment}}{U_{theoretical}} 100\% \qquad \text{Eq. 6-1}$$

In Figure 6-26, the blue curve represents the ITM, the red curve is the ITM with low pass filter and the green curve is the ITM with phase compensation. The black "X" represents the occurrence of instability, as shown in Figure 6-27.

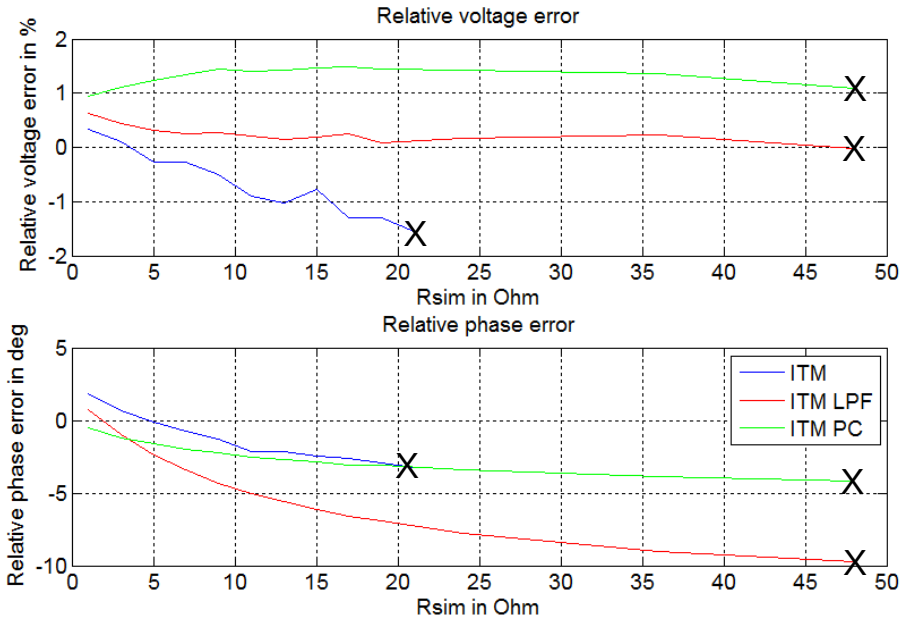



**Figure 6-26; Relative voltage error (Upper Picture) and the phase error (Lower Picture) of ITM and its compensation methods**

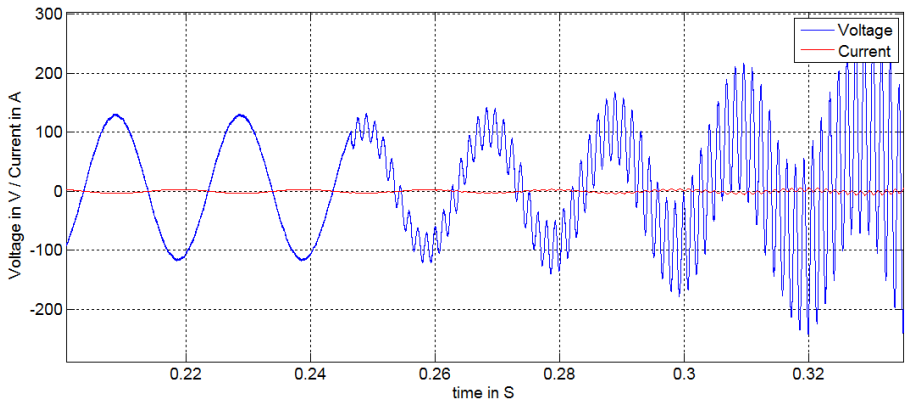



**Figure 6-27; Voltage and current waveform of ITM and $R_{sim}$=21 Ω**

According to the system stability criterion in chapter 3.3.2, the system is unstable, when the impedance on the software side is larger than the hardware side. In Figure 6-26, the system with ITM becomes unstable until the $R_{sim}$ is 21 Ω, which is already larger than the resistance of hardware side $R_{EUT}$. Because the power amplifier has a limitation with operation bandwidth, it can also be regarded as a low pass filter. Therefore the stability range of the $R_{sim}$ increases. The ITM with low pass filter, where cutoff frequency is 1000 Hz, becomes unstable when the $R_{sim}$ is greater than 48 Ω. The ITM with phase compensation becomes also unstable until the $R_{sim}$ is greater than 48 Ω. This proves that both the compensation methods can enhance the stability performance of the system, they increase the stability range of the $R_{sim}$. In real life however, in the parallel grid operation mode, the grid is always “stronger” than a DG system, which means that the internal grid “resistance” is much less than the DG “resistance”.

In Figure 6-26, the relative voltage amplitude error of the ITM with low pass filter is the smallest, but its relative phase error increases with the increase of $R_{sim}$, due to the phase shift effect of the low pass filter, the analysis in chapter 3.3.4.1 is matched.

Figure 6-28 and Figure 6-29 show the dynamic behavior of the ITM and ITM with low pass filter. When the $R_{sim}$ sharply increases, there are undesired oscillations in the output voltage, and then undesired harmonics occurs. During the PHIL testing, the undesired oscillations will reduce the accuracy by ITM or ITM with low pass filter.

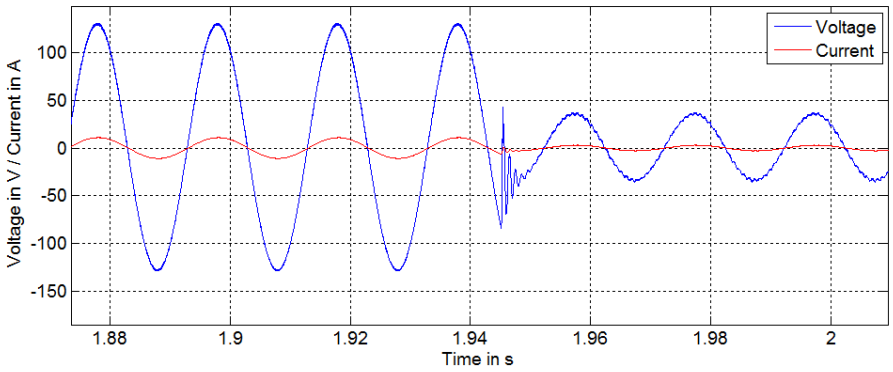



**Figure 6-28; Voltage and current waveform of ITM when $R_{sim}$ sharply increase**

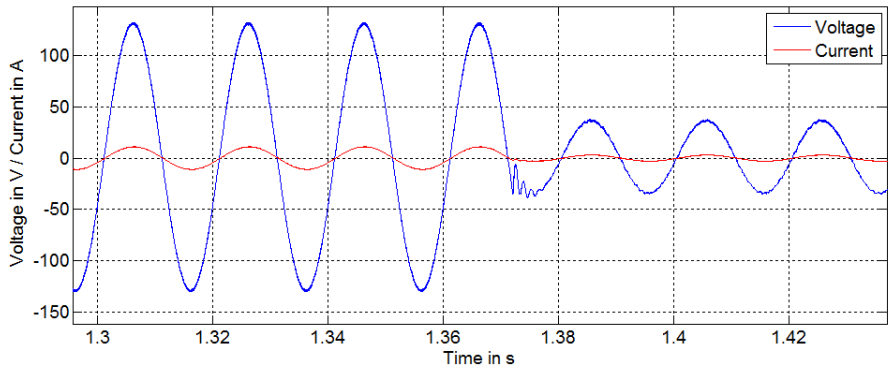



**Figure 6-29; Voltage and current waveform of ITM with low pass filter when $R_{sim}$ sharply increase**

The experiments results of the Advanced ITM and the Damping Impedance Method are shown in Figure 6-30.

In Figure 6-30, the blue curve represents as the ITM, the red curve is the AITM and the green curve represents the DIM. The systems with AITM or DIM are stable until the $R_{sim}$ is 120 Ω, and they will be also stable if $R_{sim}$ is larger than 120 Ω. The relative voltage amplitude error and the phase error of the AITM increase with the increase of $R_{sim}$. These errors are caused by the compensation resistor $R_C$ with pure resistance, when there is circle inductance in hardware side. The relative voltage amplitude error of DIM keeps round 1% with each $R_{sim}$. The relative phase error of DIM is always 1.8° (100 µs), which is the calculation step of the real-time simulator and also the inherent phase shift of the power amplifier.

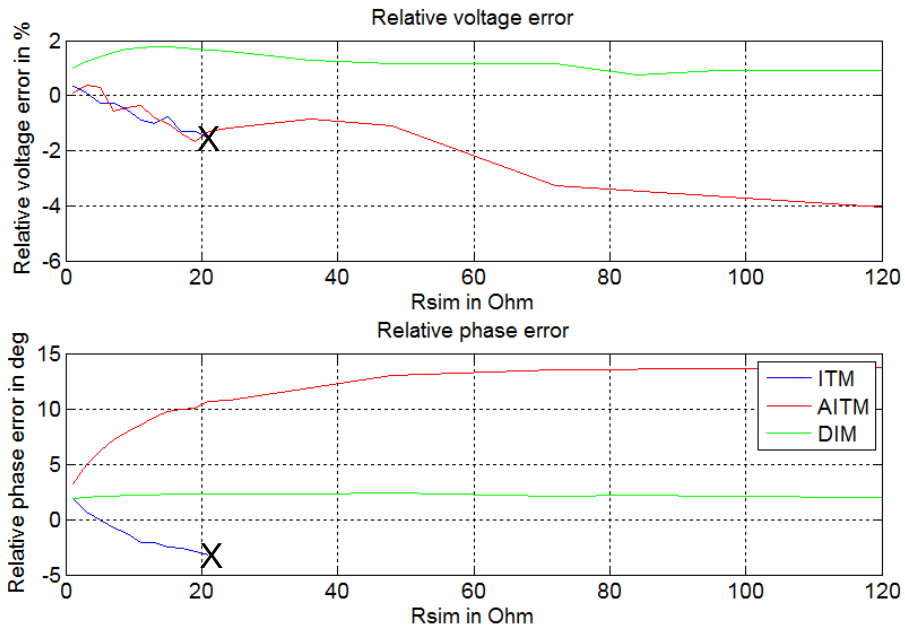



**Figure 6-30; Relative voltage error (Upper Picture) and the phase error (Lower Picture) of ITM, AITM and DIM**

Figure 6-31 and Figure 6-32 show the dynamic behavior of the AITM and DIM. When $R_{sim}$ sharply increases, the output voltage reduced also sharply without undesired oscillations and undesired harmonics. Therefore, the dynamic performance of the AITM and DIM is better than ITM and the ITM with low pass filter.

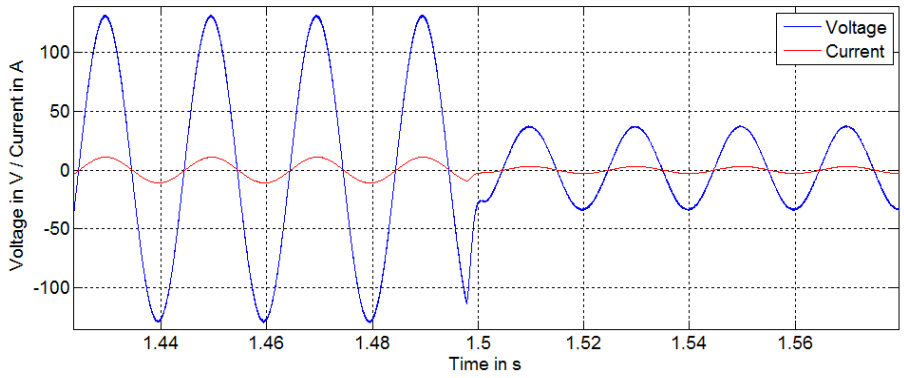



**Figure 6-31; Voltage and current waveform of AITM when $R_{sim}$ sharply increase**

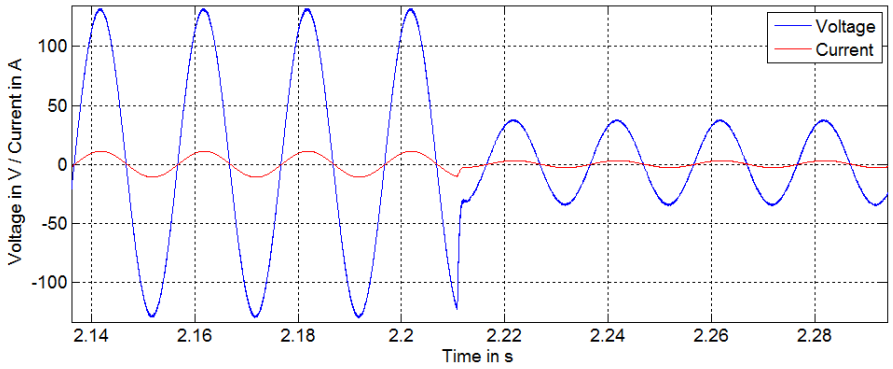



**Figure 6-32; Voltage and current waveform of DIM when $R_{sim}$ sharply increase**

In Figure 6-33 shows the relative voltage error and the phase error of the above PHIL interface algorithms.

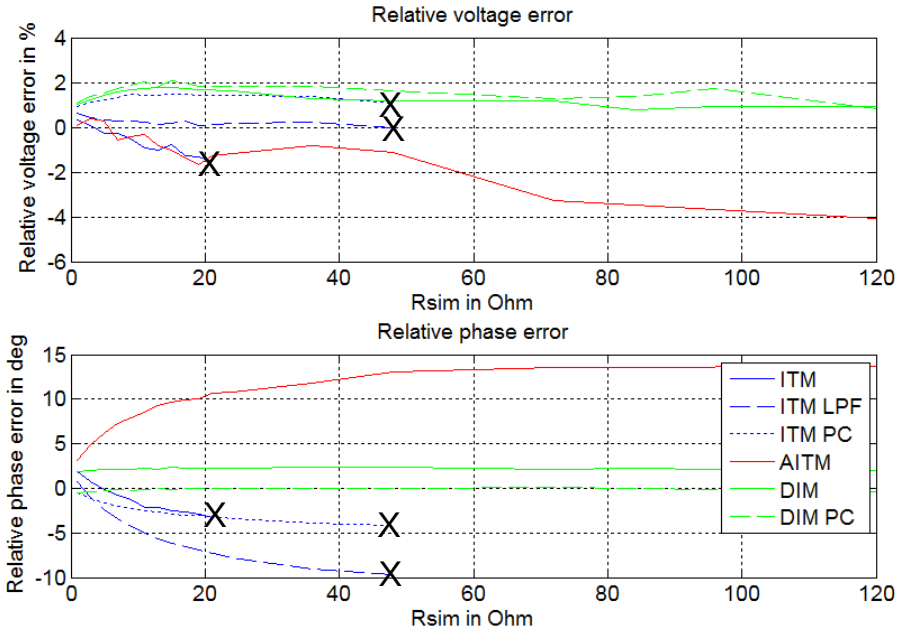



**Figure 6-33; Relative voltage error (Upper Picture) and the phase error (Lower Picture) of different PHIL interfaces**

In Figure 6-33 , the ITM with low pass filter has the smallest relative voltage amplitude error but the largest phase error. The DIM with phase compensation has the smallest relative phase error, which is always 0°. Considering the requirements of accuracy, stability and the dynamic performance, the Damping Impedance Method has the best comprehensive performance, which verifies the analysis in chapter 3.3 and chapter 3.4.

## 6.3 Power Hardware-in-the-Loop testing with Grid-connected Inverters

In order to have a complete verification of the PHIL test system, the experiments of actual photovoltaic grid-connected inverters is carried out in this chapter.

### 6.3.1 Set up of the Experiments

As is shown in Figure 6-34, the complete PHIL test system is established based on the configuration diagram in Figure 6-21. The DC port of the EUT is connected to the DC source, which is the PV simulator. The PV simulator corresponds to simulation the output of the photovoltaic array(s). Base on the grounds of the theoretical analysis in chapter 3 and the experiments results in chapter 6.2, the Damping Impedance Method is applied in the PHIL test system as PHIL interface algorithm.

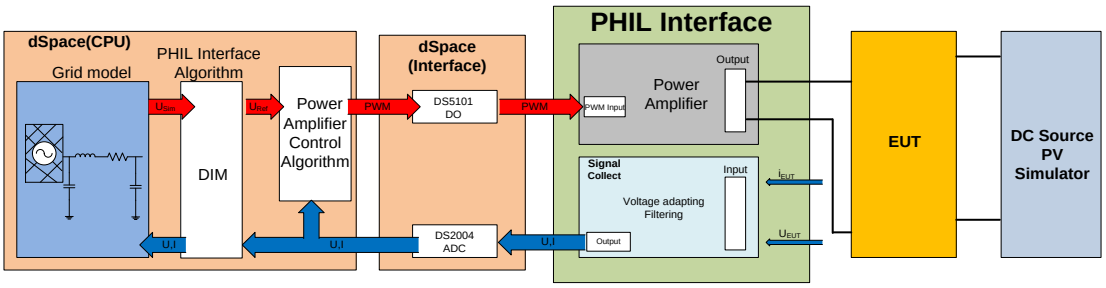



**Figure 6-34; Configuration diagram of the complete PHIL test system**

As EUTs in this chapter, the three different photovoltaic grid-connected inverters from three different producers are used. This is shown in Figure 6-35. The rated power of all these EUT is all 4000 W, and the rated output voltage is 230 $V_{RMS}$. From left to right are the EUT1 (white), EUT2 (red) and EUT3 (yellow).

EUT 1 (White) | EUT 2 (Red) | EUT 3 (Yellow)

**Figure 6-35; Three different photovoltaic grid-connected inverters (EUTs)**

In order to reproduce a residential grid environment, where the photovoltaic grid-connected inverters are used, a grid model is built in dSpace, as shown in Figure 6-36.

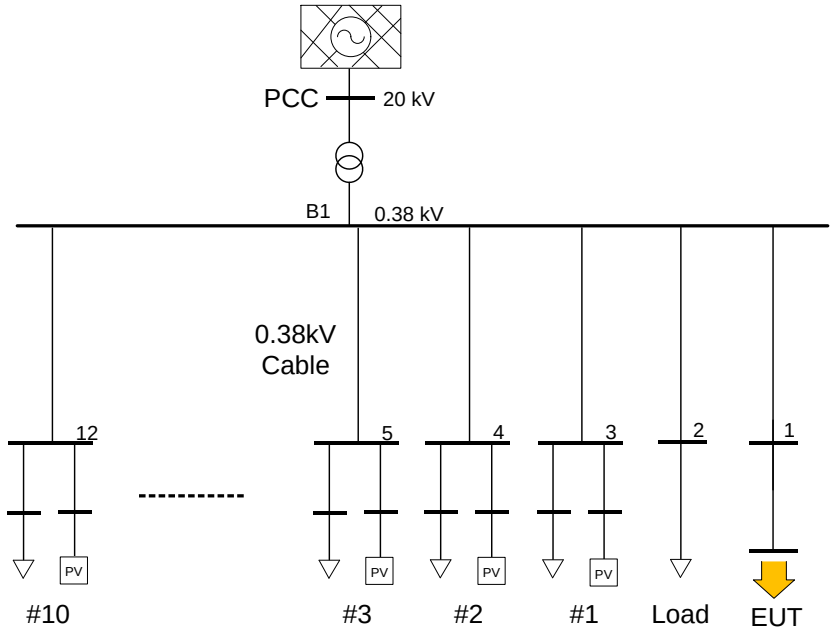



**Figure 6-36; Single line diagram of the testing grid model**

As is shown in Figure 6-36, through the transformer, the medium voltage city power grid is connected to the low voltage residential power grid. The transmission lines in this grid are 0.38 kV cables. The node 1 is connected to the EUT. The node 2 is connected to a 3 kW resistive load. From node 3 to node 12, each node is connected to a 4 kW PV inverter and a parallel 5 kW resistive load, in order to simulate the residential situation. The cable length from node 1 to the bus bar B1 is 0.1 km. The cable length between other nodes to B1 is 0.4 km. A short to ground fault is occur at the cable between bus bar B1 and node 2. The equivalent simplification model of Figure 6-36 is shown in Figure 6-37 with the simplification method in chapter 4. The parameters of this grid are shown in Table 6-1.

| Name | Parameter Name | Value |
|---|---|---|
| Medium voltage city power grid | Voltage | 20 kV |
| | Short circuit capacity | 100 MVA |
| Transformer | Rated power | 0.8 MVA |
| | Primary/ Secondary side voltage | 20/0.38 kV |
| | Connection type | Dyn |
| | Impedance voltage | 6.5% |
| Cable | Specific resistance | 0.13 Ω/km |
| | Specific inductance | 0.11 mH/km |
| Load | Rated power | 5 kW |
| PV inverter | Rated power | 4 kW |

**Table 6-1; Parameters of the testing grid**

In the real-time simulator (dSpace), the duration of each simulation period of this simplified model (Figure 6-37) is only 3.7 µs, which the total simulation step in 100 µs. Therefore, the equivalent simplification method in chapter 4 can effectively reduce the computational complexity and save computation time.

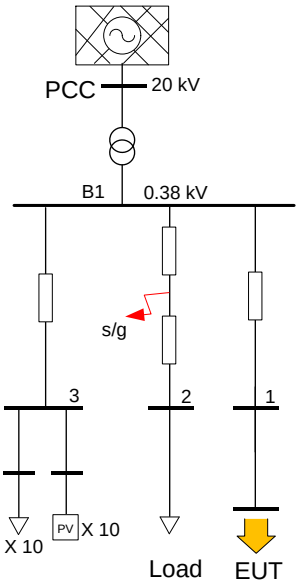



**Figure 6-37; Equivalent simplification model of the testing grid**

### 6.3.2 Experiments Results and Analysis

#### 6.3.2.1 Ideal Voltage Source and Power Hardware-in-the-Loop Test System

In order to reduce the impact to the grid from the grid-connected PV inverter, the controller of the PV inverter will use the soft start mode during start-up, where the amplitude of the output current will be slowly increased from zero to the rated current. The experiment results of the soft start situation of the EUT2 (red) are shown in Figure 6-38 and Figure 6-39. For better observation, the output current is magnified 10 times in these figures, the same below.

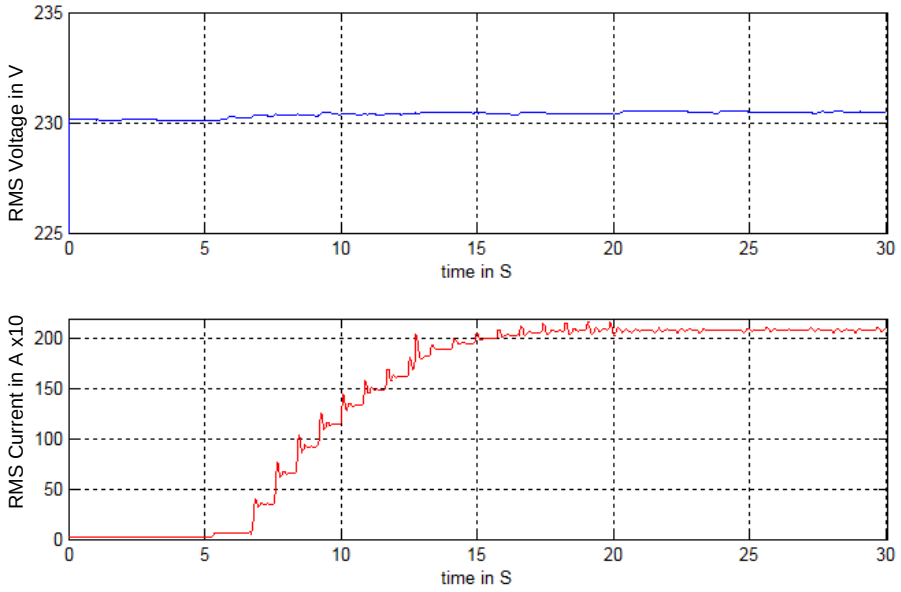



**Figure 6-38; RMS Voltage (Upper picture) and RMS current (Lower picture) during start-up with ideal voltage source**

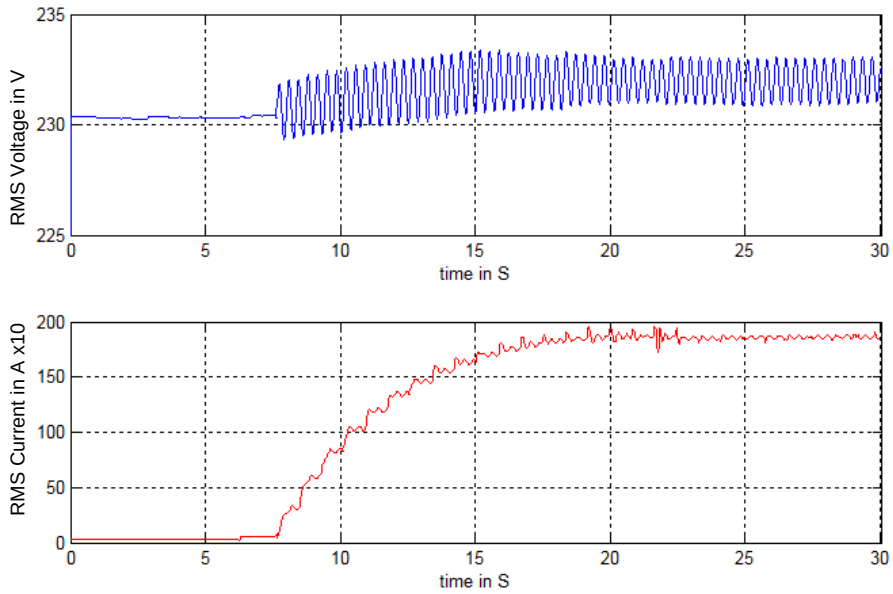



**Figure 6-39; RMS Voltage (Upper picture) and RMS current (Lower picture) during start-up with PHIL test system**

Figure 6-38 shows the experimental result with the Ideal Voltage Source. When the amplitude of the output current from the EUT (red curve) increases, the amplitude of the output voltage from ideal voltage source keeps almost constant. Figure 6-39 shows the experimental result with the PHIL test system. It can be seen that, when the amplitude of the output current from EUT (red curve) increases, the amplitude of the output voltage from the PHIL test system obviously increases. In addition, the waveform of the RMS voltage oscillating, which is caused by the RMS current oscillation. This result shows the retroactive effect of the real grid environment. The testing ability of the Power Hardware-in-the-Loop is verified.

It can be also seen that, the waveform of the current amplitude in Figure 6-38 changes in the form of steps and impulses. The waveform of the current amplitude in Figure 6-39 does not change obviously in the form of step or impulse. This means that, the reactions from the EUT to these to test methods are different.

Figure 6-40 and Figure 6-41 show the results of the LVRT testing of EUT1 (white). The output power of the EUT1 is set to 60% rated power. The residual voltage is set to 0.75 p.u. and the voltage dip duration is 625 ms. The residue voltage is directly set to 0.75 p.u. in the ideal voltage source. By selecting the location of the ground to short, the 0.75 p.u. residual voltage is also realized in PHIL test system.

Compare the results in Figure 6-40 and Figure 6-41, after the voltage dip, the output voltage (blue curve) of the PHIL test system is a little larger than the ideal voltage source. Due to the delay of the controller of the neighboring PV inverters, the output current stays high as during the voltage dip, that raising the voltage, as is mentioned in chapter 2.2.1.

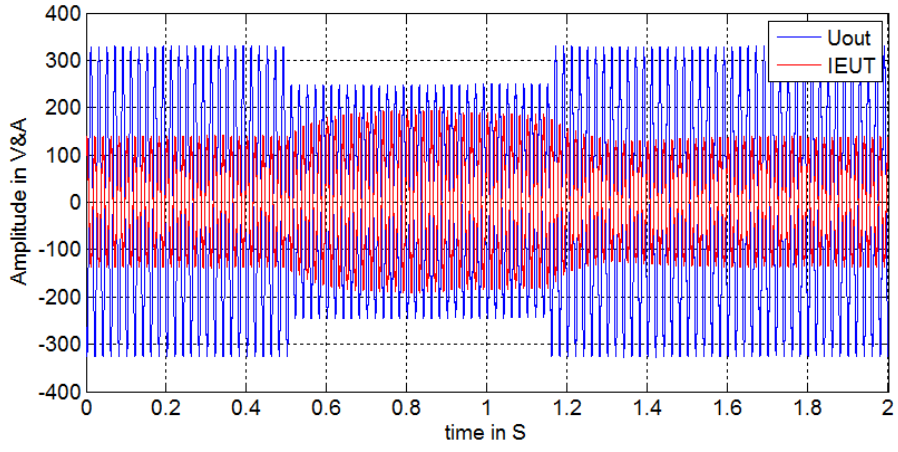



**Figure 6-40; LVRT testing of EUT1 in 60% rated power with the ideal voltage source**

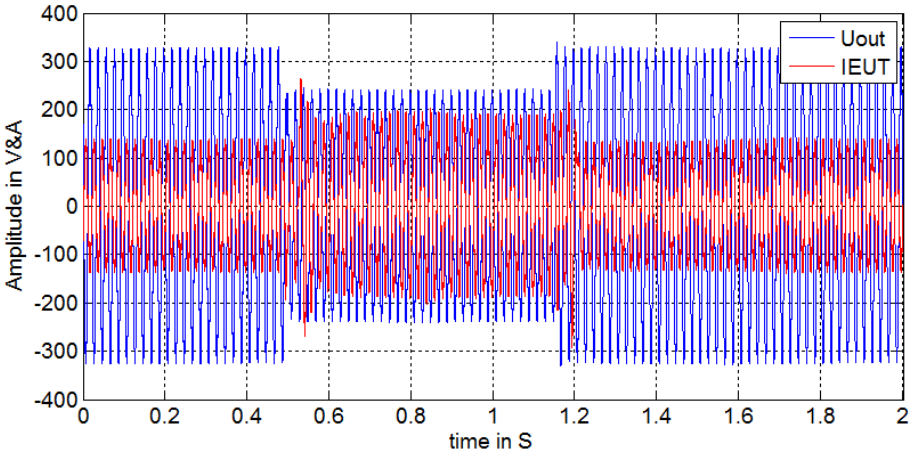



**Figure 6-41; LVRT testing of EUT1 in 60% rated power with the PHIL test system**

The most significant difference between Figure 6-40 and Figure 6-41 is the waveform of the output current of EUT (red curve). In Figure 6-40, the output current changes smoothly during and after the voltage dip. In Figure 6-41, the output current changes dramatically during and after the voltage dip.

After this test the output power of EUT is set to the 100% rated power. The LVRT testing is carried out with the residual voltage of 0.75 p.u. and a duration of 625 ms. The testing results are shown in Figure 6-42 and Figure 6-43.

In Figure 6-42, when the ideal voltage source is applied, the output current of EUT still changes smoothly during and after the voltage dip. In Figure 6-43, when the PHIL test system is applied, the output current changes dramatically during the voltage dip. After the voltage dip, the EUT cannot normally operate and shuts down. There is such a large difference of the reaction from EUT between ideal voltage source and PHIL test system. This is of the difference of the grid impedances and the neighboring PV inverters. This is already explained in chapter 2.2 and chapter 2.5.

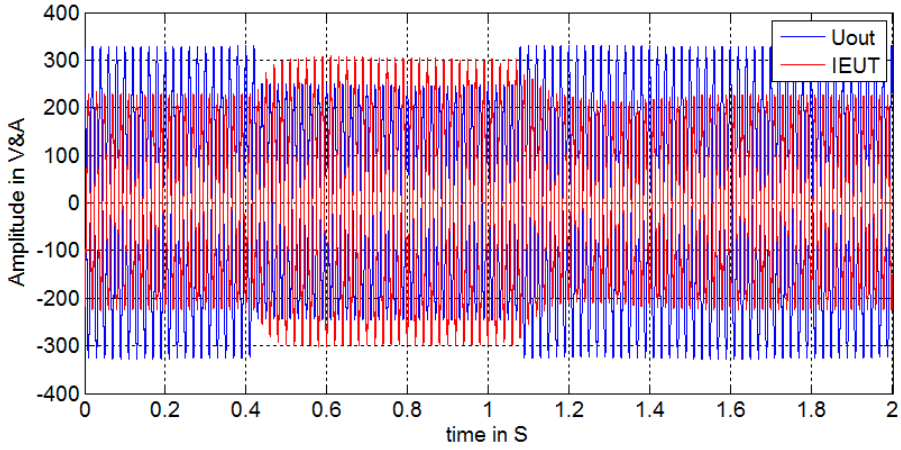



**Figure 6-42; LVRT testing of EUT1 in 100% rated power with the ideal voltage source**

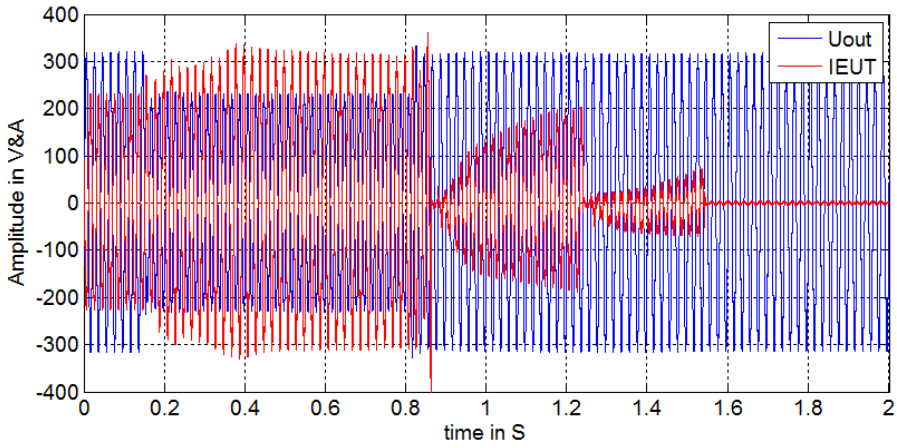



**Figure 6-43; LVRT testing of EUT1 in 100% rated power with the PHIL test system**

Figure 6-44 shows the details of the Figure 6-43. After the voltage dip, the output current of EUT (red curve) sharply reduces to zero, and cause a current oscillation, which may be caused by the LC filter of the EUT. At the same time, there is also a voltage oscillation with the same frequency, which is produced by the PHIL test system. This also verifies the retroactive effect of the PHIL test system.

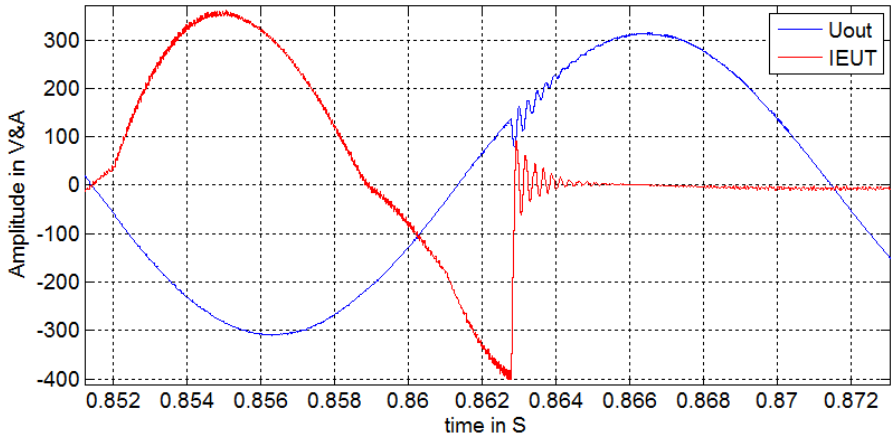



**Figure 6-44; LVRT testing of EUT1 in 100% rated power with the PHIL test system (Details)**

In Figure 6-45 and Figure 6-46 show the LVRT testing results of the three different EUTs with 100% rated output power, the residual voltage of 0.75 p.u. and a duration of 625 ms.

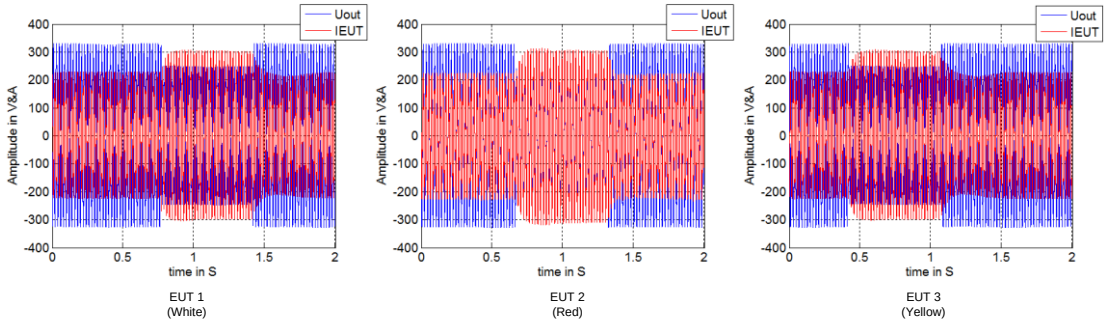



**Figure 6-45; LVRT testing of EUT1, 2 and 3 in 100% rated power with an ideal voltage source**

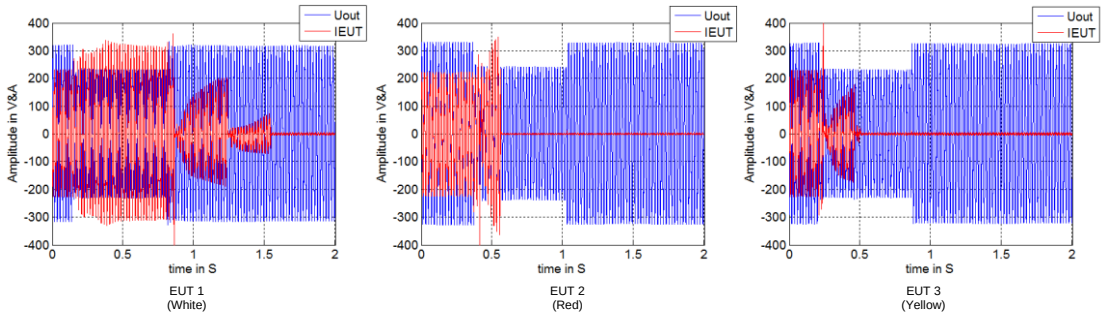



**Figure 6-46; LVRT testing of EUT1, 2 and 3 in 100% rated power with the PHIL test system**

As shown in Figure 6-45, the output currents of the EUTs change all smoothly during the test, when the ideal voltage source is applied. So the EUT can easily pass the LVRT testing with ideal voltage source. Figure 6-46 shows that the output currents of the EUTs change all dramatically during the test, when the PHIL test system is applied. And none of the EUT can pass the LVRT testing with the same testing condition, because the EUTs all shut down after or during the voltage dips.

Therefore, the ideal voltage source reduces the difficulty of the LVRT testing. The PHIL test system provides a real testing grid environment, which makes the LVRT testing more realistic.

### 6.3.2.2 Hardware Impedances and Software impedances

In this chapter, the comparative experiments concerning the hardware impedance and software impedance will be carried out with EUT3 (yellow), in order to verify the accuracy and the credibility of the PHIL test system.

In the grid compatibility testing, the testing of voltage changes, voltage fluctuations and flicker should be carried out with connecting of the reference impedance according to the IEC 61000-3 standards [90] [91].

The configuration of this experiment is shown in Figure 6-48. The same configuration is used for modeling in the PHIL test system, but there is no hardware impedance but only the software impedance in the real-time simulator. Figure 6-47 shows the photo of the impedance cabinet for IEC 61000-3 testing.

**Figure 6-47; Photo of the impedance cabinet**

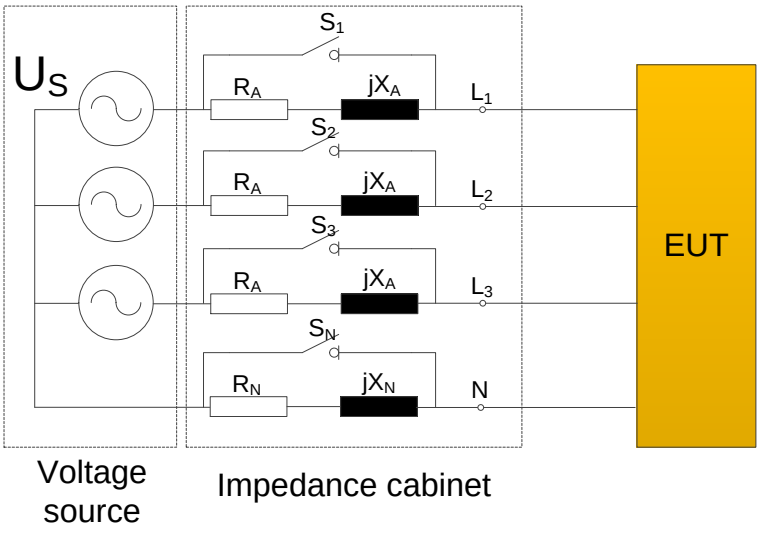
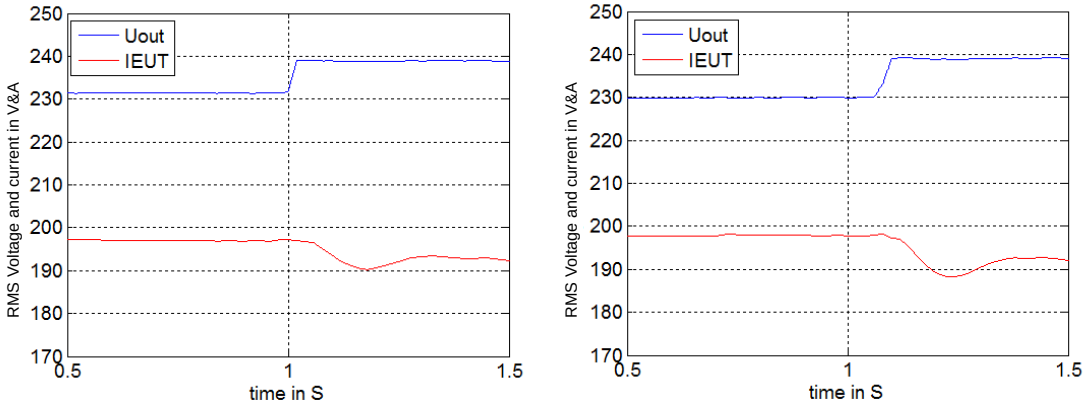



**Figure 6-48; Configuration topology of the experiment with the impedance cabinet**

As can be seen in Figure 6-48, the impedance cabinet is connected between the voltage source and the EUT in series. By the changing of the state of the switches $S_1$-$S_N$, the impedance between the voltage source and the EUT is changed. First, all switches are closed, there is a direct connection between the voltage source and EUT. Then open these switches are opened simultaneously, and the reference impedance appears between the voltage source and the EUT. The parameters of the reference impedance according to the IEC 61000-3 standards are shown in Table 6-2. In 61000-3 standards, there are two sub standards, IEC 61000-3-3, which has the larger reference impedance and IEC 61000-3-11, which has the smaller reference impedance (see Table 6-2). The experimental results of the both reference impedance are shown in Figure 6-49 and Figure 6-50.

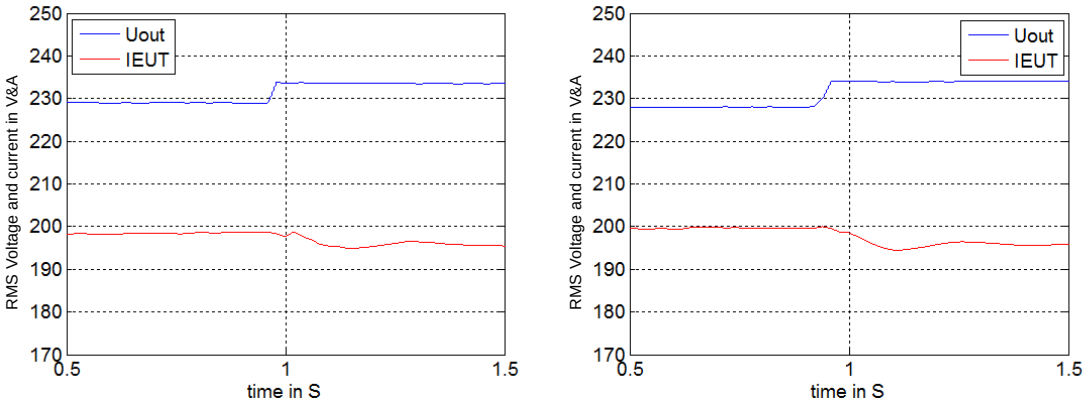
| IEC 61000-3-3 | | IEC 61000-3-11 | |
|---|---|---|---|
| **Name** | **Value** | **Name** | **Value** |
| $R_A$ | 0.24 Ω | $R_A$ | 0.15 Ω |
| $X_A$ | j0.15 Ω | $X_A$ | j0.15 Ω |
| $R_N$ | 0.16 Ω | $R_N$ | 0.15 Ω |
| $X_N$ | j0.10 Ω | $X_N$ | j0.10 Ω |

**Table 6-2; Parameters of the reference impedance**




a) With hardware impedance b) With software impedance

**Figure 6-49; RMS Voltage and current of hardware impedance (left) and software impedance (right) with IEC 61000-3-3**




a) With hardware impedance b) With software impedance

**Figure 6-50; RMS Voltage and current of hardware impedance (left) and software impedance (right) with IEC 61000-3-11**

As is shown in Figure 6-49, when these switches $S_1$ – $S_N$ opens, the reference impedance appeared between the voltage source and the EUT. The voltage amplitude of EUT (blue curve) increases due to this impedance and the power flow. In order to keep the output power constant, the output current amplitude of the EUT (red curve) decreases. It can also be seen in Figure 6-49 and Figure 6-50, that output voltage and current amplitude of EUT with the PHIL test system (software impedance) are essentially identical to the voltage and current amplitude with the impedance cabinet (hardware impedance). The accuracy and the credibility of the PHIL test system are proved.

## 6.4 Summary of this Chapter

In this chapter, an 800 kVA power amplifier is built. In steady performance experiments, the power amplifier operates in different classical PHIL testing conditions. It is proved that, this power amplifier has good accuracy in the frequency from 50 Hz to 2000 Hz. Through the application of the voltage dips, the fast response speed and the good stable performance have been verified.

Based on the power amplifier, the PHIL test system is built. Several PHIL interface algorithms are built into the real-time simulator. Through the experiment of different ratios of the impedance of hardware side and software side, the analysis of the accuracy, stability performance and the dynamical performance are carried out. The good comprehensive performance of the Damping Impedance Method has been verified.

Finally, a complete PHIL test system with actual photovoltaic grid-connected inverters is set up. Through the comparative experiments of three EUTs with different test generator configuration, such as ideal voltage source, PHIL test system and the impedance cabinet, the accuracy, reliability and credibility of the complete PHIL test system have been comprehensive verified.

# 7 Conclusions and Outlook

## 7.1 Conclusions

The Power Hardware-in-the-Loop test method can test distributed generation systems in a nearly real power grid environment. This test method can obtain the real operation characteristics of the EUTs, before they actually operate in real grid environment. This improves the reliability and credibility of the grid compatibility testing. In this thesis, a comprehensive research is carried out for the test methods, the PHIL interface algorithms, the grid models and the power amplifier.

This thesis is focused on the phenomenon, where the DG system passed the grid compatibility testing, but will not operate normally in the real grid. This phenomenon is studied under the aspects of hardware and control strategies of the DG systems, as well as the test methods and test generator. A.m. phenomenon is also reproduced in the laboratory. The grid-connected performance of the DG systems will be affected by the grid impedances and other neighboring DG systems. Open loop test methods and its test generator cannot reproduce these influences. Test methods provide the guidance for research and development of DG system, thus resulting in the defects in the control strategy of the DG systems. Open loop test methods and their recommended test generators, such as SI-VSG and ideal voltage source cannot detect these defects of DG system: the reliability and credibility of the grid compatibility testing is reduced. As a result, it is concluded that the PHIL test method and the PHIL test system is necessary.

In this thesis, the operation sequence of the suggested PHIL test system is analyzed in detail, the stability criterion based on the operation sequence is obtained. The running time of the measurement and sampling phase and the real-time calculation phase must be greater than or equal to the running time of the amplifier phase. In this high power PHIL test system, this condition is difficult to meet, so the operation sequence is optimized in this thesis. The real-time simulator is responsible for the calculation of the numerical grid model and also the control software of the power amplifier.

The developed PHIL test system connects the numerical grid model and hardware EUT through the PHIL interface. Because of the delay and interference in the information and power exchange between the software and hardware side, the PHIL interface algorithm is adopted to reduce the influence of delay and interference on the stability and accuracy of the system. On the basis of the existing PHIL interface algorithm, in this thesis several improvements are carried out. This thesis presents the online impedance parameter identification and phase compensation algorithm based on coordinate transformation, in order to enable the PHIL test system to test any kind of hardware EUT in any software

testing grid environment. Through the experiment of the different ratios of the impedance of hardware side and software side, the accuracy, stable and dynamical performance of the presented PHIL interface is verified.

In this thesis, through the analysis of the PHIL test system and DG systems (EUT), the performance requirements of the PHIL test system is given. It can sever as reference for other power levels of PHIL test system. It can sever as a reference to the development of PHIL test systems.

In the real-time simulation of the grid model of PHIL test system, the accuracy and computational complexity are needed to be considered first. Because large DG systems usually operate together with other DG systems in the same grid, the influences of these other DG systems also need to be reproduced by the testing grid model. In this thesis, a universal simplified model for DG systems based on power electronic equipment is presented through a detailed study of a large photovoltaic generation system and the Direct-drive Permanent Magnet Synchronous Generator. The resulting simplified model takes the input of the system DG as a constant, and the grid-connected device is considered as an ideal voltage or current source to reduce the complexity of the computational complexity. An equivalent modeling method for multi DG systems and the collection system of the power plant is also presented. By comparing the equivalent simplified model with the simulation results of the detailed model, the equivalent simplified model shows good accuracy.

In view of the requirements of accuracy, response speed and operation bandwidth in the high power PHIL test system, in this thesis a power amplifier is designed with a four-quadrant rectifier and three sets of single-phase inverters. In this thesis, the voltage and current dual loop control strategy based on the PR-P regulator is presented. The regulator parameters are determined by theory. The correctness of hardware topology design and control strategy is verified by experiment.

Finally, a set of PHIL testing on an 800 kVA level is carried out with real grid-connected inverters, the grid-connected inverters are tested through various operation conditions and grid environmental. The function of the PHIL test system is verified.

## 7.2 Outlook

In the course of this thesis, the need for further research showed up.

E.g. the phase compensation algorithm is only applicable to the non-harmonic component, and the three-phase balanced voltage signal. In future research, other delay compensation algorithms could be considered, such as predictive control techniques.

Also, the simplified modeling of photovoltaic generation system and Direct-drive Permanent Magnet Synchronous Generator is carried out. In the future, the simplified modeling of other types of DG systems should be developed, such as Double Fed Induction Generator.

The hardware parameters and the controller parameters of the DG system ware obtained by the usual algorithm this thesis. This cannot fully reproduce the real characteristics of the DG system. So in the future, the system identification method could be used to determine the parameters of the real DG system in order to get an even more realistic test environment.

In order to carry out PHIL testing for MVA class wind turbines, the MVA class power amplifier has to be developed in the future. The equivalent switching frequency and output voltage could be improved, e.g. by using carrier phase-shifting method.

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