

Mitigation of Low Frequency Common Mode Voltage in a Non-Isolated EV Charger

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Abstract—Non-isolated three-phase AC/DC electric vehicle (EV) chargers offer enhanced efficiency and power density compared to those incorporating a galvanic isolation stage. Due to the high parasitic capacitance of the EV battery to ground, even small Common Mode (CM) voltage components can generate significant leakage currents, potentially exceeding the 30 mA threshold defined by IEC 61851. In this work a non-isolated EV-charger concept consisting of a three-level T-type converter as AC/DC-stage and a symmetrical buck converter as DC/DC-stage is analyzed in detail. A low frequency (LF) CM voltage compensation strategy of the DC/DC converter stage is proposed to compensate the often used third-harmonic signal to increase the modulation range of the AC/DC converter. Extensive simulation verify the applicability of this compensation method resulting in considerably reduced leakage currents. A loss breakdown on the main circuit elements demonstrates the subsequent loss reduction.

Index Terms—Non-isolated Charger, Three-Phase, EMI Filter, Leakage Current, On-Board Charger

I. INTRODUCTION

Driven by the goal of reducing greenhouse gas emissions by 43% by 2030 (cf. [1]), the demand for electric vehicles is rising significantly. On-board chargers (OBCs) for electric vehicles must accommodate a wide range of grid voltages to charge high-voltage (HV) batteries with a voltage range of 250 V to 450 V. State of the art OBCs are usually galvanically isolated and typically a two-stage approach is used with a three-phase AC/DC converter and an isolated DC/DC converter for charging the battery. Galvanic isolation stages, which rely on the (bulky) isolation stage usually implemented using a low frequency (LF) or medium-frequency (MF) transformer, present significant challenges to both power density and efficiency [2], [3]. Non-isolated EV charger concepts raise increasing attention due to their possibly higher power density, improved efficiency, and lower cost compared to conventional isolated solutions. The adoption of transformerless converters in photovoltaic (PV) systems has demonstrated substantial benefits, doubling power density and improving efficiency by up to 2% [4], [5]. However, these chargers rely on

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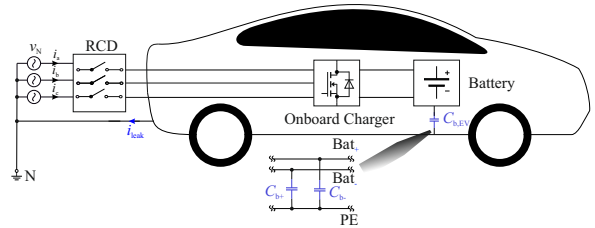


Fig. 1: Charging structure of a non-isolated on-board EV charger, HV-battery and RCD.

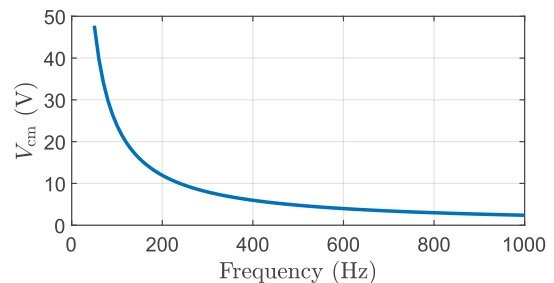


Fig. 2: Maximum permitted RMS CM voltage over RCD frequency range for the maximum (LF) ground leakage current $i_{leak} = 30$ mA (RMS) for $C_{b,EV} = 2$ μ F.

residual current devices (RCDs) to ensure safety, as specified by relevant standards (e.g., IEC 61851 or UL 2202). Such a charging structure including the grid, the RCD, the on-board charger and the car’s battery is shown in **Fig. 1**. Due to the elimination of galvanic isolation, low impedance CM paths are formed that can lead to significant leakage currents, potentially causing RCDs to trip [6], [7]. The most important part of these CM paths are the parasitic capacitances that are formed between the battery and the chassis, with values of several μ F (2-5 μ F) [8]. The maximum CM voltage (RMS) that can be present in the system without violating the RCD trip limit (30 mA RMS defined by IEC 61851) for the frequency range that the RCD is monitoring (< 1 kHz) is shown in **Fig. 2**. Some research groups have proposed modulation methods and topologies that limit LF and HF CM noise by utilizing a neutral conductor, often called three-phase four-wire systems [8]. Closed-loop solutions have been developed to suppress these leakage currents by regulating the LF CM ground current near to zero, without using bulky CM filters [9], [10]. In this work, a CM mitigation method is discussed for the case of

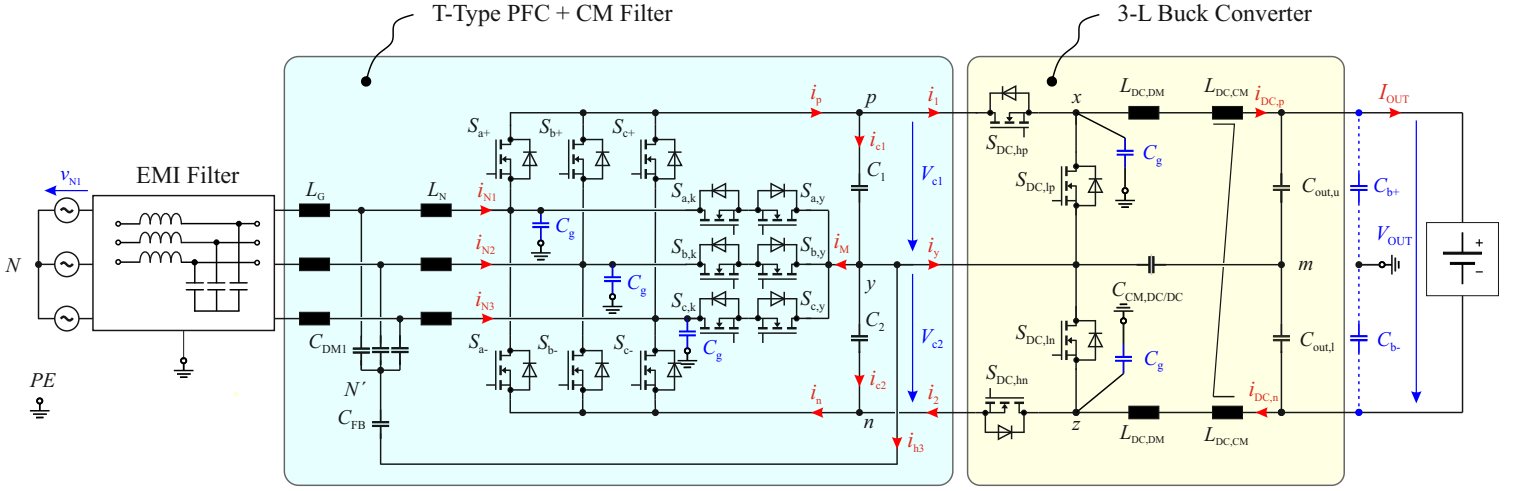


Fig. 3: Basic structure of the proposed non-isolated on-board charger consisting of a three-phase three-level T-type AC/DC converter and a symmetrical buck-stage. Both converter stages additionally introduce a high frequency CM filter stage.

a three-phase non-isolated on-board EV charger comprising a three-level boost PFC rectifier stage and a dual-buck DC/DC converter stage, in which the dual-buck DC/DC converter stage is used to compensate the LF CM voltage generated by the three-level PFC stage.

II. CONVERTER TOPOLOGY AND OPERATING PRINCIPLE

A. System Description

The basic structure of the proposed non-isolated EV charger is shown in **Fig. 3** and specifications are given in **Table I**. The topology consists of a three-phase three-level T-type AC/DC converter followed by a symmetrical buck DC/DC converter stage. Both converter stages include a high frequency CM filter. In case of the three-level T-type converter the capacitor midpoint y is thereto connected to the artificial star point built by the three DM filter capacitors C_{DM1} . In this case the DM filter capacitors form a low-pass (LP) CM filter together with the boost inductors L_N . In order to be able to select the cut-off frequency of the CM filter independently of the DM filter stage, capacitor C_{FB} is inserted in series to the DM capacitors. Please note that in this solution the high frequency components of the CM voltage create additional current ripple in the boost inductors L_N , however, the high frequency components in the CM voltage of the DC-link are well filtered, only the low frequency components, i.e. mainly the third-harmonic component remains.

For implementation of the required buck-stage a symmetrical variant is chosen to limit high frequency CM emissions. In addition, a CM filter stage similar to the three-level AC/DC converter is implemented but for the DC/DC-stage an additional CM-choke $L_{DC,CM}$ is connected in series to the two inductors $L_{DC,DM}$. The CM inductor $L_{DC,CM}$ builds together with the filter capacitors $C_{CM,DC/DC}$ a low-pass filter, however, in this case the high frequency CM-voltage is applied across the CM-inductor and doesn't increase the current ripple in the output of the buck stage.

TABLE I: Specifications of the Non-Isolated OBC.

Converter Specifications	
RMS Grid voltage	$V_{LL} = 400$ V
DC Output Voltage Range	$V_{out} = 250 - 450$ V
Rated output power	$P_{out} = 11$ kW
Battery Parasitic Capacitance	$C_{b,EV} = 2$ μ F

The modulation index $M = V_{N,peak}/(V_{DC}/2)$ of the three-level T-type converter without any measures is limited to $M = 1$. However, applying a third-harmonic CM component with amplitude $M_3 = 1/6$ (optimum for maximizing modulation range) in the modulation signal allows to increase the modulation range to $M = 2/\sqrt{3}$ lowering the required DC-link voltage and therefore further reducing PFC switching losses by $\sim 13\%$ [11]. In addition, the three-level T-Type converter intrinsically creates a low frequency capacitor midpoint current i_M with a main component at 150 Hz. This creates additional losses and a low frequency unbalance in the two DC-link capacitors. This unwanted effect can also be reduced by adding a third-harmonic component to the modulation signal. The optimal amplitude to minimize this midpoint current is $M_3 = 1/4$ and by using this low frequency CM component the midpoint current is almost reduced to zero thus reducing the losses in the DC-link capacitors and the required DC-link capacitance value.

The third harmonic-component in the modulation signal for both optimization goals, however, is visible in the DC-link of the converter and additional measures must be taken to limit the LF CM current caused by this voltage component.

B. CM Equivalent Model

The proposed converter structure can thereto be analyzed by using the equivalent model shown in **Fig. 4**. The CM behavior of the AC/DC-stage is modeled by equivalent LF and HF voltage sources $v_{CM,AC/DC,LF}$ and $v_{CM,AC/DC,HF}$, and the DC/DC-stage upper and lower half-bridges are modeled with

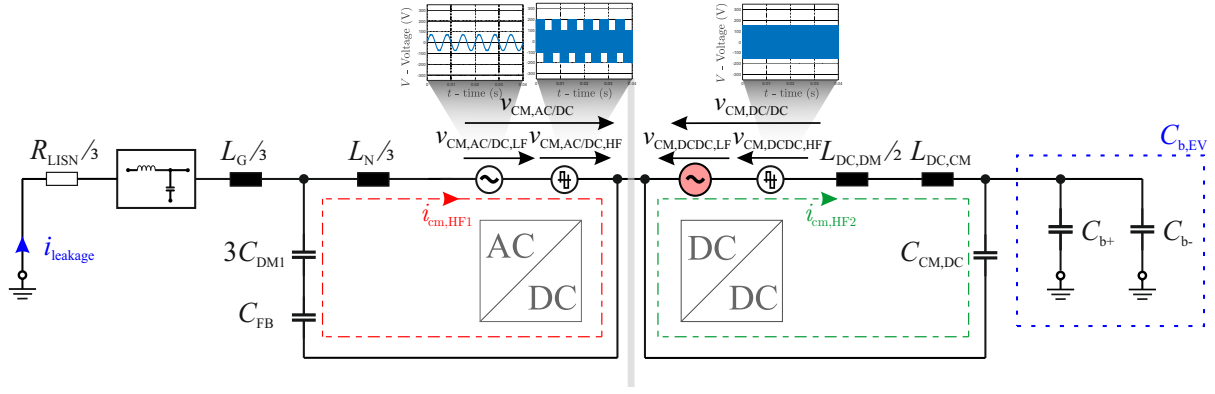


Fig. 4: CM equivalent model with battery parasitic capacitors C_{b+} and C_{b-} . CM noise shown for $V_{DC} = 600$ V and $V_{out} = 300$ V.

$v_{CM,DC/DC,LF}$ and $v_{CM,DC/DC,LF}$. These voltage sources include HF components, i.e. switching frequency and harmonics, and LF components, mainly third-harmonic component. The voltages are given by

$$v_{DM,AC/DC} = v_{py} + v_{yn}, \quad v_{DM,DC/DC} = v_{xy} + v_{yz}. \quad (1)$$

$$v_{CM,AC/DC} = \frac{v_{pPE} + v_{nPE}}{2}, \quad v_{CM,DC/DC} = \frac{v_{xPE} + v_{zPE}}{2}. \quad (2)$$

The discussed CM-filter stage of the three-level T-type converter built by the boost inductors L_N and C_{FB} is visible. On the battery side, the CM inductor $L_{DC,CM}$ form together with the CM capacitor $C_{CM,DC/DC}$ a second order LP filter to mitigate the HF CM voltage generated by the DC/DC-stage.

The LF CM voltage appears in the DC-link midpoint and is dominated by the third-harmonic signal of the AC/DC-stage used to increase the modulation range. These LF CM voltage components cause CM currents through the parasitic capacitors of the battery to ground and may result in nuisance tripping of the RCDs, considering that the capacitance values of the parasitic capacitors of the battery pack can be in the order of several μF [6], [7]. On the other hand, the symmetrical buck-stage is able to generate a LF CM voltage. If the CM voltage of the DC/DC-stage is controlled to compensate the low frequency CM voltage of the AC/DC-stage, i.e. $v_{CM,AC/DC,LF} = v_{CM,DC/DC,LF}$ then the midpoint of the buck-stage output capacitors and hence the battery stack show a potential close to PE thus reducing the LF CM currents considerably. Please note, that only the LF CM voltage can be compensated by this approach which is the main reason for the applied high frequency CM filter strategy of the AC/DC and DC/DC converter.

III. CM MITIGATION METHOD

To suppress the LF CM voltage generated by the AC/DC-stage, a CM mitigation method is therefore proposed. The DC/DC-stage needs to be modulated in such a way to compensate the LF CM voltage generated by the AC/DC-stage. In the following derivation, averaging over one switching cycle is used as switching ripple effects are not of interest for the LF CM mitigation. The averaged duty cycles of the upper and

lower bridge and voltages \bar{v}_{xy} and \bar{v}_{yz} of the buck stage are defined as

$$d_1(t) = \frac{V_{out}/2 + V_{CM,DCDC,LF}}{V_{C1}(t)}, \quad d_2(t) = \frac{V_{CM,DCDC,LF} - V_{out}/2}{-V_{C2}(t)}, \quad (3)$$

$$\bar{v}_{xy}(t) = d_1(t) \cdot V_{C1}(t), \quad \bar{v}_{yz}(t) = d_2(t) \cdot V_{C2}(t). \quad (4)$$

For that definition it is assumed that the (virtual) midpoint m stays constant at ground potential and that the two output voltages across the capacitors $C_{out,u}$ and $C_{out,l}$ are equal, i.e. $V_{out}/2$. Then, the DM component $v_{DM,DC/DC,LF}$ as well as the CM component $v_{CM,DC/DC,LF}$ of the DC/DC converter can be written as

$$v_{DM,DC/DC,LF}(t) = d_1(t) \cdot V_{C1}(t) + d_2(t) \cdot V_{C2}(t), \quad (5)$$

$$v_{CM,DC/DC,LF}(t) = \frac{d_1(t) \cdot V_{C1}(t) - d_2(t) \cdot V_{C2}(t)}{2}. \quad (6)$$

It is also intrinsic to the operation of the system that the total voltage in the DC-link is controlled to be constant, thus it can be obtained

$$V_{DC} = V_{C1}(t) + V_{C2}(t). \quad (7)$$

The LF CM voltage generated by the AC/DC-stage is a result of the modulation and is given by

$$v_{CM,AC/DC,LF}(t) = V_m \cdot \sin(3\omega t) = M_3 \cdot \frac{V_{DC}}{2} \cdot \sin(3\omega t) \quad (8)$$

if third harmonic component is used either to increase the modulation range or to reduce the midpoint current. The output voltage of the charger V_{out} is generated by proper modulation of the DC/DC-stage using the duty cycles

$$D_1 = D_2 = D = \frac{V_{out}}{V_{DC}}. \quad (9)$$

The DC/DC-stage shall compensate the LF CM voltage mainly consisting of a third-harmonic component and therefore in addition to the "DC component" also an AC component $d_{ac}(t)$ needs to be added. Referring to (5) and (6) the AC component $d_{ac}(t)$ needs to be added to the duty cycle d_1 of the upper

half-bridge and subtracted from the duty cycle d_2 of the lower half-bridge

$$d_1(t) = D_1 - d_{ac}(t) = D - d_{ac}(t), \quad (10)$$

$$d_2(t) = D_2 + d_{ac}(t) = D + d_{ac}(t). \quad (11)$$

The output current I_{out} is controlled by the output current controller to a constant value. The average half-bridge input currents as well as the average mid-point current $i_y(t)$ of the DC/DC converter are written as

$$i_1(t) = d_1(t) \cdot I_{out}, \quad i_2(t) = d_2(t) \cdot I_{out}, \quad (12)$$

$$\begin{aligned} i_y(t) &= -(1 - d_1(t)) \cdot I_{out} - (1 - d_2(t)) \cdot I_{out} \\ &= -2 \cdot d_{ac}(t) \cdot I_{out}. \end{aligned} \quad (13)$$

The sum of the midpoint currents $i_y + i_M + i_{h3}$ leads to a variation of the individual capacitor voltages. Therefore, also the current $i_M(t)$ generated by the three-level T-type AC/DC converter must be considered. This current has a strong third-harmonic component but also components at $k \cdot 150$ Hz where $k = 1, 3, 5, \dots$. The components for $k > 1$ are, however, small and can be neglected here. A careful analysis of the midpoint current of the three-level T-type converter results in

$$\begin{aligned} i_M(t) &= \hat{I}_N \sum_{i=1}^3 [M \cdot A^2 + M_3 \cdot \sin(3\omega t) \cdot A] \cdot (-\text{sgn}(A)) \\ &\simeq \left(\hat{I}_N \cdot \frac{M}{2} - \hat{I}_N \cdot 2 \cdot M_3 \right) \cdot \sin(3\omega t), \end{aligned} \quad (14)$$

with $A = \sin(\omega t - (i-1)\frac{2\pi}{3})$. The third current component which has to be considered for calculation of the capacitor midpoint current is the current i_{h3} as a result of the AC/DC CM filter structure where the midpoint y is connected to the artificial star-point N' built by the filter capacitors C_{DM1} . The LF CM current i_{h3} is a result of the added LF CM voltage of the AC/DC-stage and is applied on $3C_{DM1}$ and C_{FB} and is given by

$$\begin{aligned} i_{h3}(t) &= C_{tot} \cdot \frac{dv_{CM,AC/DC,LF}(t)}{dt} \\ C_{tot} &= \frac{3 \cdot C_{DM1} \cdot C_{FB}}{3 \cdot C_{DM1} + C_{FB}} \end{aligned} \quad (15)$$

This current is, however, quite small (15 mA peak for $M_3 = 0.25$ and $V_{DC} = 600$ V) and can be neglected.

The differential equations for the two capacitor voltages are hence

$$C_1 \cdot \frac{dV_{C1}(t)}{dt} = \frac{i_M(t)}{2} - d_{ac}(t) \cdot I_{out} + i_{h3}(t), \quad (16)$$

$$C_2 \cdot \frac{dV_{C2}(t)}{dt} = -\frac{i_M(t)}{2} + d_{ac}(t) \cdot I_{out} - i_{h3}(t). \quad (17)$$

Combining (5) and (6) with (10) and (11), the voltages of the DC-link capacitors can be rewritten as

$$V_{C1}(t) = \frac{v_{DM,DC/DC,LF}(t) + 2 \cdot v_{CM,DC/DC,LF}(t)}{2 \cdot (D - d_{ac}(t))} \quad (18)$$

$$V_{C2}(t) = \frac{v_{DM,DC/DC,LF}(t) - 2 \cdot v_{CM,DC/DC,LF}(t)}{2 \cdot (D + d_{ac}(t))} \quad (19)$$

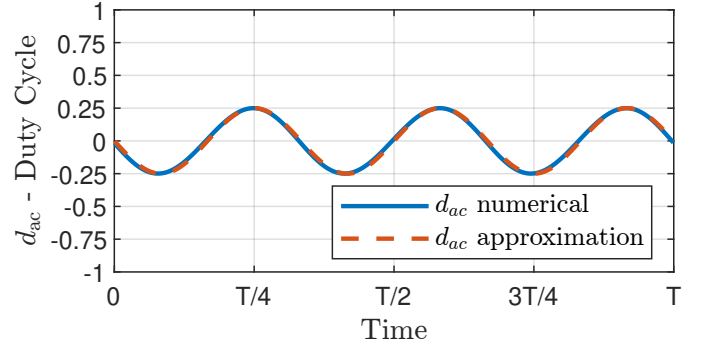


Fig. 5: Numerical solution (solid line) and approximation (dashed line) of $d_{ac}(t)$ for the proposed LF CM mitigation technique of the DC/DC converter for $M_3 = 1/4 \sin(3\omega t)$.

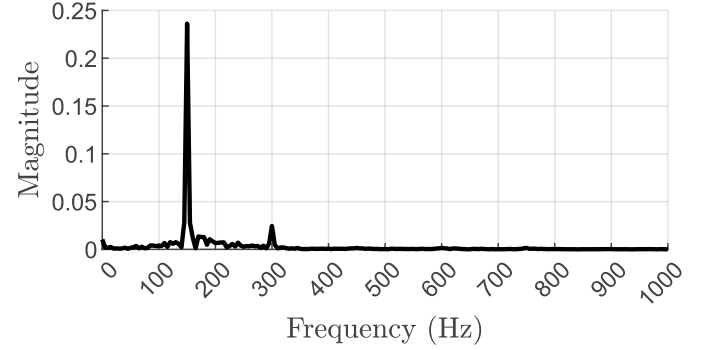


Fig. 6: Frequency spectrum of the numerically acquired $d_{ac}(t)$ for $M_3 = 1/4 \sin(3\omega t)$.

Using (16), (17), (18) and (19) assuming equal DC-link capacitors $C_1 = C_2$ and considering the desired DM and CM voltage components $v_{DM,DC/DC,LF}(t)$ and $v_{CM,DC/DC,LF}(t)$ the differential equation

$$\begin{aligned} \frac{d(d_{ac}(t))}{dt} &= \frac{2 \cdot (D - d_{ac}(t))^2 \cdot (2d_{ac}(t) \cdot I_{out})}{C_1 \cdot (v_{DM,DC/DC,LF}(t) + 2v_{CM,DC/DC,LF}(t))} \\ &\quad - \frac{2(D - d_{ac}(t)) \cdot \frac{dv_{CM,DC/DC,LF}(t)}{dt}}{(v_{DM,DC/DC,LF}(t) + 2v_{CM,DC/DC,LF}(t))} \end{aligned} \quad (20)$$

can be defined. Please note that the DM component is the battery voltage and the CM component should be the LF CM voltage of the AC/DC-stage which should be compensated by this approach. Equation (20) is challenging to solve analytically due to its inherent nonlinearity, coupled dynamics, and time-dependent coefficients. These characteristics render the equation unsuitable for standard analytical techniques, necessitating numerical methods for practical solutions and (20) is hence solved numerically for $d_{ac}(t)$ using MATLAB's `ode45` solver. The results are shown in **Fig. 5** and the corresponding frequency spectrum of the solution is depicted in **Fig. 6**. As expected, the result contains a third-harmonic component with the magnitude of 1/4 and higher order harmonics. As an analytical expression is difficult to be defined, a low error approximation can be made for $d_{ac}(t)$. Knowing that DC/DC converter needs to compensate the LF CM voltage generated by the AC/DC converter $v_{CM,AC/DC} = V_m \cdot \sin(3\omega t)$ to ensure

zero LF CM current, the duty-cycle $d_{ac}(t)$ can be estimated by

$$d_{ac}(t) = -\frac{2 \cdot V_m}{V_{DC}} \cdot \sin(3\omega t). \quad (21)$$

Using this duty cycle the resulting CM and DM voltages are given by

$$v_{CM,DC/DC,LF}(t) = -V_m \cdot \sin(3\omega t) - \frac{2 \cdot D}{3\omega C_1} \left[M_3 I_{out} - \hat{I}_N \left(\frac{M}{4} - M_3 \right) \right] \cos(3\omega t) \quad (22)$$

$$v_{DM,DC/DC,LF}(t) = D \cdot V_{DC} + \frac{M_3}{3\omega C_1} \left[M_3 I_{out} + \hat{I}_N \left(\frac{M}{4} - M_3 \right) \right] \sin(6\omega t). \quad (23)$$

According to (23) this modulation method creates a fluctuation of the DM DC/DC-stage voltage (output voltage) at twice the frequency of the reference CM voltage, i.e. 300 Hz, as the modulation process finally introduces a multiplication between a sinusoidal duty cycle $d_{ac}(t)$ with sinusoidal varying capacitor voltages V_{C1} and V_{C2} . If an output voltage controller is used with a bandwidth above the 6th harmonic, this variation is handled by the controller accordingly by adjusting the duty cycles $d_1(t)$ and $d_2(t)$ and the ripple is shifted to the DC-link voltage V_{DC} . The resulting 6th harmonic voltage ripple in the DC-link V_{DC} , however, shows a value below < 1 V for the converter at hand and is almost negligible.

A. Controller Structure

In the following, a control structure for the DC/DC converter including the LF CM mitigation technique is introduced. The proposed control scheme is presented in **Fig. 7**. The DC/DC converter output is controlled using a cascaded PI structure. The inner current controller $K_3(s)$ controls the charging current while a superimposed output voltage controller $K_2(s)$ generates the reference current i_{DC}^* . The current controller generates the duty-cycle component D used in (10) and (11). The CM component given by d_{ac} in (10) and (11) is set by a dedicated CM voltage controller. The CM voltage is thereto measured and the high frequency components are filtered to achieve $v_{CM,DCDC,LF}$. This voltage is now compared with the CM voltage of the AC/DC-stage $v_{CM,ACDC,LF}$ and the deviation is the input of the CM voltage controller $K_1(s)$. For the CM voltage controller a simple P-type controller with feedforward of the LF CM voltage of the AC/DC-stage $v_{CM,ACDC,LF}$ (through $d_{ac,ff} = -M_3 \cdot \sin(3\omega t)$) is used. Finally, the duty cycles for the upper and lower bridge $d_1(t)$ and $d_2(t)$ are calculated by combining d_{AC} and D . The design of the dedicated controllers is not further discussed here for the sake of brevity.

IV. CONVERTER LOSSES

The proposed CM mitigation method influences power losses in several key components, including the power semiconductors and the DC-link capacitors and in the following these loss elements are in focus of the analysis. The cases for

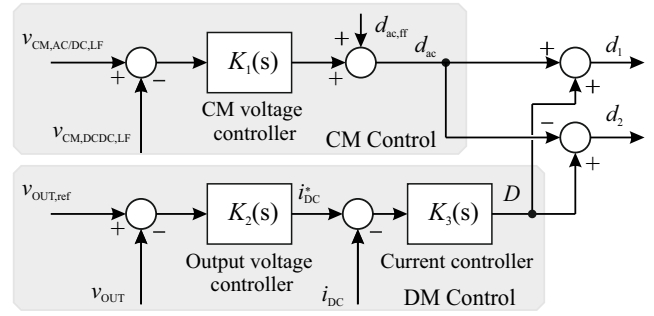


Fig. 7: Proposed control structure for the DC/DC-stage of the non-isolated 3- Φ EV charger consisting of a DM controller part ($K_2(s)$ and $K_3(s)$) and a CM voltage controller $K_1(s)$.

comparison are the modulation without 3rd harmonic signal in the AC/DC-stage ($M_3 = 0$) resulting in a DC-link voltage of $V_{DC} = 700$ V for a symmetrical 400 V grid and modulation with a 3rd harmonic signal with amplitude $M_3 = \frac{1}{4}$ resulting in a DC-link voltage of $V_{DC} = 600$ V. For the three-level T-type converter with a grid voltage of 400 V, switches with a blocking voltage of 1200 V are required for $S_{n,+}$ and $S_{n,-}$ and hence conduction losses are given by

$$P_{cond,n+} = P_{cond,n-} = \hat{I}_N^2 \cdot \left(\frac{2M}{3\pi} \right) \cdot R_{ds,on,1200} \quad (24)$$

while for the mid-point switches $S_{n,k}$ and $S_{n,y}$ a blocking voltage of 650 V is sufficient and conduction losses are hence given by

$$P_{cond,n,k} = P_{cond,n,y} = \hat{I}_N^2 \cdot \left(\frac{1}{4} - \frac{2M}{3\pi} \right) \cdot R_{ds,on,650} \quad (25)$$

where n is the number of phase $n \in \{a, b, c\}$. For calculation of the three-level T-type switching losses, a hard switching model according to [12] is used. The switching losses in a T-type bridge-leg are given by

$$E_{sw} = E_{loss,cap}(V_{sw}, I_{sw}) + Q_{rr}(I_{sw})V_{sw} + \frac{1}{2} \frac{V_{sw}^2}{dv_{sw}/dt} I_{sw} + \frac{1}{2} \frac{I_{sw}^2}{di_{sw}/dt} V_{sw}. \quad (26)$$

The first term, $E_{loss,cap}$, represents the energy stored in the nonlinear parasitic output capacitance of the MOSFETs, which strongly depends on the switched voltage, while Q_{rr} is the reverse recovery charge of the MOSFET body diode involved in the commutation. The last two terms $\frac{1}{2} \frac{V_{sw}^2}{dv_{sw}/dt} I_{sw}$ and $\frac{1}{2} \frac{I_{sw}^2}{di_{sw}/dt} V_{sw}$ in (26) represent $V-I$ overlap losses which can be neglected if WBG power semiconductors such as SiC or GaN are applied, given their high switching speeds. The capacitive energy losses and the energy losses of reverse recovery of the

semiconductors of phase n are given by

$$\begin{aligned}
E_{sw,AC/DC} = & E_{oss,Sn,k} \left(\frac{V_{dc}}{2} \right) + \\
& + Q_{oss,Sn+} \left(\frac{V_{dc}}{2} \right) \frac{V_{dc}}{2} - E_{oss,Sn+} \left(\frac{V_{dc}}{2} \right) + \\
& + \left[E_{oss,Sn-}(V_{dc}) - E_{oss,Sn-} \left(\frac{V_{dc}}{2} \right) \right] - \\
& - \left[Q_{oss,Sn-}(V_{dc}) - Q_{oss,Sn-} \left(\frac{V_{dc}}{2} \right) \right] \frac{V_{dc}}{2} + \\
& + \tau_{Sn+} |I_{sw}| \frac{V_{dc}}{2}
\end{aligned} \quad (27)$$

where Q_{oss} and E_{oss} represent the charge and the energy stored in the parasitic output capacitance of the respective switches, and τ is the time required for charge recombination in the switches. Details of this enhanced switching loss model can be found in [12]. The losses of the DC/DC-stage are modeled in a similar manner. Conduction losses of the power switches in the DC/DC-stage can be calculated by

$$P_{cond,hp} = P_{cond,hn} = D_1 \cdot I_{out}^2 \cdot R_{ds,on,DC/DC} \quad (28)$$

$$P_{cond,lp} = P_{cond,ln} = (1 - D_1) \cdot I_{out}^2 \cdot R_{ds,on,DC/DC} \quad (29)$$

and switching losses are estimated using loss data provided in the datasheet, however, scaled to the occurring voltage level

$$\begin{aligned}
P_{sw,hp} &= P_{sw,hn} = P_{sw,lp} = P_{sw,ln} \\
&= f_{s,DC/DC} \cdot (E_{on,hp} + E_{off,hp}).
\end{aligned} \quad (30)$$

Next, the LF power losses in the DC-link capacitors due to ESR are considered. Please note that switching frequency ripple components are not considered in this comparison as they do not change considerably by applying the proposed CM mitigation technique. Without third-harmonic signal in the modulation strategy of the DC/DC converter the capacitor losses caused by the low frequency components in the capacitor current are given by

$$P_{ESR,LF} = \frac{ESR}{2} \cdot \hat{I}_N^2 \cdot \left(\frac{M}{2} \right)^2 \quad (31)$$

and a relatively large current component caused by the third harmonic mid-point current of the AC/DC-stage exists (compare also with (14)). When the third-harmonic signal is used in the AC/DC-stage and compensation is applied in the DC/DC-stage the additional losses due to the LF midpoint current result in

$$P'_{ESR,LF} = \frac{ESR}{2} \cdot \left[M_3 \cdot I_{out} + \hat{I}_N \left(\frac{M}{2} - 2 \cdot M_3 \right) \right]^2 \quad (32)$$

V. SIMULATION RESULTS

To verify the fundamental operating principle of the proposed method, extensive simulations were conducted using PLECS circuit simulation software with the parameters given in **Table II** and specifications listed in **Table I**. Both, the

TABLE II: Parameters of the non-isolated Charger

Simulation Parameters	
AC/DC semicond. S_k	AIMCQ120R030M1T, 1200 V, 30 m Ω
AC/DC semicond. $S_{k,y}$	IMLT65R050M2H, 650 V, 50 m Ω
DC/DC-stage semicond. $S_{DC/DC}$	IMLT65R020M2H, 650 V, 20 m Ω
DC-link Capacitors C_1, C_2	4 \times B43268C5277M060, 450 V
AC/DC Switching Frequency	$f_{s,AC/DC} = 100$ kHz
DC/DC Switching Frequency	$f_{s,DC/DC} = 100$ kHz
Boost Inductance	$L_N = 3 \times 130$ μ H
DC-link Capacitance	$C_o = 2 \times 1$ mF
Output DM Inductance	$L_{DC,DM} = 2 \times 20$ μ H
Output CM Inductance	$L_{DC,CM} = 2.5$ mH
Output Capacitance	$C_{out} = 2 \times 22$ μ F
DC/DC-stage CM Capacitance	$C_{CM,DC/DC} = 50$ nF

AC/DC as well as the DC/DC converter operate with a switching frequency of 100 kHz and the two modulators are operating synchronously. The converter is operated at a grid voltage of 400 V, battery voltages of $V_{out} = \{250 \text{ V}, 350 \text{ V}, 450 \text{ V}\}$ under full charging power of $P_{out} = 11$ kW. The AC/DC-stage uses a third harmonic signal with $M_3 = 1/4$ but the compensation method is enabled at $t = 20$ ms. The corresponding results are shown in **Fig. 8**. During the first period, where the compensation strategy is not enabled, a large third-harmonic leakage current i_{leak} occurs due to the LF CM-voltage generated by the AC/DC-stage and the large parasitic capacitance $C_{b,EV}$ of the battery to ground. This current obviously exceeds the limits of 30 mA of commercial RCDs.

When the compensation method is enabled at $t = 20$ ms the DC/DC converter stage starts to compensate the CM voltage generated by the AC/DC-stage by modulating d_1 and d_2 , and third harmonic variations of these duty-cycles are visible and the results are in good agreement with the theoretical derivations. The generated CM voltage of the DC/DC-stage corresponds to that of the AC/DC-stage. The modulation introduces fluctuations in the capacitor voltages $V_{C1}(t)$ and $V_{C2}(t)$ at third harmonic (150 Hz), however, the total DC-link voltage V_{DC} remains nearly constant, exhibiting only a small fluctuation at 300 Hz. As expected, the grid currents are not affected by the compensation approach.

When the compensation method is enabled, the leakage current i_{leak} is reduced considerably. The resulting leakage RMS currents are shown in **Fig. 8** for the inspected battery voltages. The leakage currents remain well below the IEC 61851 limit of 30 mA for all battery voltages validating the applicability of the proposed modulation method.

As a next step the main power semiconductor as well as DC-link capacitor losses of the approaches without third-harmonic component in the AC/DC-stage and the proposed modulation strategy are calculated using the specifications listed in **Table II**. The calculated losses are summarized in **Fig. 9** for $V_{out} = 250$ V which is the minimum battery voltage

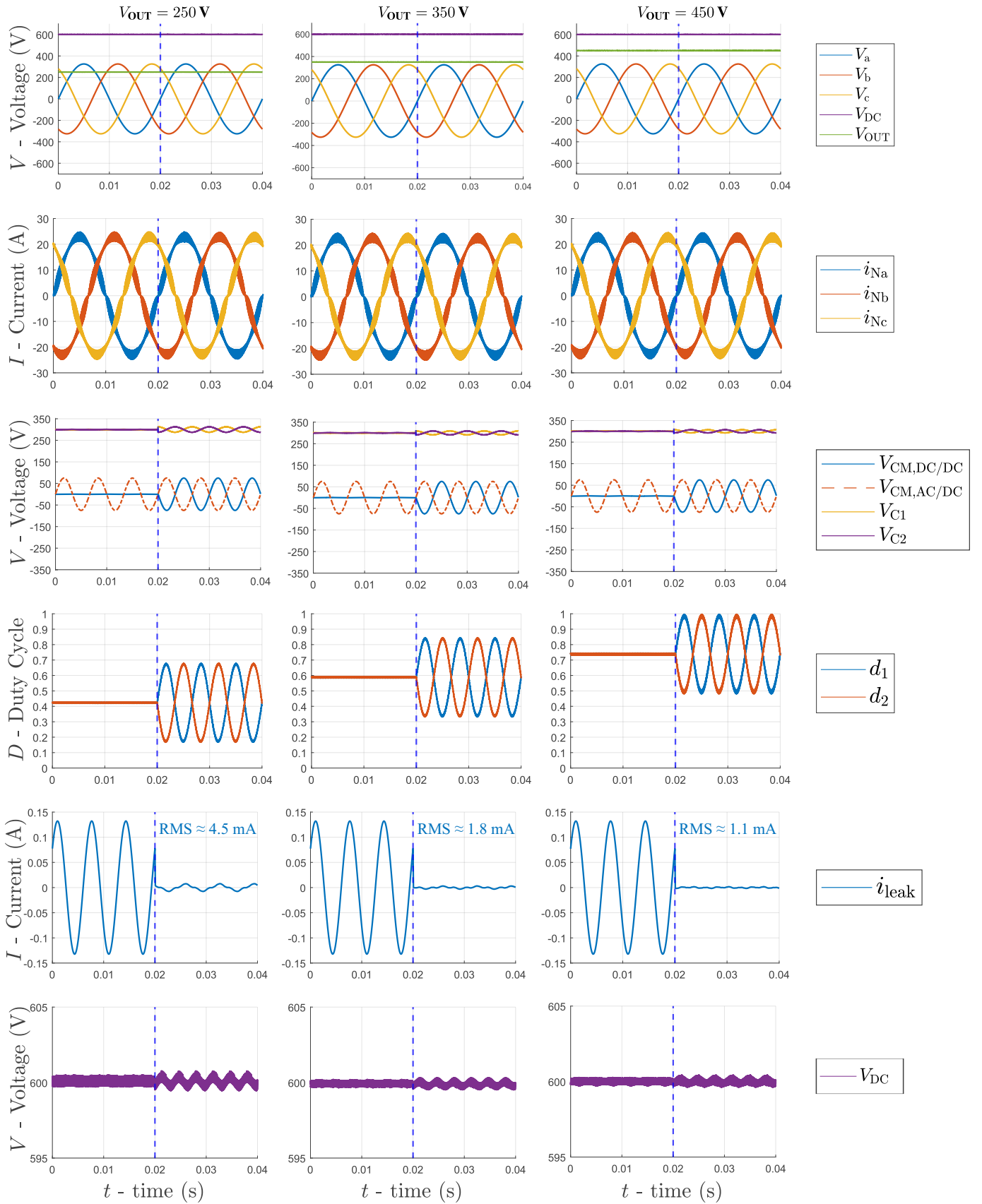


Fig. 8: Simulation results applying the proposed modulation method on the three-phase non-isolated onboard charger concept for a grid voltage of 400 V, battery voltages of $V_{out} = \{250\text{ V}, 350\text{ V}, 450\text{ V}\}$ and an output power of $P_{out} = 11\text{ kW}$. Modulation strategy is enabled at $t = 20\text{ ms}$. Simulated key waveforms include the DC-link voltage V_{DC} , battery voltage V_{out} , grid voltages v_{Ni} and currents i_{Ni} , DC-link capacitor voltages V_{C1} and V_{C2} and corresponding duty cycles d_1 and d_2 as well as CM voltages of the AC and DC stage $V_{CM,AC/DC}$ and $V_{CM,DC/DC}$ and the resulting leakage current i_{leak} .

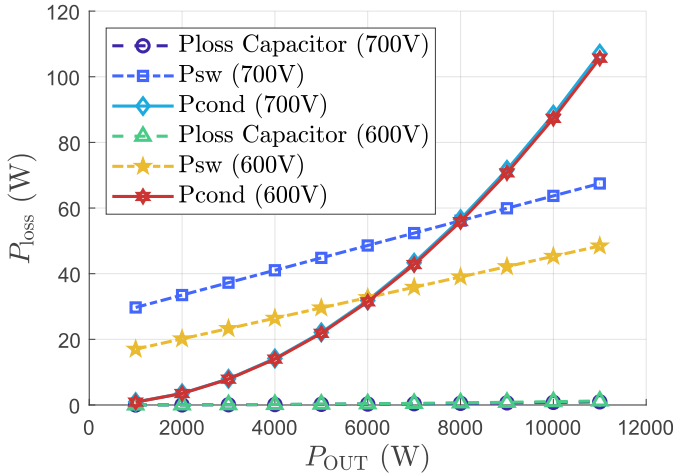


Fig. 9: Calculated loss comparison between the approaches without 3rd harmonic component in the AC/DC-stage ($V_{DC} = 700$ V) and the proposed modulation approach ($V_{DC} = 600$ V) as a function of P_{out} and $V_{out} = 250$ V using the parameters specified in **Table II**.

and therefore worst-case scenario for the current stress of the DC-link capacitors C_1 and C_2 . For the approach without third-harmonic signal in the AC/DC converter the DC-link voltage is set to 700 V while the DC-link voltage is reduced to 600 V for the proposed modulation method. In **Fig. 9** total conduction losses P_{cond} , total switching losses P_{sw} as well as DC-link capacitors losses $P_{loss, capacitor}$ are plotted as a function of charging power P_{out} . Whereas the conduction losses of the two approaches are quite similar the switching losses of the approach with third-harmonic signal in the AC/DC-stage and compensation allows to reduce the switching losses considerably (e.g. 25% in full load operation with $P_{out} = 11$ kW). Conduction losses P_{cond} are dominating in both cases for higher output power, however, the efficiency improvement is most noticeable at low and mid-load levels, where switching losses dominate total converter losses. The losses in the ESR of the DC-link capacitors C_1 and C_2 represent in both cases a very small portion of the overall losses (≈ 1 W in both cases). The increased DC-link capacitor currents and losses need to be considered during design of the converter when the proposed method shall be applied.

VI. CONCLUSION

This paper presents a novel low frequency common-mode (LF CM) voltage mitigation strategy for non-isolated three-phase AC/DC electric vehicle (EV) chargers. By leveraging the modulation of the DC/DC-stage to compensate for the LF CM voltage generated by the AC/DC-stage, the proposed method significantly reduces leakage currents, preventing nuisance tripping of residual current devices (RCDs). Simulation results confirm that the technique successfully maintains leakage currents well below the 30 mA threshold defined by IEC 61851, demonstrating its effectiveness in ensuring compliance with safety standards. Beyond leakage current suppression,

the method also enables a reduction in the required DC-link voltage, leading to improved efficiency. While this approach introduces additional losses in the DC-link capacitors due to increased ESR-related current ripple, the overall efficiency gains outweigh these drawbacks, particularly at low and mid-load conditions. Future work will focus on experimental validation of the proposed strategy to assess its real-world performance.

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