

Teaching Microcontroller Design with RISC-V



Florian Riedl
florian.riedl@tugraz.at
Graz University of Technology

Microcontroller Design @ TU Graz

- Processor Architecture Lecture (Theory)
- Processor Architecture Practicals (Exercises)
- Microcontroller Design Laboratory (Application)
 - Develop a μC for an FPGA
 - Practical application of acquired knowledge

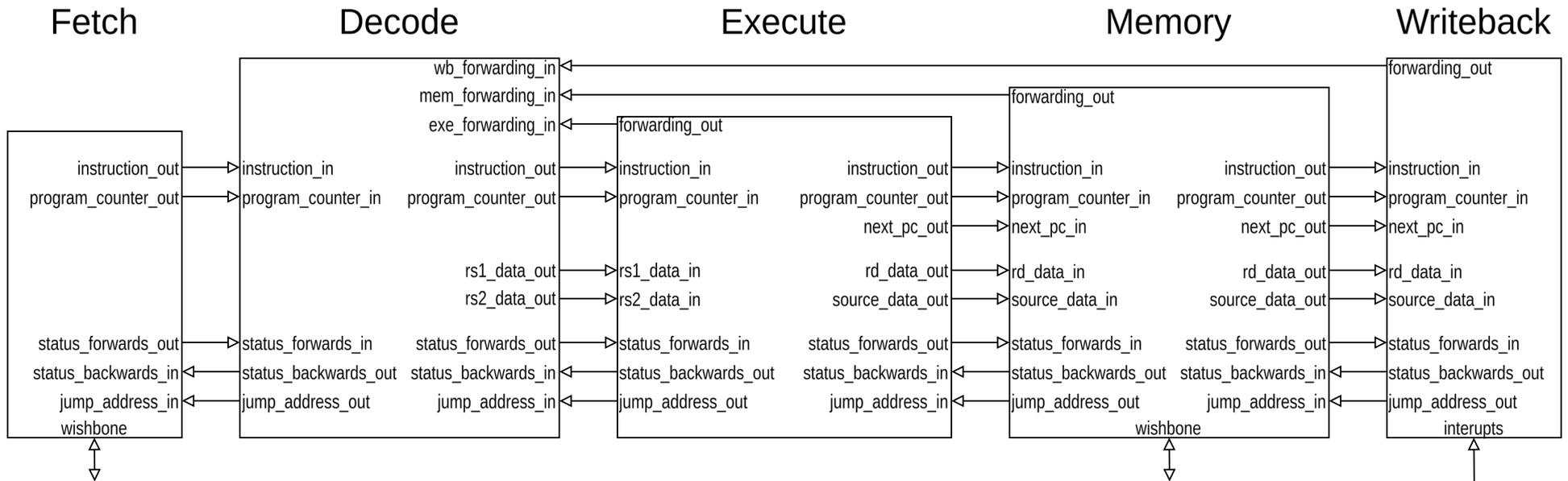
Old HaDes Architecture

- Microarchitecture mostly detached from lecture
 - Multicycle architecture (not pipelined)
 - Harvard architecture (separate instruction memory)
- Custom instruction set architecture
 - Special assembly syntax required
 - No C-compiler available

Why RISC-V?

- Not just a toy architecture
 - Knowledge transfer to/from other courses/industry
 - Good toolchain support (compilers, assembler)
 - Detailed documentation
- Opportunity to align with lecture and practicals
 - Most notably a 5-stage pipeline

Introducing: HADES-V



Technical Details

- Minimal RV32I implementation
 - Including interrupts/exceptions, CSRs, ...
- 5-stage pipeline
 - Fetch, Decode, Execute, Memory, Writeback
- Memory access via Wishbone interface
 - Two memory read ports, some basic peripherals

Course Details

- Implementation using SystemVerilog
 - Students implement and connect the stages
 - MCU adjacent final free-form assignment
- Opaque reference implementation
 - Allows students comparative testing of stages
 - Allows running of full system tests at any point

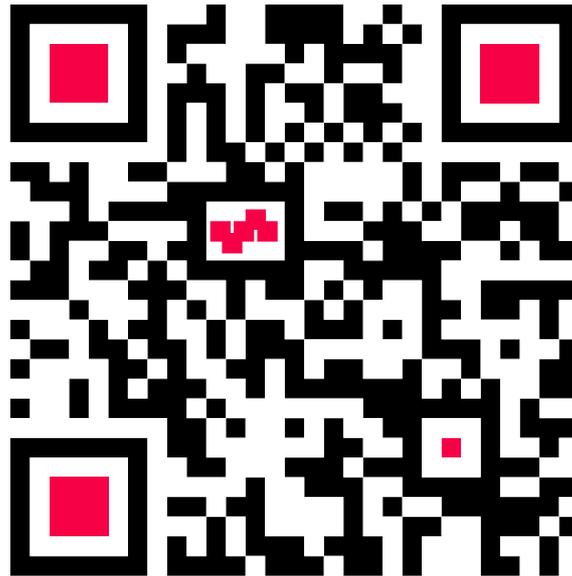
Introducing: PERSEPHONΞ

- Extensive test suite for HADES-V
 - SystemVerilog testbench for each stage
 - Assembly tests for full CPU
 - Automated grading and student feedback
- Ensures fairness and increases motivation
 - Provides feedback before final submission

RISC-V Community Challenge with HADES-V

- Course contents available to the public as OER
 - You get the course manual and template repository
- You can sign-up to participate in the challenge
 - We provide you the PERSONAL feedback
- You receive no grade, but a certificate
 - 3 different Credly certificates can be awarded

Join us for the Challenge!



<https://community.riscv.org/e/mp8k48/>