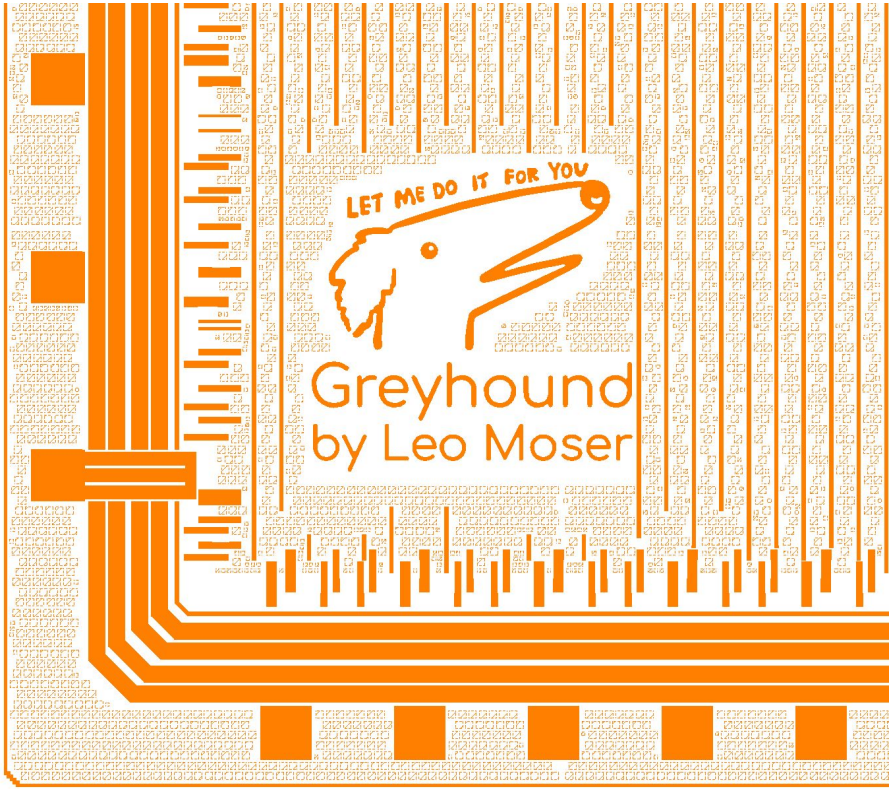
Greyhound

A Reconfigurable and Extensible RISC-V SoC and eFPGA



About Me - Leo Moser

- Open Source Silicon Advocate!
- Member of the FOSSi Foundation
- Master's at Graz University of Technology
- Previous work around FOSSi:
  - Work @ Efabless:
    - CACE
    - Improve magic & netgen for IHP
    - OpenLane 2 support for IHP
  - Work @ IHP:
    - LibreLane end-to-end flow
  - Work @ wafer.space:
    - Full-chip LibreLane template
    - Work on the gf180mcu PDK
    - Automatic reticle stitcher

@leo:fossi-chat.org

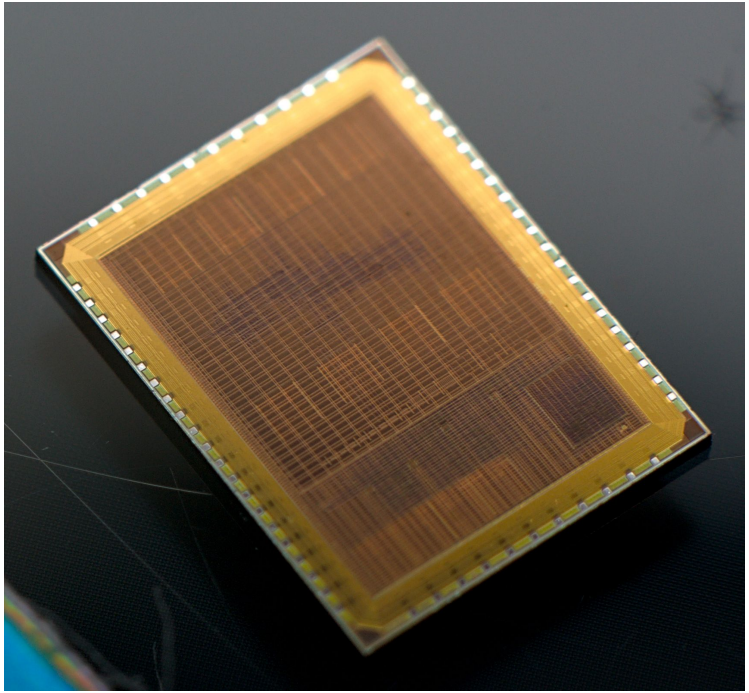
Open Source Silicon - The Story So Far

- June 2020: **sky130** PDK released
- December 2022: **gf180mcu** PDK released
- Since 2023: **ihp-sg13g2** PDK

  in active development

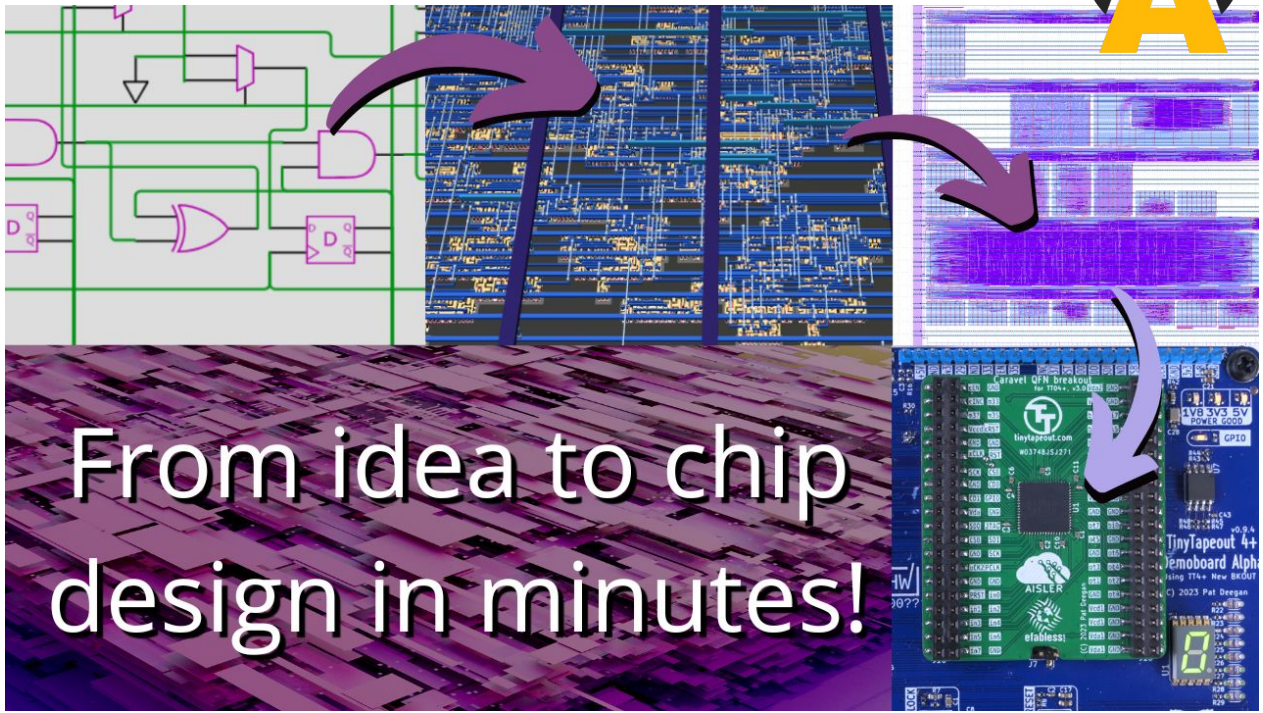
Open Source Tapeout Programs

- ChipFoundry
  - $ 14,950 @ up to 15mm²
  - SKY130
  - 100 QFN-packaged chips
- wafer.space
  - $ 8,500 USD @ ~20mm²
  - GF180MCU
  - 1,000 die wire-bonded onto PCBs
- IHP
  - Low-Cost MPW Access for Open-Source Designs
  - 2800€/1500€ per mm²
  - SG13G2 and SG13CMOS(5L)



Tiny Tapeout

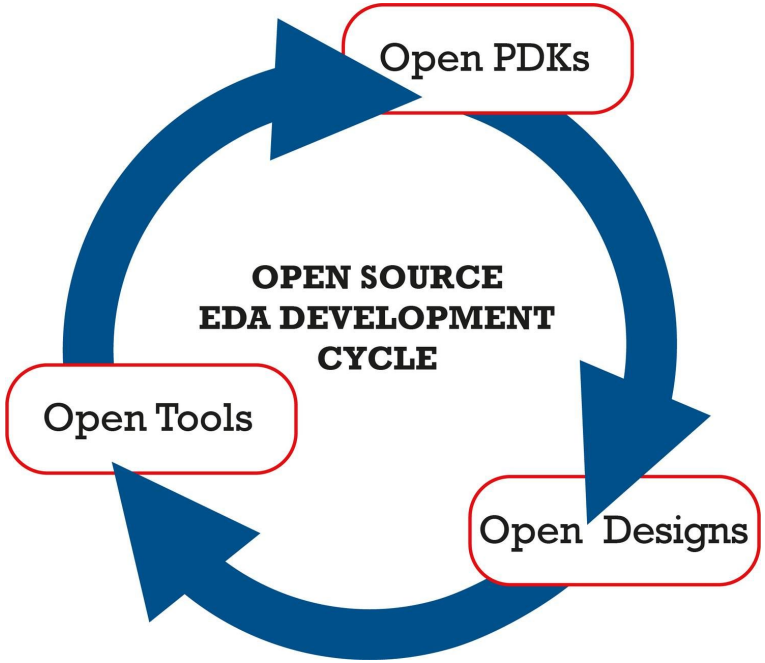
European Open Source Awards



https://tinytapeout.com

The Chip Design Revolution in Education

- Students can freely access:
  - EDA tools
  - PDKs
  - and designs
- Chip design is becoming attractive again!



R. Scholz et al., “Update on IHP open source PDK initiative” FSiC2024

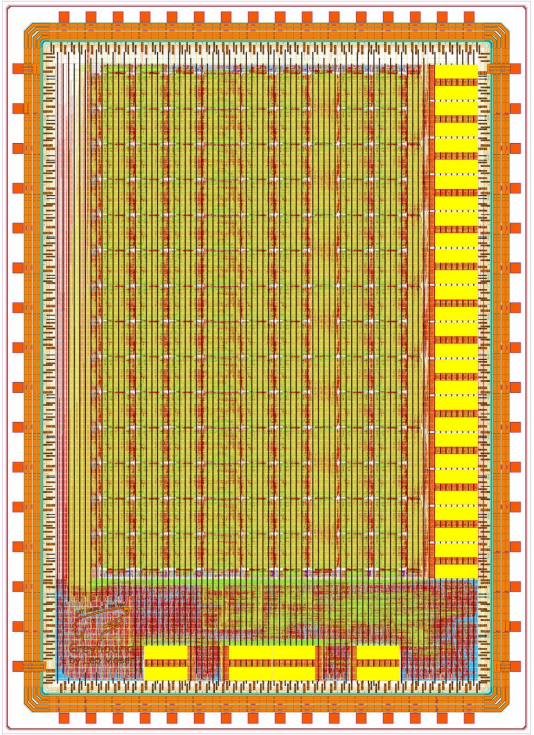
What’s Greyhound?

Greyhound: A RISC-V SoC with tightly coupled eFPGA

- RISC-V core: CV32E40X
- eFPGA fabric: FABulous
  - Custom instruction extension, custom peripheral or standalone FPGA
- Implemented with LibreLane!
- IHP Open PDK:
  - SG13G2 130nm BiCMOS
  - SG13CMOS 130nm CMOS
- Manufactured at IHP’s pilot line

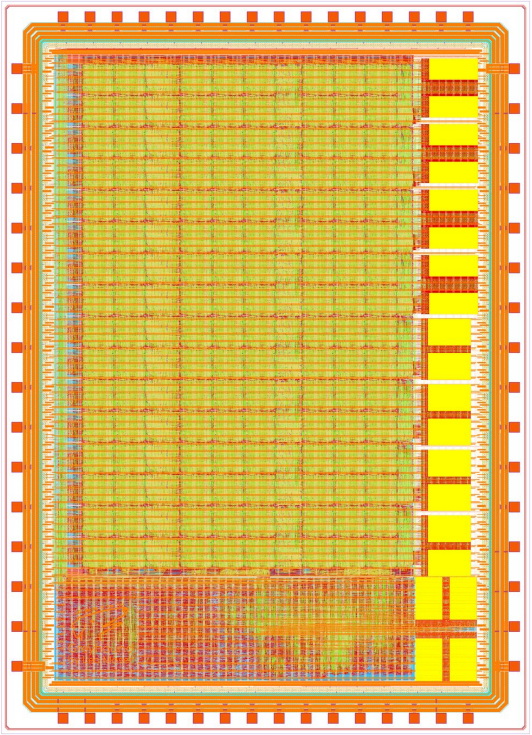
Open Source: https://github.com/mole99/greyhound-ihp

Greyhound v1



07 April 2025, SG13G2

Greyhound v2



14 September 2025, SG13CMOS

Greyhound v1

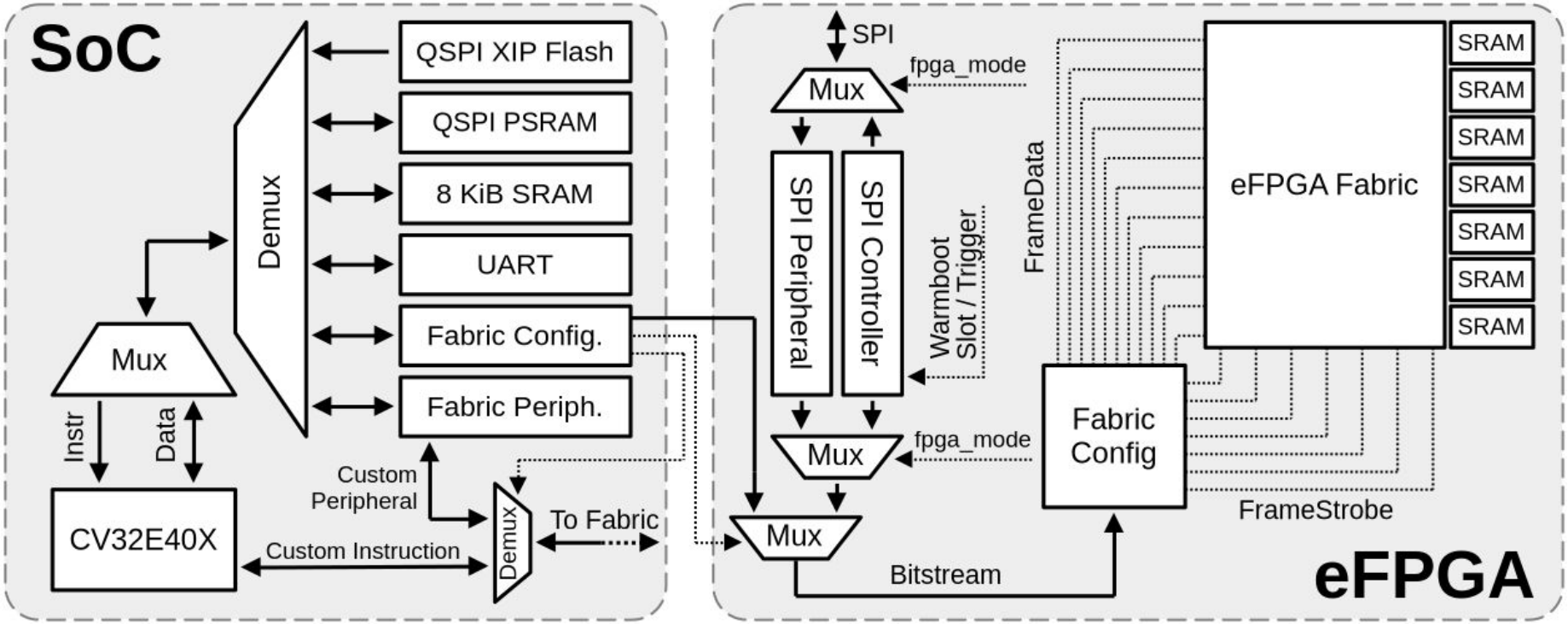
Greyhound v2

- CV32E40X (RV32IMA)
  - 8 KiB SRAM
  - QSPI Flash controller for XIP
  - QSPI PSRAM controller
  - Highly configurable UART
  - Fabric Peripherals

- Cache: 8 lines of 32 bytes, direct mapped
- 784× LUT4 + FF
- **7**× SRAM (32×1024, 1RW)
- 7× MAC
- 14× Register file
- 4× CPU_IF (XiF, Peripheral)
- 1× WARMBOOT
- 32× I/Os

- Cache: **16** lines of 32 bytes, direct mapped
- **1024**× LUT4 + FF
- 4× SRAM (32×1024, 1RW)
- **4**× BRAM (16×1024, 2RW)
- **8**× MAC
- **16**× Register file
- **1**× OBI_PERIPHERAL
- **1**× CUSTOM_INSTRUCTION
- 1× WARMBOOT
- 32× I/Os

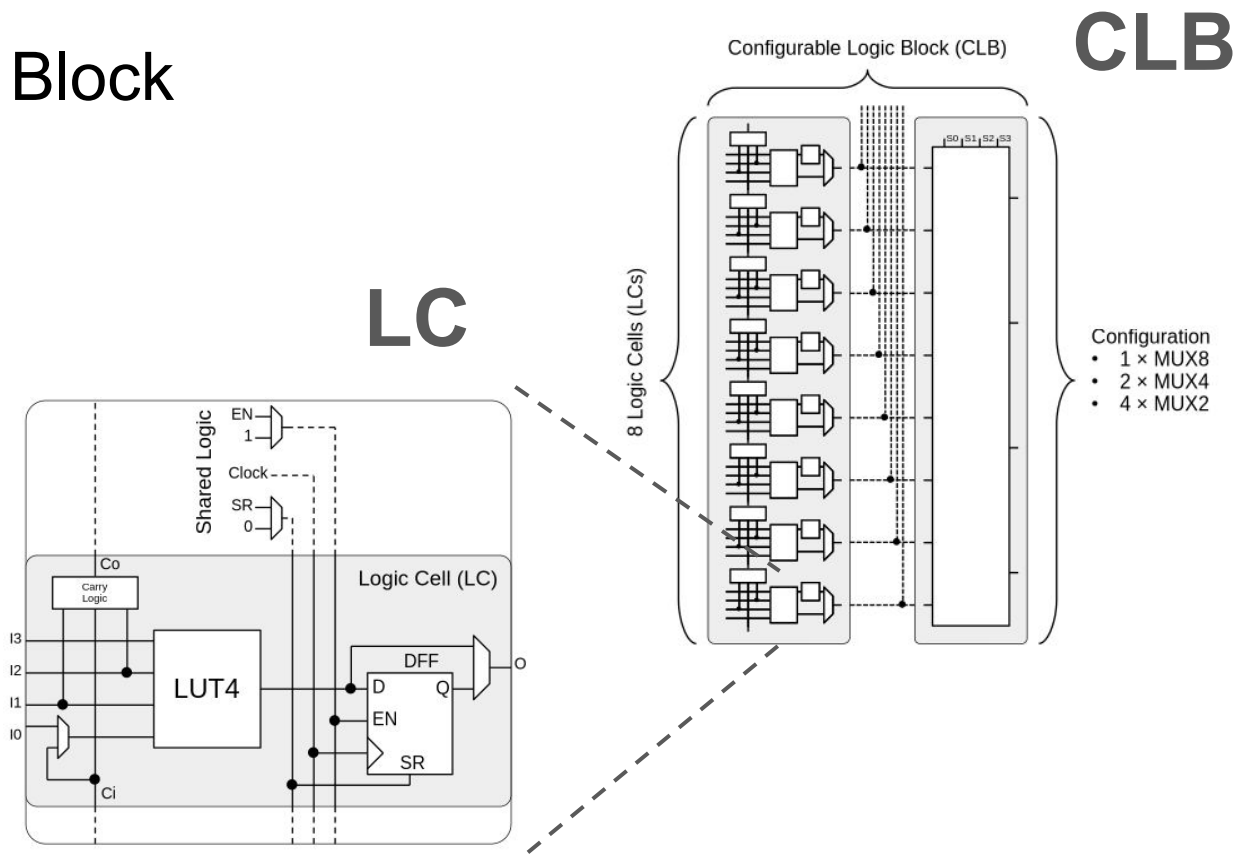
Top-Level Block Diagram



Configurable Logic Block

- One CLB consists of
  - 8 Logic Cells
  - 1 Multiplexer

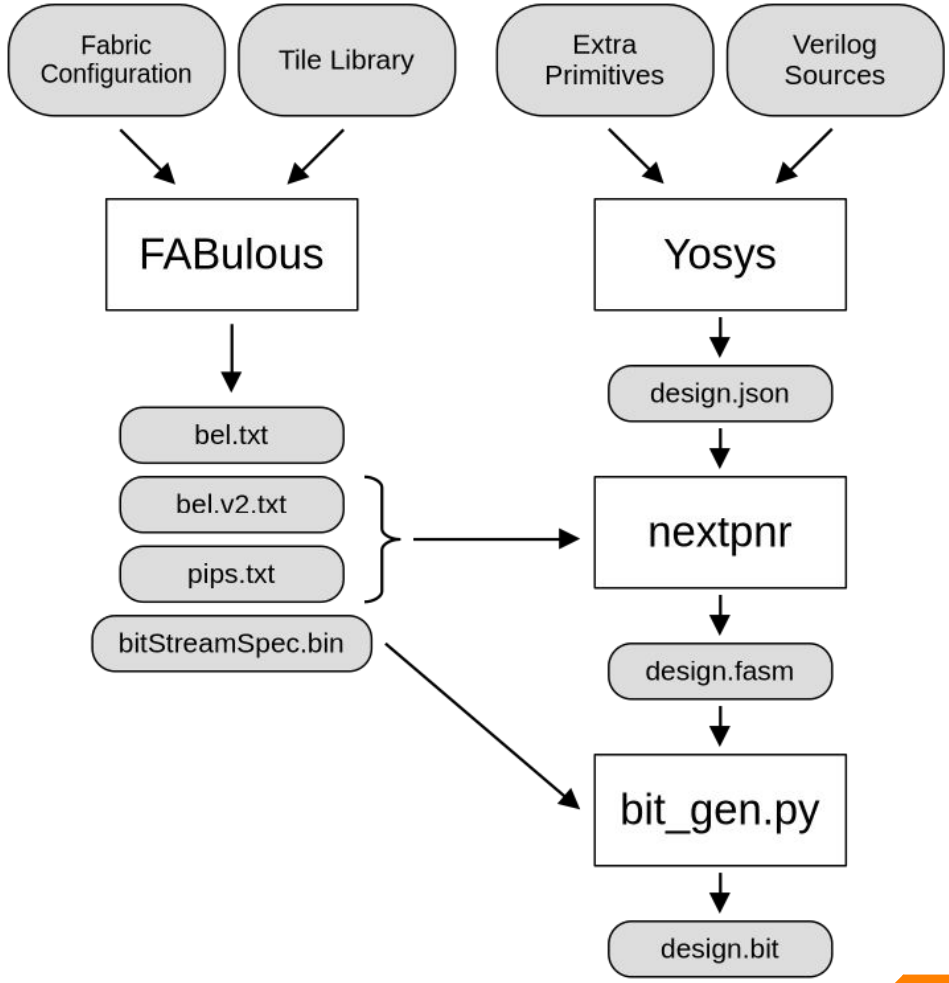
- One LC consists of
  - Carry chain
  - LUT4
  - D-FF
  - Shared Logic



User Designs

- Yosys & nextpnr toolchain
- + fasm python package
- RISC-V designs
  - QERV (4-bit variant)
  - FazyRV (1-bit variant)

	LC usage	
FPGA	**QERV**	**FazyRV**
Greyhound	720	754
iCE40 UP5K	709	634



Verification

Design Verification

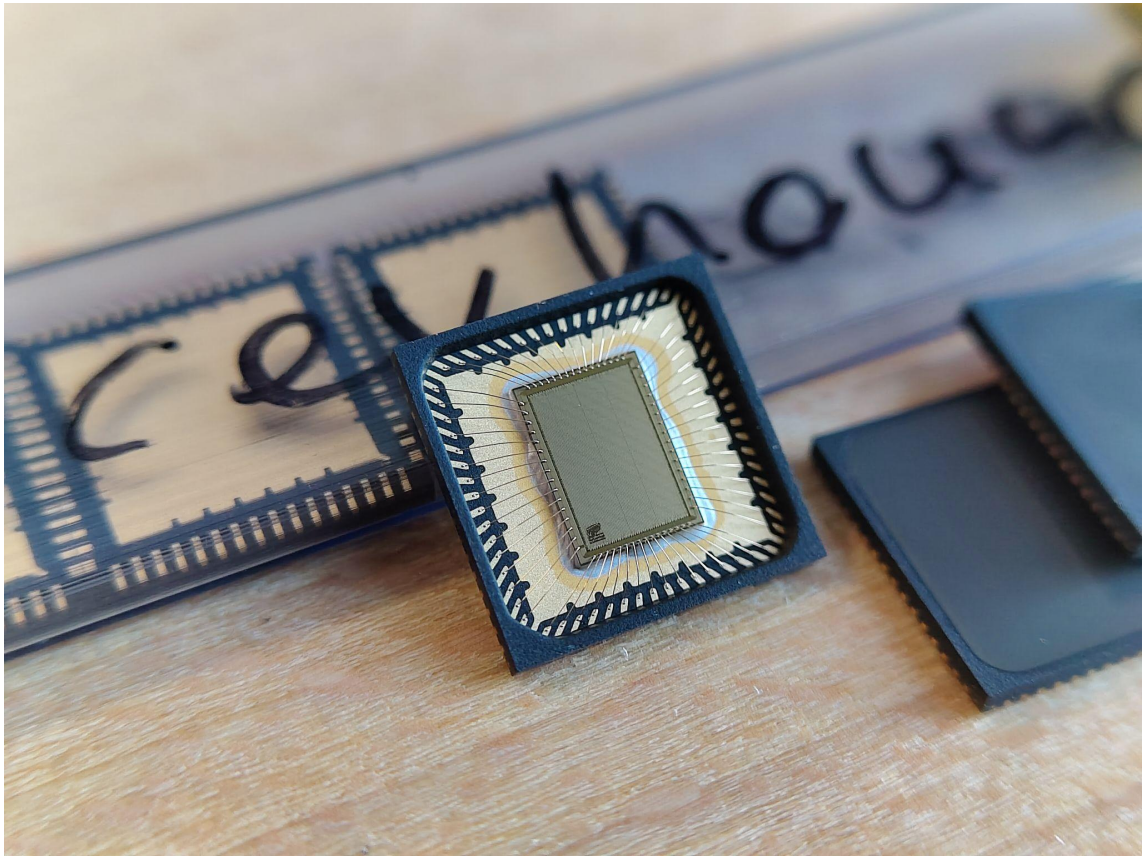
- Testbenches with cocotb!
- Simulations:
  - SoC on its own ✅
  - Fabric on its own ✅
  - Chip top-level ✅
- LibreLane
  - LVS ✅
  - DRC ✅

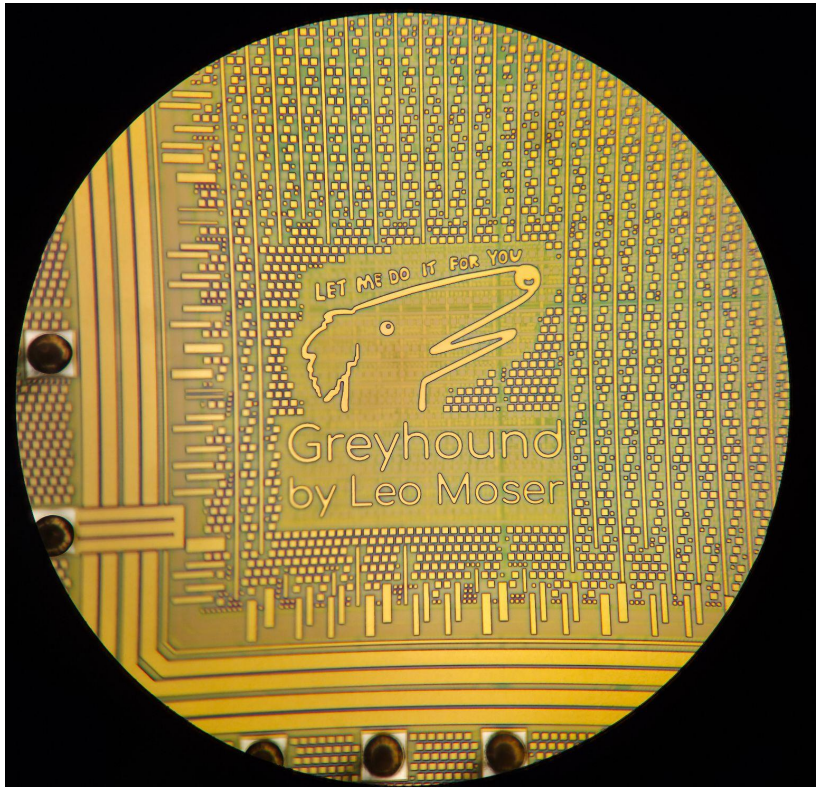
	frequency	
corner	**v1**	**v2**
nom_fast_1p32V_m40C	85 MHz	69 MHz
nom_typ_1p20V_25C	55 MHz	51 MHz
nom_slow_1p08V_125C	34 MHz	32 MHz

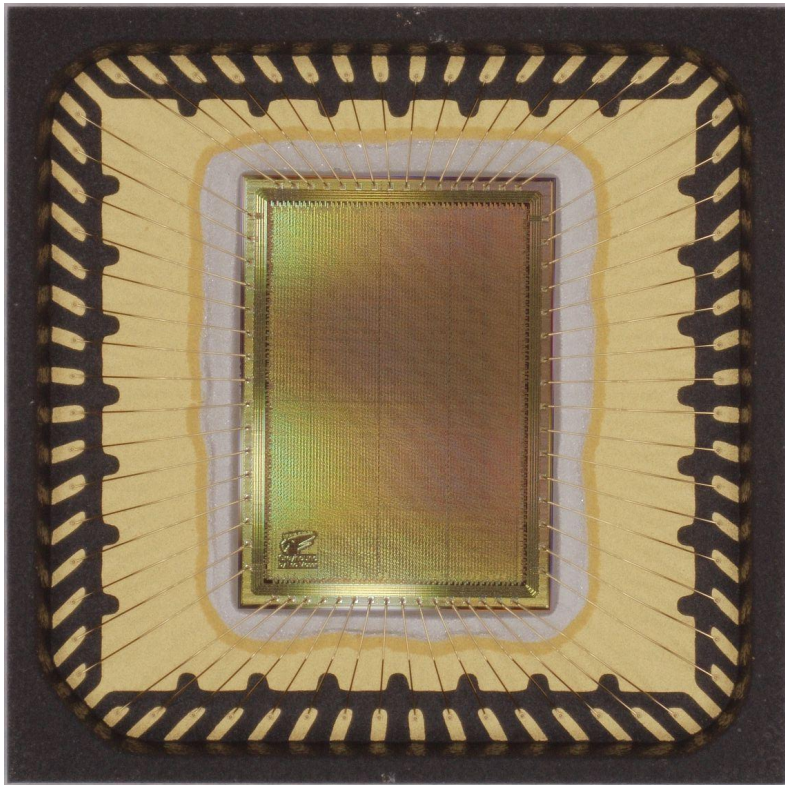
STA results for the SoC

Open Source Silicon

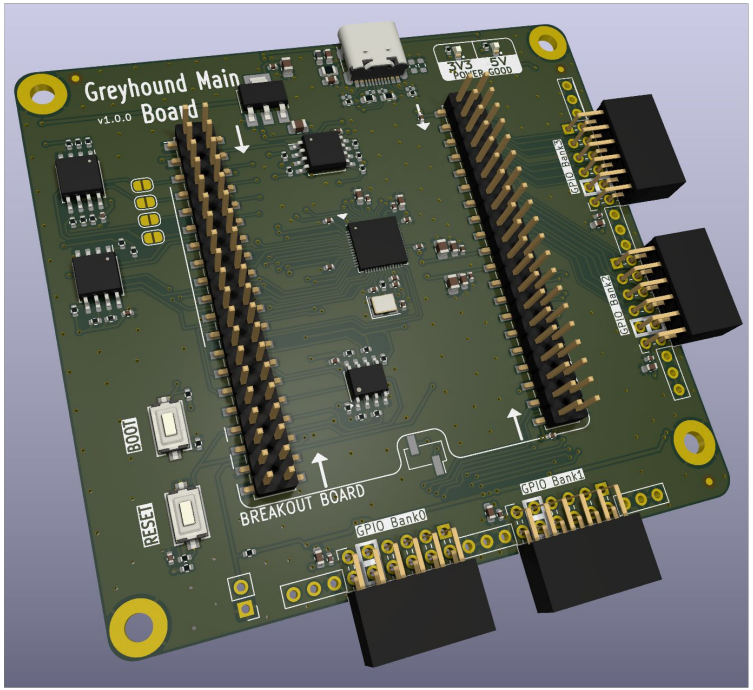
Greyhound v1



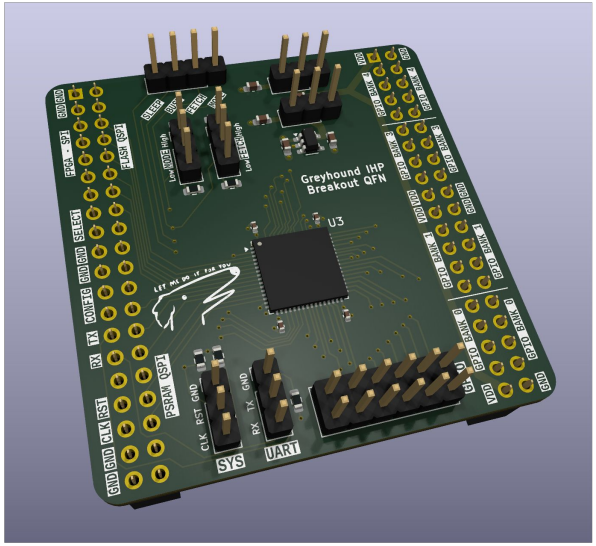

LET ME DO IT FOR YOU
Greyhound
by Leo Moser



Greyhound Main Board



Greyhound Breakout PCB



The Future of Greyhound

- Future revision?
  - Fabric:
    - More clock domains
    - Timing annotation
  - DFT:
    - Scan chain insertion
  - JTAG:
    - 2 TAPs (core and fabric)
    - Debug support via GDB and OpenOCD
    - Integration by Stefan Huwar

Excited about the future!

Questions?

https://github.com/mole99/greyhound-ihp

Extra Slides!

Tiny Tapeout FABulous Fabric