SCIENCE · PASSION · TECHNOLOGY

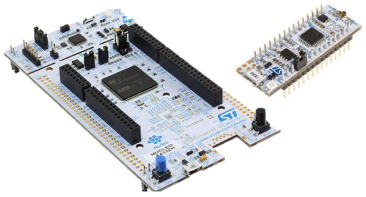
TU Graz

Open Thesis / Project

Software-based error mitigation strategies for embedded memories

Motivation

As a consequence of the ongoing digitalization, trust and reliability within embedded memories are becoming evermore important. A fundamental aspect to increase a memories' reliability are methods and concepts, which allow a memory to autonomously detect and resolve its soft errors. Most mitigation strategies are realized using additional hardware chips, consequently increasing memory's cost, processing speed and die-area. Thus, incorporating HW-based strategies into existing automation solutions usually requires the redesign of the whole system. Better option are software-based solutions (error correction and detection codes or software redundancy). Software solutions usually lead to a decrease of available memory as well as an increase of computation time, access time, and complexity of the overall system. This thesis explores available software-based mitigation strategies, their implementation on real CPUs, measure their performances and compares them in order to define and find a trade-offs as well as decent solution for a COTS CPUs.



Target Group

Students in ICE/Telematics and Comp. Science.

Thesis Type

Bachelor Thesis / Master Project.

Goals and Tasks

- Overview of the exiting software-based mitigation strategies
- Implementation of different strategies on real CPUs
- Measurements and comparison of performances (overheads, speed, complexity, etc) between strategies

Required Prior Knowledge

- Solid background in embedded systems
- Programming skills in C/C++
- Architecture of the embedded memories
- Interest in Fault-tolerant systems

Used Tools & Equipment

- Developing boards from STM
- C/C++

Contact Person

- Dr. Konrad Diwold
  kdiwold@tugraz.at
- Dipl.-Ing. Amer Kajmakovic
  amer.kajmakovic@pro2future.at

Institute for Technical Informatics
Networked Embedded Systems Group

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