Failure-In-Time Estimations through Hardware-Software Simulations

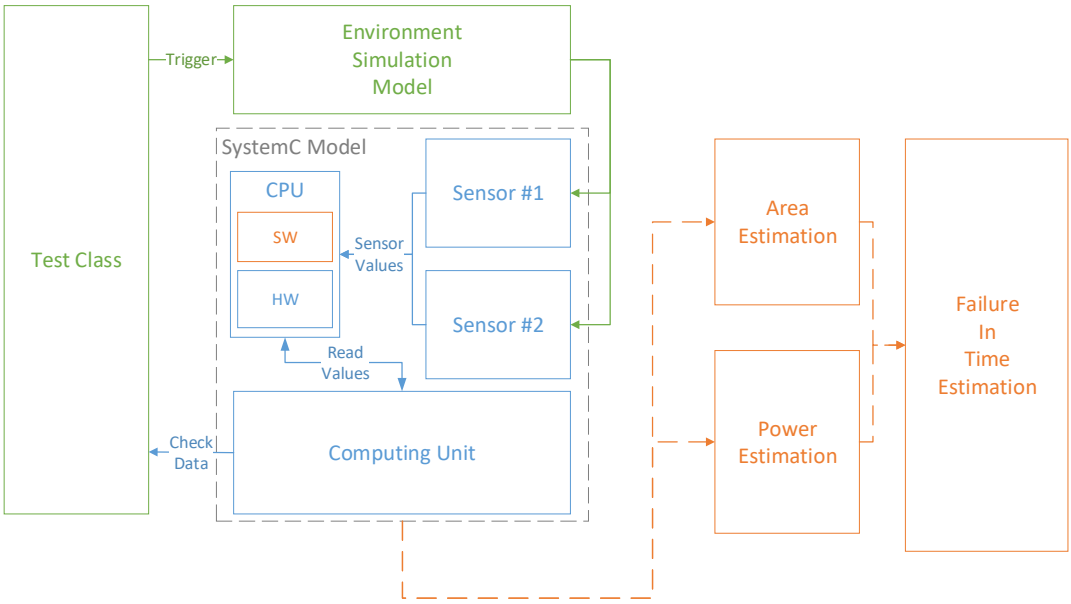

Figure 1: Concept overview Failure-In-Time estimations through Hardware-Software simulations in SystemC.

Description

The Failure-In-Time (FIT) Rate is an important safety indicator, especially for the component reliability. The FIT Rate describes the possible amount of failures in 1 Billion Operating hours and depends on the used materials and temperatures during operation. Nowadays, the FIT Rate is specified during the design phase but not evaluated through simulation models. Higher FIT Rates results in the need of more safety circuits, to decrease the FIT Rate, and this could lead to project delays.

For this purpose, we want to create a methodology to estimate the resulted FIT Rate of the system through a SystemC simulation model.

Tasks

- Literature Research
- Create SystemC Test Model
- Enable Area and Power estimation (e.g. Powersim Library)
- Derive Gate Equivalents
- Estimate Failure-In-Time Rate
- Documentation

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