Open Thesis / Project:

Exploring Open-Source FPGA Synthesis & P&R Toolchains for DPR

Motivation & Summary

With this project, we aim to enable dynamic partial reconfiguration (DPR) using fully open-source tools (Yosys for synthesis and nextpnr for place-and-route). DPR allows a portion of an FPGA to be reconfigured at runtime, but this capability is largely absent in today's open-source FPGA flows. This thesis will explore and extend the toolchain to support DPR on hardware platforms that have open-tool support (such as Lattice iCE40 or ECP5). Possible directions include developing methods to partition designs into static and reconfigurable regions, creating flows for partial bitstream generation, and demonstrating on-the-fly hardware reconfiguration. The focus is on using and improving open-source tools to build a reproducible DPR flow, with an aim to contribute these enhancements back to the community and achieve publishable results.

Recommended Prior Knowledge

- Digital logic design (Verilog/VHDL)
- FPGA architecture and tool flow fundamentals
- Open-source FPGA tools (Yosys, nextpnr)
- Partial reconfiguration concepts

Thesis Type

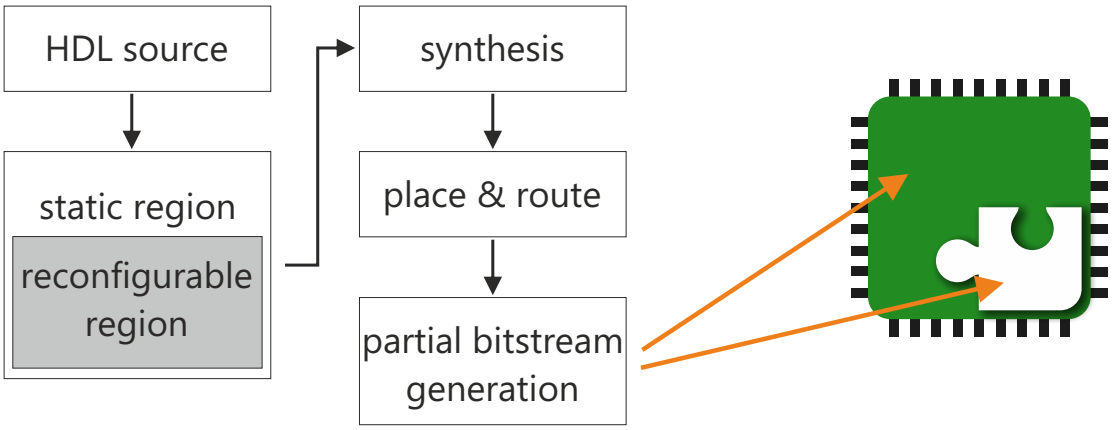
- Master's Project
- Master's Thesis

Student Target Groups

- Computer Science (CS)
- Information and Computer Engineering (ICE)

Goals & Tasks

- Analyze the current state of open-source FPGA flows and identify gaps for supporting DPR.
- Design a methodology to partition FPGA designs suitable for open-source tool flows.
- Extend or script the Yosys and nextpnr toolchain to generate partial bitstreams for a target open FPGA (e.g., Lattice iCE40/ECP5).
- Demonstrate DPR on hardware by implementing a proof of concept.
- Evaluate the DPR workflow in terms of performance and reliability, and contribute docs and/or code back to the open-source community.



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