Open Thesis / Project:

Generative AI Copilots for Enhanced Digital Hardware Design Workflows

Motivation & Summary

This thesis explores the use of generative AI code assistants (LLM copilots) to streamline digital hardware design (RTL/FPGA/ASIC) workflows. By leveraging open-source code generation models adapted specifically to hardware description languages, developers can automate and improve tasks such as Verilog module generation, linting, and design documentation. This thesis will explore setting up a self-hosted AI copilot environment, fine-tune the model on domain-specific data, and integrate it into the hardware development pipeline. Finally, the effectiveness of the AI copilot must be evaluated in terms of productivity gains and design correctness.

Recommended Prior Knowledge

- Hardware Description Languages (Verilog/SystemVerilog)
- Basics of Machine Learning (neural networks, language models)
- FPGA/ASIC design flow (synthesis, simulation, verification)
- Programming skills (for model fine-tuning)

Thesis Type

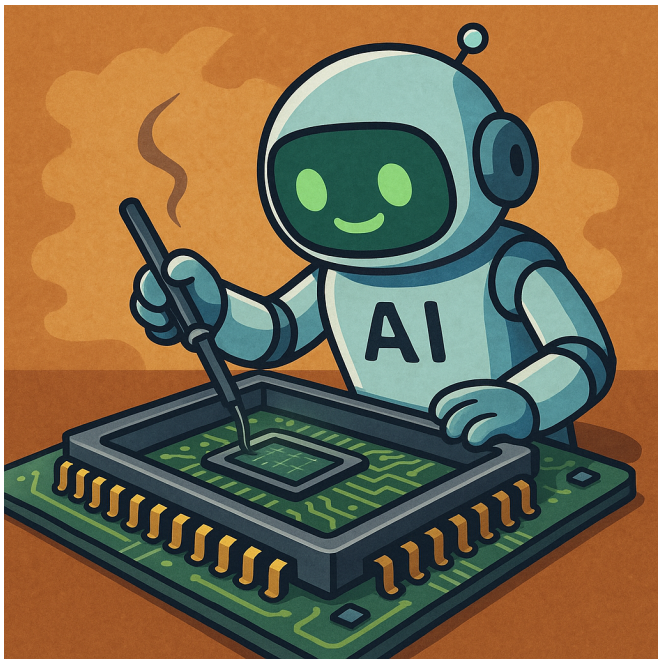
- Bachelor's Thesis
- Master's Project
- Master's Thesis

Student Target Groups

- Computer Science (CS)
- Information and Computer Engineering (ICE)
- Electrical Engineering (EE)

Goals & Tasks

- Deploy a suitable open-source code LLM in a self-hosted environment.
- Fine-tune the model on domain-specific hardware design data (HDL code and documentation).
- Integrate the AI copilot into an RTL/FPGA design workflow (e.g., as an IDE plugin or CLI tool).
- Demonstrate the copilot on tasks like Verilog generation, code linting, or synthesis optimization.
- Evaluate the impact on development productivity and design correctness.



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