Open Thesis / Project:

Runtime-reconfigurable RISC-V MCUs

Motivation & Summary

Dynamic Partial Reconfiguration (DPR) enables on-demand specialization of embedded RISC–V cores by swapping accelerator logic at runtime while the CPU keeps running. This thesis studies how DPR improves flexibility, performance, and energy efficiency in FPGA/eFPGA-based systems. You will design a standardized socket between the static pipeline and reconfigurable regions using instruction-set extension interfaces (custom instructions/CSRs), and prototype swappable accelerators for a dedicated usecase (e.g., crypto, DSP). The work spans hardware, software, and tool flow: partial bitstreams, reconfiguration control, and driver/runtime integration.

Recommended Prior Knowledge

- FPGA design, ideally with DPR concepts
- Processor architecture, preferably RISC–V
- Verilog/SystemVerilog

Thesis Type

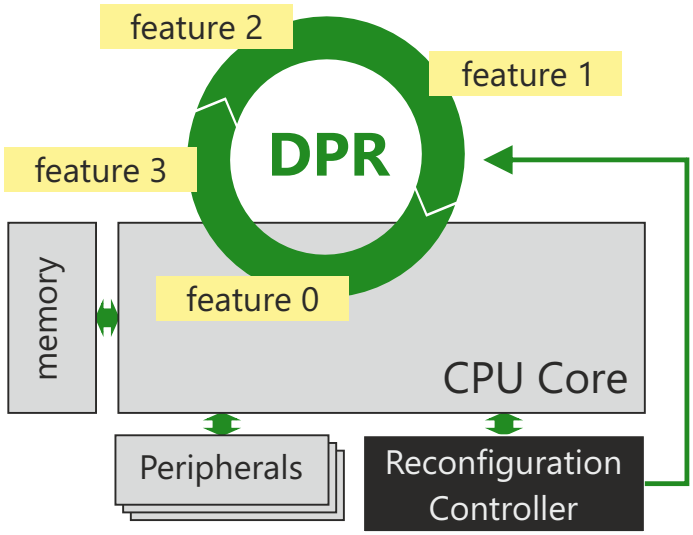
- Bachelor's Thesis
- Master's Project
- Master's Thesis

Student Target Groups

- Computer Science (CS)
- Information and Computer Engineering (ICE)
- Electrical Engineering (EE)
- Space Sciences and Earth from Space (SSES)

Goals & Tasks

- Specify a standardized extension interface between the static and DPR regions.
- Prototype your CPU system in an FPGA.
- Implement DPR functionality.
- Evaluate performance/energy/area/latency vs. static designs; provide open, reproducible artifacts.



Contact & Information

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