Open Thesis / Project:

Greyhound v2 – Improve an Open-Source RISC-V SoC with eFPGA

Motivation & Summary

Greyhound is an open-source RISC-V SoC that tightly couples an embedded FPGA (eFPGA) fabric and was built entirely using open-source frameworks (the FABulous eFPGA generator and OpenLane/LibreLane ASIC flow). It demonstrates how on-chip reconfigurable logic can serve as a custom instruction extension or a flexible peripheral for the processor. Building on this baseline, this thesis will explore a next-generation eFPGA-enabled SoC in the open-source silicon ecosystem. Possible directions include improved CPU–FPGA interfaces, tighter integration of the eFPGA fabric with the SoC, and physical design optimizations for timing closure and power efficiency. The focus is on using open-source tools and flows to ensure reproducible chip generation, with an aim for publishable results.

Recommended Prior Knowledge

- Digital design (Verilog/SystemVerilog)
- Processor architecture (RISC-V, SoC integration)
- FPGA/eFPGA fundamentals
- Basic ASIC design flow (e.g., OpenLane/OpenROAD)

Thesis Type

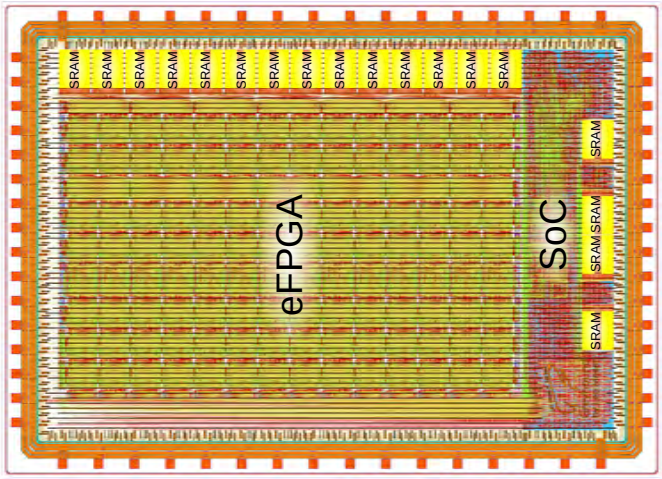
- Master's Project
- Master's Thesis

Student Target Groups

- Computer Science (CS)
- Information and Computer Engineering (ICE)
- Electrical Engineering (EE)

Goals & Tasks

- Extend the Greyhound SoC or design a new RISC-V + eFPGA SoC using the FABulous framework.
- Implement improved custom instruction or peripheral interfaces for the eFPGA.
- Achieve tighter integration between the eFPGA fabric and SoC subsystems.
- Optimize the eFPGA tile layout and SoC floorplan.
- Explore advanced open-source ASIC flows and eFPGA architecture enhancements (new standard cells, OpenROAD/LibreLane improvements, adding BRAM/DSP tiles) to improve performance and reproducibility.



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