Open Thesis / Project:

RISC-V MCU with a Runtime-Reconfigurable Datapath

Motivation & Summary

Runtime reconfigurability of Field-Programmable Gate Arrays (FPGAs) is a mechanism to modify a digital design while it is running. Microcontroller Unit (MCU) architectures like the *more*MCU use a pre-defined interface between the static pipeline portion and dynamically reconfigurable partitions to add new logic. The scope of this work goes one step further: We want to create an MCU where the datapath bit width can be changed during runtime. To do so, we want utilize different flavors of the scalable FazyRV core and add the possibility to interchange those flavors at runtime.

Recommended Prior Knowledge

- FPGAs
- Verilog/SystemVerilog
- RISC-V

Thesis Type

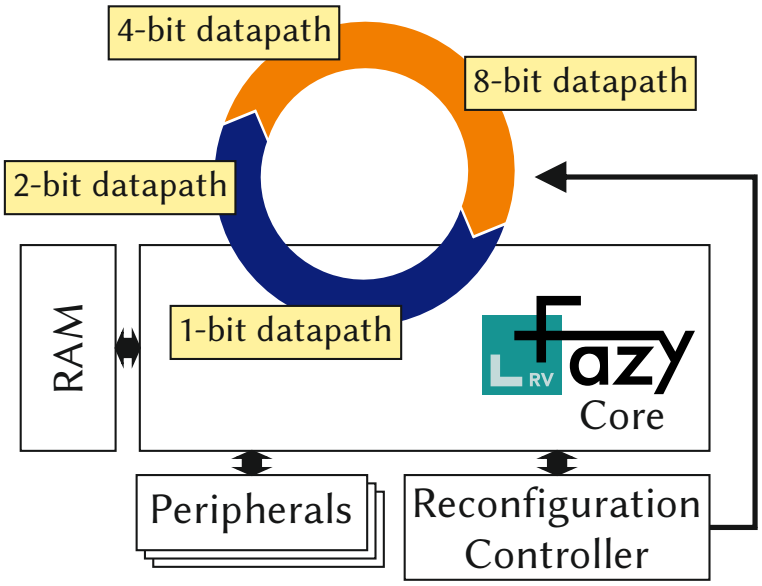
- Bachelor's Thesis
- Master's Project
- Master's Thesis

Student Target Groups

- Computer Science (CS)
- Information and Computer Engineering (ICE)
- Electrical Engineering (EE)
- Space Sciences and Earth from Space (SSES)

Goals & Tasks

- Setup the MCU architecture
- Setup the runtime reconfigurability
- Design the static reconfigurability interface
- Implement the funtionality to exchange the datapath at runtime



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