SCIENCE ▪ PASSION ▪ TECHNOLOGY

Open Thesis / Project:

Extend our Scalable FazyRV RISC-V Core

Motivation & Summary

FazyRV is a scalable minimal-area RISC-V core for low-workload tasks and the IoT. It allows scaling the data path to a width of either 1, 2, 4, or 8 bits at synthesis time and trade area vs. performance. In addition, users can find the best-fitting configuration and trade-off for their system requirements and technology by exploring FazyRV's manifold variants. This project gives you the possibility to extend FazyRV, evaluate your modifications, and bring your improvements upstream.

Recommended Prior Knowledge

- Field-Programmable Gate Arrays (FPGAs)
- Processor Architecture, ideally RISC-V
- Verilog/SystemVerilog
- FPGA basics

Thesis Type

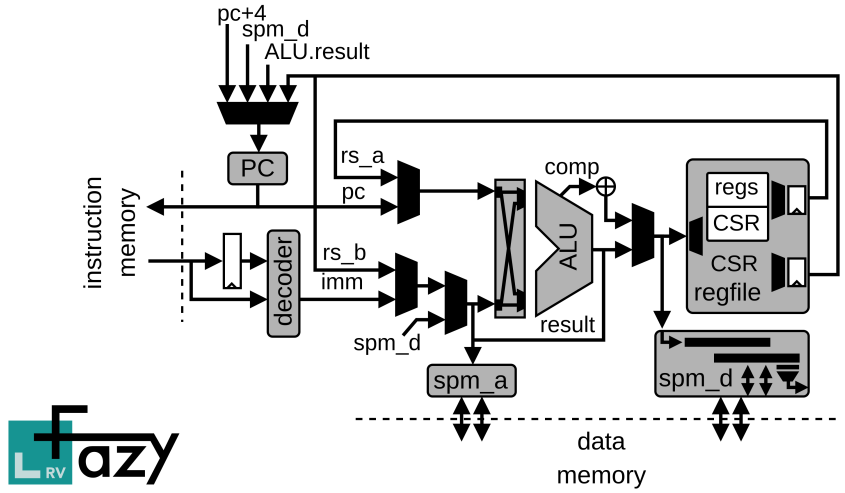
- Bachelor's Thesis
- Master's Project
- Master's Thesis (starting point, contribute your own ideas)

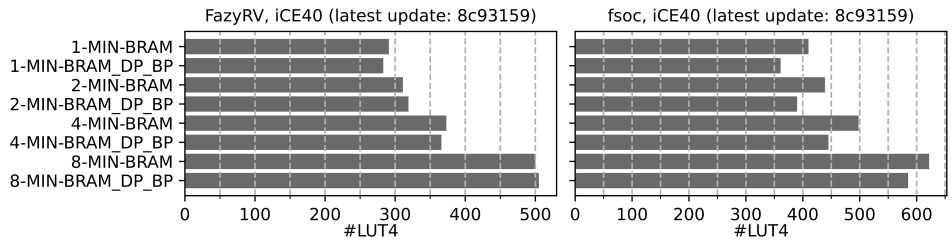
Student Target Groups

- Computer Science (CS)
- Information and Computer Engineering (ICE)
- Electrical Engineering (EE)
- Space Sciences and Earth from Space (SSES)

Goals & Tasks

- Extend FazyRV
- Implement features like compressed instructions, ...
- Improve the tooling
- Verify and evaluation your modifications





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