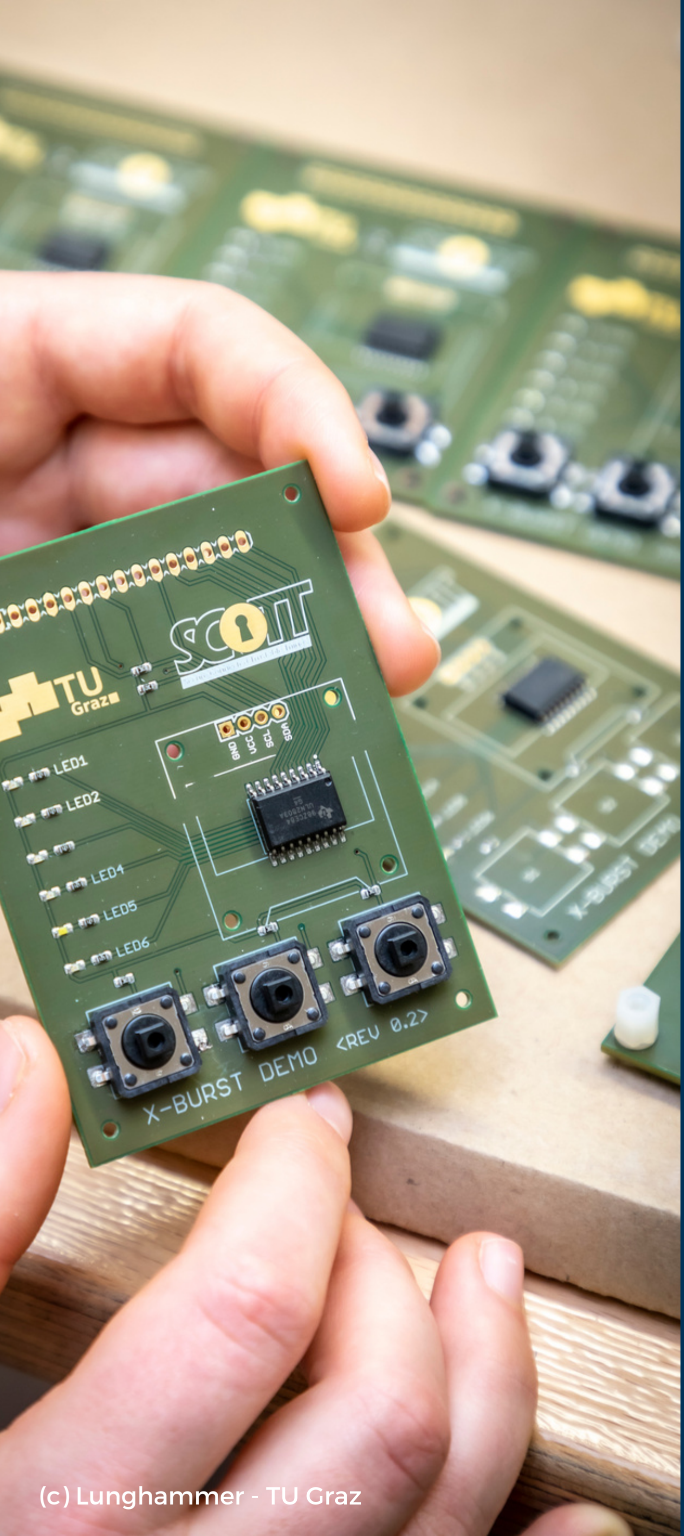
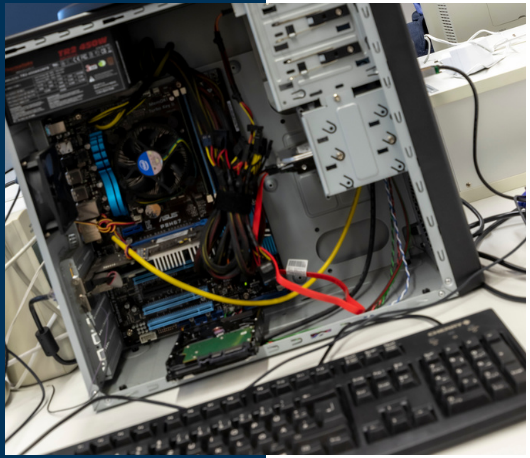


TU Graz

OPEN TOPICS FOR PROJECTS, BACHELOR AND MASTER THESES

SS 2022

Institute of Technical Informatics



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INSTITUTE OF TECHNICAL INFORMATICS

We offer research and education on modern networked embedded systems (such as Internet of Things and Cyber-Physical Systems) with focus on software, hardware, and networking. Our working groups make significant contributions to improve dependability, real-time properties, safety security, and efficiency of these systems to enable novel applications.

We are involved in numerous collaborations with industry partners. Besides funded research projects, we also collaborate directly with industry, for example by jointly supervising masters and PhD theses.

The education focus is on foundations of Computer Engineering, Real-time systems, Distributed Systems, Functional Safety, and Pervasive Computing. The Institute significantly contributes to the courses of study in Information and Computer Engineering (previously Telematics), Electrical Engineering, Informatics, and Software Engineering.

RESEARCH GROUPS

Network Embedded Systems

The Networked Embedded Systems working group investigates design, implementation, and test of sensor networks, Internet of things, and Cyber-Physical Systems with special emphasis on networking and software engineering aspects.

HEADED BY PROF. KAY RÖMER

Embedded Automotive Systems

The Embedded Automotive System group investigates the design, implementation, and test of operating systems, multi-core architectures, and wireless networks within the automotive domain.

HEADED BY PROF. MARCEL BAUNACH

Hardware / Software-Codesign

The HW/SW codesign group deals with embedded systems, HW/SW codesign, and power awareness.

HEADED BY ASS. PROF. CHRISTIAN STEGER

Industrial Informatics

The Industrial Informatics group is tightly cooperating with industry to tackle the needs and challenges in technology, process improvement, and new compulsory standards.

HEADED BY DR. GEORG MACHER

NETWORKED EMBEDDED SYSTEMS GROUP

Modern embedded systems typically consist of multiple computers that are connected by a wireless or wired network. Sensor networks, Internet of Things, Cyber-Physical Systems are all examples of this type of technology. The Networked Embedded Systems working group, headed by Prof. Dr. Kay Römer, investigates design, implementation, and test of such systems with special emphasis on wireless networking (Assoc.Prof. Carlo Alberto Boano), sensing and embedded machine learning (Assoc.Prof. Olga Saukh), and cognitive embedded systems (Dr. Konrad Diwold).

Typical challenges that need to be tackled are the openness and dynamicity of such systems, resource and energy constraints, harsh environmental conditions, and the need for dependable operation despite these difficulties. The working group focuses on experimental research, where concepts are transformed into realistic prototypes that are used in experiments to assess the properties and performance of the concepts.

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@ Prof. Kay Römer
roemer@tugraz.at

Research Area 1: Dependable Wireless IoT Systems

Networks of low-power wireless sensors and actuators are becoming an integral part of our daily life: hidden in our homes, cities, and cars, worn on our wrists, integrated in our clothes. They are a fundamental building block of the Internet of Things (IoT) and therefore need to operate efficiently and reliably. The research activities in the "Dependable Wireless Embedded Systems" group aim to analyze and improve the performance of low-power wireless technologies and protocols used to build present and future IoT systems, with the ultimate goal of increasing their dependability and real-world applicability.

We are always looking for highly motivated and brilliant students interested in doing a project or thesis on our research topics. We typically define the concrete topic after a short meeting with the student, in order to adjust the project/thesis to their interests and skills.

Assoc. Prof. Carlo Boano
cboano@tugraz.at

Examples of Available topics

- Detecting and Mitigating Coexistence Problems through RF Spectrum Analysis
- Benchmarking the Performance of UWB Platforms under Wi-Fi 6E Interference
- Centimeter-Accurate Navigation of Nano-Drones using UWB Technology
- Generating Repeatable Wi-Fi 6E Interference Patterns using Intel's AX210
- Integrating QUIC into the Contiki OS
- Bringing a full BLE 5.2 Stack to tiny Embedded Devices using Contiki-NG
- Towards a Battery-Free Internet of Things

Contacts

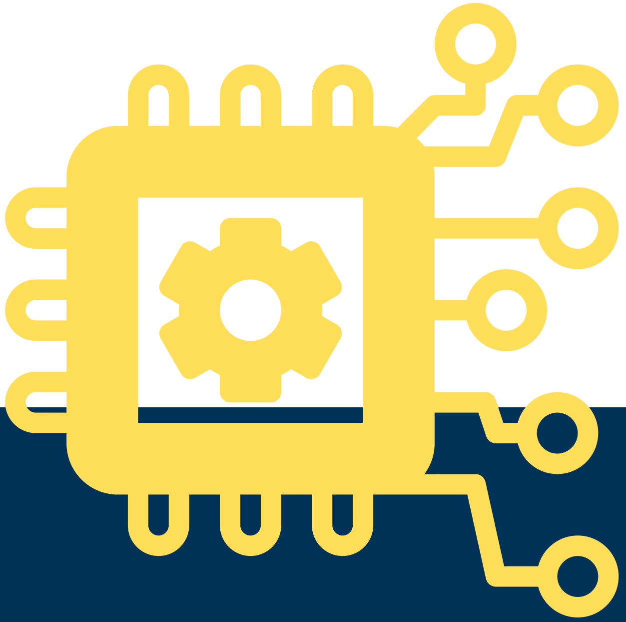
- **Assoc. Prof. Carlo Alberto Boano (cboano@tugraz.at) [Group Leader]**
- Markus Schuß (markus.schuss@tugraz.at) [Focus on Benchmarking IoT Systems]
- Rainer Hofmann (rainer.hofmann@tugraz.at) [Focus on Cross-Technology Communication]
- Michael Stocker (michael.stocker@tugraz.at) [Focus on Ultra-Wideband Localization]
- Max Schuh (schuh@tugraz.at) [Focus on Ultra-Wideband Communication]
- Hannah Brunner (hannah.brunner@tugraz.at) [Focus on Harvesting / Sustainable IoT Systems]
- Elisabeth Salomon (elisabeth.salomon@tugraz.at) [Focus on Dependability in the Cloud Continuum]
- Pei Tian (tian@tugraz.at) [Focus on Efficient & Reliable LoRa Networks]
- Markus Gallacher (markus.gallacher@tugraz.at) [Focus on Jamming Detection and Mitigation]

Today a wide range of sensors integrate with IoT devices to measure their surrounding contexts. As the number of integrated sensors and their complexity grows, so are the amounts of data they produce and the need for this data to be processed. The state-of-the-art computational models that, for example, recognize a face, detect events of interest, track user emotions, or monitor physical activities are increasingly based on deep learning principles and algorithms. Unfortunately, deep models typically exert severe demands on local device resources, and this conventionally limits their adoption within mobile and embedded platforms.

Our group works on new sensing concepts based on machine learning models, and on solving the challenges when running machine learning models on resource-scarce embedded devices.

We are always looking for highly motivated and brilliant students.

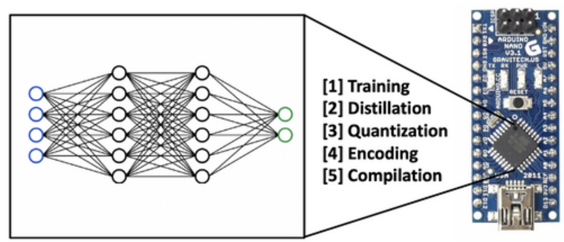
Assoc. Prof. Olga Saukh
saukh@tugraz.at



Research Area 2: Embedded Information Processing

Examples of Available topics

- Application-specific privacy for shared sensor data (contact papst@tugraz.at)
- Sparse inference for embedded deep learning (contact papst@tugraz.at)
- Distributed training with local partial updates (contact entezari@tugraz.at)



TinyML

Contacts @

- Assoc. Prof. Olga Saukh (saukh@tugraz.at) [Group Leader]
- Rahim Entezari (entezari@tugraz.at) [Focus on embedded deep learning]
- Franz Papst (papst@tugraz.at) [Focus on privacy and robustness in IoT data]
- Cao Nguyen Khoa Nam (cao.nam@tugraz.at) [Focus on environmental sensing]

Research Area 3: Cognitive Products and Production

Bringing cognition into products requires dependable and low-cost sensing, networking, and software platforms. These building blocks will allow the design and realization of cognitive products, where the “cognition” denotes a products ability to adapt and its functionality across the across the whole product lifecycle in order to maximize customer satisfaction, product quality and sustainability, and to minimize production overheads. Within this area we study and investigate technological building blocks required for future products and production systems and demonstrate their applicability by realizing case studies of cognitive products.

We are always looking for highly motivated and brilliant students.

Dr. Konrad Diwold
kdiwold@tugraz.at

Available topics

- Waste monitoring & augmentation in recycling processes (contact konrad.diwold@pro2future.at)
- Digital Twins as enabler for future safety automation (contact amer.kajmakovic@pro2future.at)

Contacts

@

- **Dr. Konrad Diwold (kdiwold@tugraz.at / konrad.diwold@pro2future.at) [Group leader]**
- Dr. Jesus Pestana (jesus.pestana@pro2future.at) [Focus on drone control & vision]
- Amer Kajmakovic (amer.kajmakovic@pro2future.at) [Focus on Automation and Safety]
- Katarina Milenković (katarina.milenkovic@pro2future.at) [Focus on Semantic web and ML]
- Daniel Kraus (daniel.kraus@pro2ufuture.at) [Focus on RF system design]
- Elisei Ember (Elisei.ember@pro2future.at) [Focus on wireless communication]
- Vignesh Manjunath (vignesh.manjunath@pro2future.at) [Focus on EAS]
- Tanveer Ali Ahmad (tanveer.ali-ahmad@pro2future.at) [Focus on EAS]

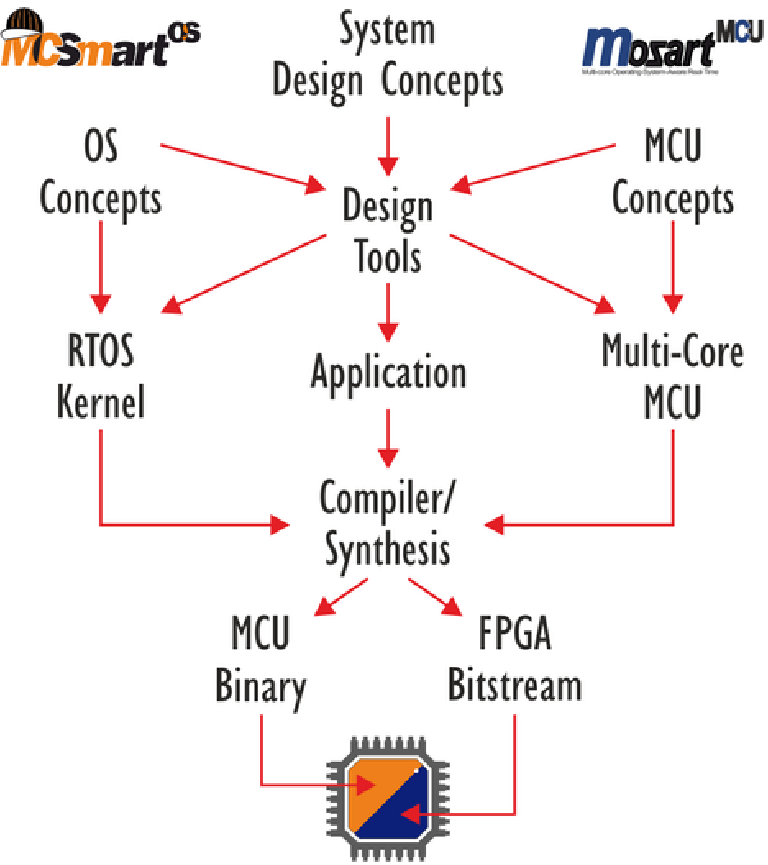
EMBEDDED AUTOMOTIVE SYSTEMS

The EAS group aims on fundamental and applied research in highly dependable embedded systems with mixed real-time demands.
Examples include electronic control units for smart, networked and autonomous vehicles, advanced robotics, or the Internet of Things.

These application domains are also expected to bring forth the most disruptive core technologies for the next decade. Considering the design, implementation, test, and maintenance of such systems, a holistic view on the hardware (processor architectures), software (operating systems/applications), and networks (interfaces) reveals a large variety of exciting challenges and projects.

@
Prof. Marcel Baunach
baunach@tugraz.at

Research Area 1: Hardware / Embedded Processor Architectures



This area offers the opportunity to get a deep understanding in the design and implementation of MCU architectures, including single-core and multi-core as well as FPGA-based soft cores (e.g., RISC-V) and standard ASICs (e.g., Aurix, ARM, etc.):

- Hardware accelerators for application-specific processors
- Code and logic synthesis in hardware and software
- Self-reconfiguring logic & partial reconfiguration at runtime
- Special hardware support for low-level software (OS)
- Security and resource sharing for multi and many-core
- MCU self-supervision and runtime profiling
- Design of flexible hardware/software interfaces

Keywords: MCU/FPGA, HDL, C/C++/Scripting, RISC-V/mosartMCU

Open topics

Self-modifying Processors:

Tomorrow's hardware will be updatable similar to today's software.

> Support us in developing processors that can change their own logic and features in case of bugs or new requirements.

Hardware support for OS features:

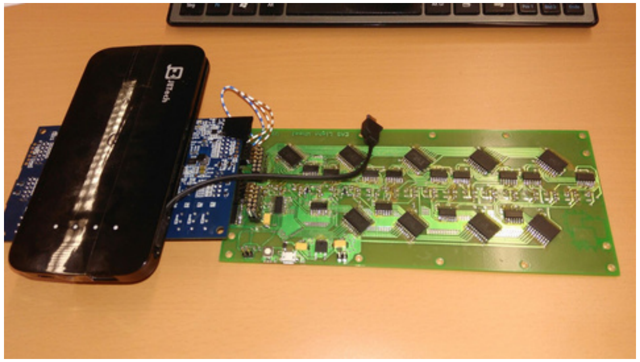
Future basic software and processors will be tailored to each other.

> Work together with experienced OS developers to accelerate kernel features through novel hardware concepts.

Optimization of processor runtime characteristics in software:

Software has a significant impact on various runtime characteristics of the hardware.

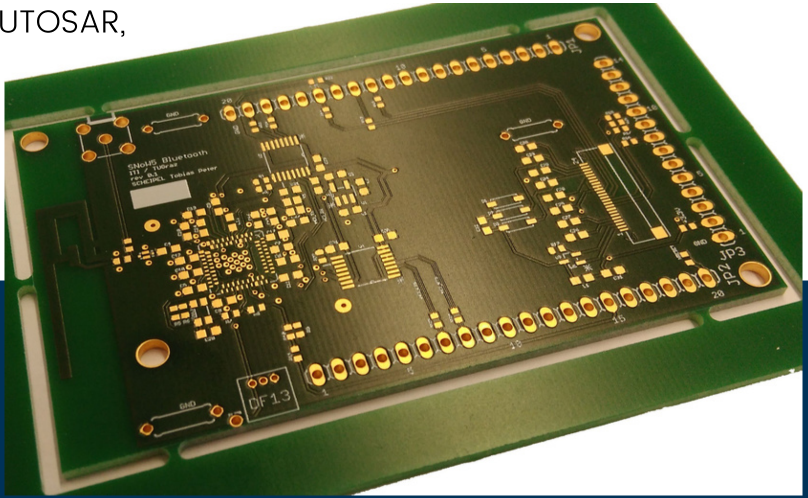
> Support us in understanding the effects in detail and optimize software to reduce energy consumption, avoid power peaks and cross-core implications, or optimize temperature profiles



This area allows you to dig deep into operating systems kernels and basic software concepts for embedded real-time systems. Support us in creating a versatile kernel or work closely together with our partners to develop new concepts for various application domains:

- Design and implementation of a novel embedded operating system
- Multi-core concepts and software partitioning for handling dynamic workloads
- Support for self-reconfigurable processors
- Model based OS development for automatic porting to various MCU architectures
- Verification concepts for OS kernels and low-level software
- Automatic interfacing of synthesized hardware extensions
- Basic software and systems generation for automotive and IoT applications

Keywords: C/C++/Assembly/Scripting, formal methods, MCSmartOS/AUTOSAR, MCU/FPGA, IoT/ADAS/CPS



Research Area 2: Software / Embedded Operating Systems

Open topics

Contribute to MCSmartOS:

MCSmartOS is the basic software developed by the EAS Group for research and teaching. It supports preemptive multitasking and various features for developing complex applications for different hardware platforms (e.g., RISC-V). A previous version of SmartOS is used in the automotive industry and a more recent version is used in embedded systems onboard of a rocket of the ASTG. As a next step, we seek to provide a new implementation as open-source.

› Become part of the team and contribute your ideas and expertise to our kernel, services, drivers, ...

Provably correct and portable System Software:

System software like OS kernels or drivers provide the base for complex applications on plenty of target architectures. To guarantee their correctness and availability for new (or even reconfigurable) processors, we work on special design and implementation concepts. This includes modeling and formal verification of code and requirements, like timing, security, liveness, energy, etc.

› Support our team and external experts in implementing system software that is provably correct

Dynamic Composition of Embedded Systems:

Future embedded systems for robots, vehicles, etc. will contain complex application software that is composed of tens or hundreds of components. These components are independently developed and tested, but need to coexist on few hardware platforms and interact dependably in any situation and under all circumstances.

› Involve yourself in developing new concepts to modularize systems and prove their correctness.

Contacts

MORE TOPICS FOR BOTH RESEARCH AREAS CAN BE TAILORED TO YOUR INTERESTS.

JUST CONTACT US!

Depending on the topics, theres can also be offered within industry cooperation projects.

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- Tanveer Ali Ahmad (tanveer.ali-ahmad@pro2future.at)

HARDWARE / SOFTWARE-CODESIGN GROUP

The HW/SW codesign group at the Institute for Technical Informatics deals with embedded systems, HW/SW codesign, and power awareness. The design of embedded systems can be subject to many different types of constraints, including timing, security, power consumption, reliability, and cost.

- Ass. Prof. Christian Steger (steger@tugraz.at) [Group leader]
- Markus Feldbacher (m.feldbacher@tugraz.at)
- Fikret Basic (basic@tugraz.at)
- Gernot Fiala (gernot.fiala@tugraz.at)

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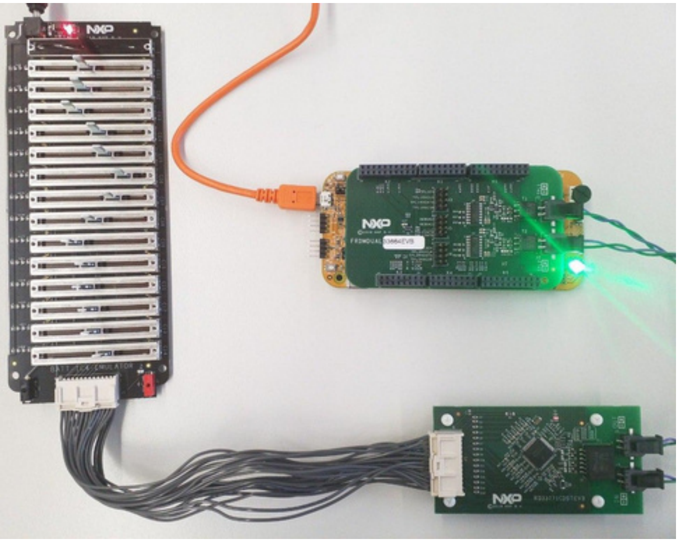
SEAMAL BMS

Security-related Topics in the domain of Battery Management Systems

in cooperation with NXP Semiconductors



Battery Management Systems (BMS) are control systems present in many safety-critical environments, e.g., in vehicles, where they are used to monitor the health status, as well as the load/unload of battery cells. They present a relatively new and open research field. TU Graz, together in cooperation with NXP Semiconductors, is interested in devising novel solutions in the area of module communications, i.e., switching from wired to wireless technology, anti-counterfeiting authentication solutions, security provisioning, and secure logging handling.

This opens many new possibilities, which include wireless updates and configurations, better sensor coverage, easier module maintenance, deployment in distributed architectures, etc.

The goal is to allow the integration of new communication technologies while at the same time ensuring the protection of the BMS data confidentiality, integrity, and authenticity.

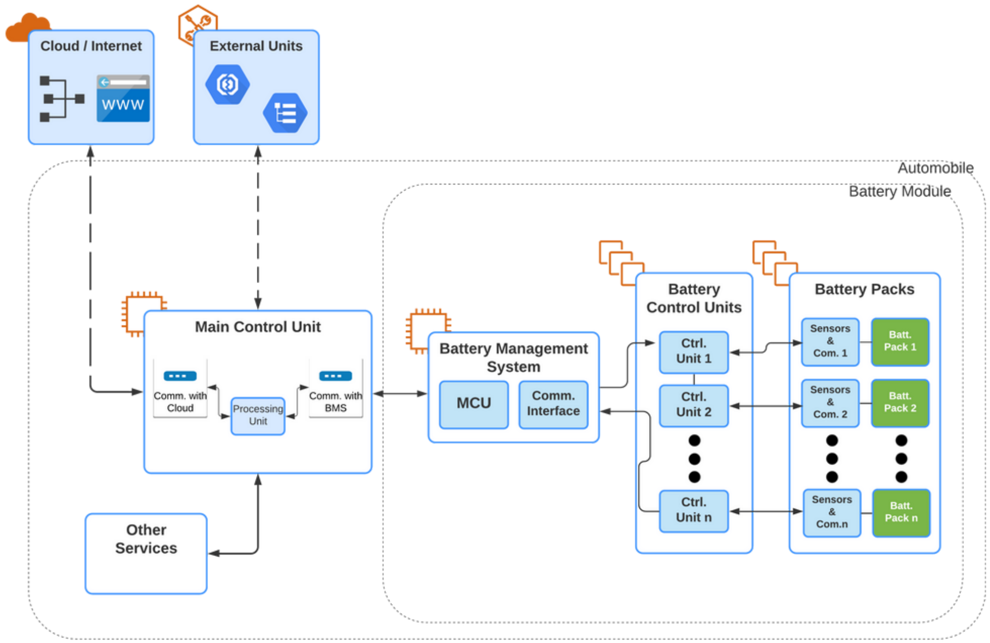
@

Ass. Prof. Christian Steger

Fikret Basic

Project topics

- Hardware and software extensions utilizing SE for providing security solutions for BMS
- BMS security architecture as part of an in-vehicle environment



Contacts

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- Ass. Prof. Christian Steger (steger@tugraz.at)
- Fikret Basic (basic@tugraz.at)

Autonomous drones have to be aware of their surroundings in order to avoid unintentional interaction with them. To achieve this, they have to sense their environment at a very high resolution to detect trees, branches, electric lines, and the various other low-altitude occlusions that occur in the real world. In the future, it might be a common sight to see autonomous drones flying beyond the visual line of sight (BVLOS) in very low-level (VLL) airspace.

Ass. Prof. Christian Steger
Felix Warmer

The ADACORSA project is working on functionally safe sensors and sense-and-avoid systems that should aid drones in achieving such challenging tasks. Designed with low weight, size, and cost in mind, the sensors and systems are intended for drones flying in very low-level airspace.

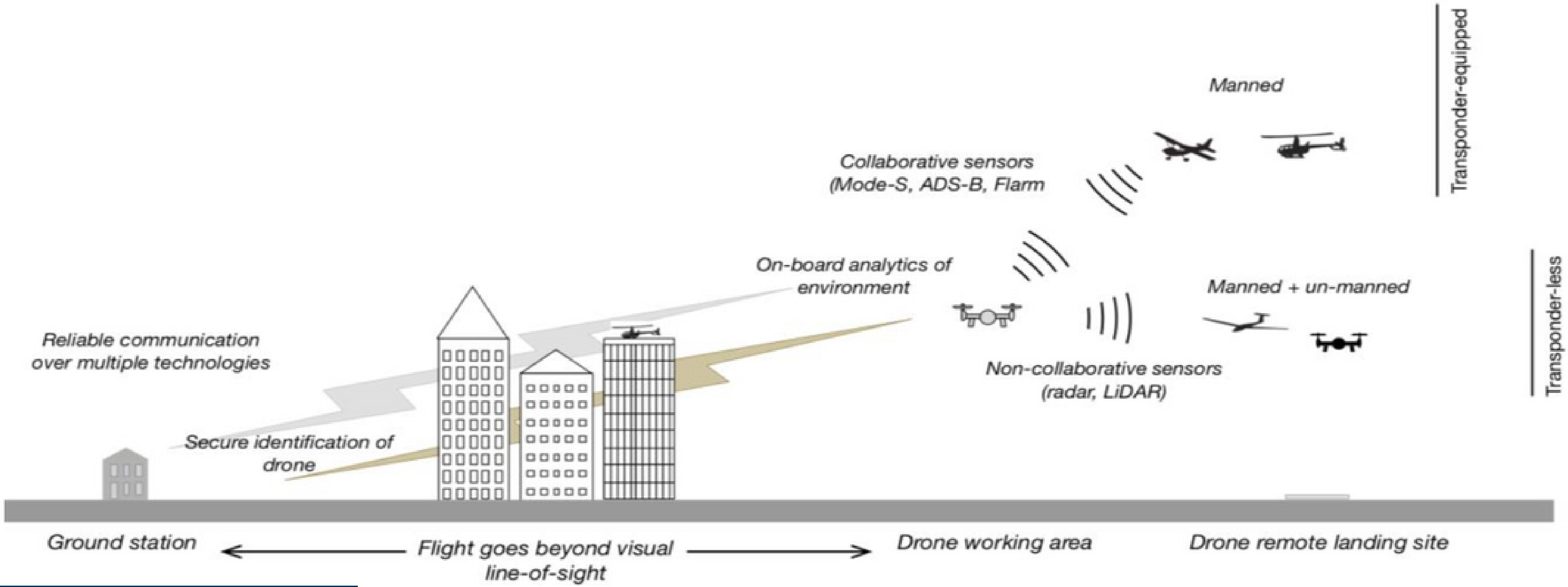
ADACORSA

Airborne data collection on resilient system architectures

ADACORSA

Project topics

- Using disparate Sensors for detection of erroneous Sensor Data
- Compensating Single Sensor failure through Secondary Sensory Data



Contacts

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- Felix Warmer (warmer@tugraz.at)

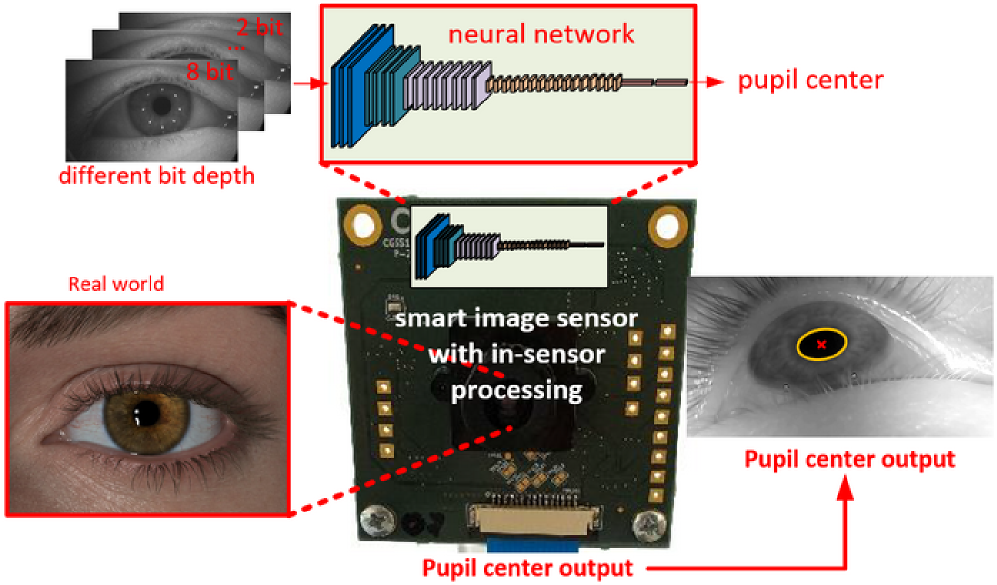
Sensor SoC

SoC topic in the area of image processing

in cooperation with ams-OSRAM AG

Embedded image processing and analysis close to the image sensor is gaining more and more momentum since it allows to reduce required communication bandwidth to the next layer of the processing hierarchy. This saves energy and enables significant efficiency improvement for different use cases.

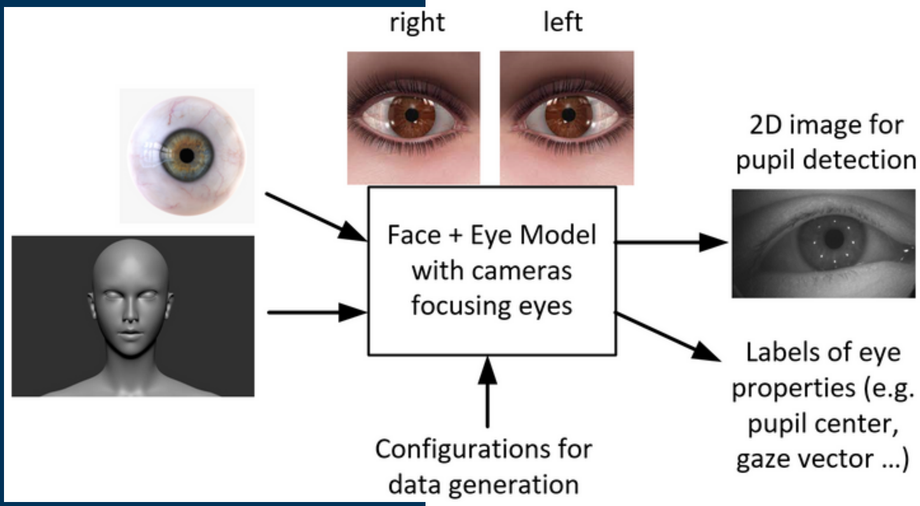
Here, the focus is on pupil detection for AR/VR applications, which is integrated into a smart image sensor with limited resources. Image processing in a smart image sensor not only comes with benefits but also includes technical challenges regarding processing time, area, and power.

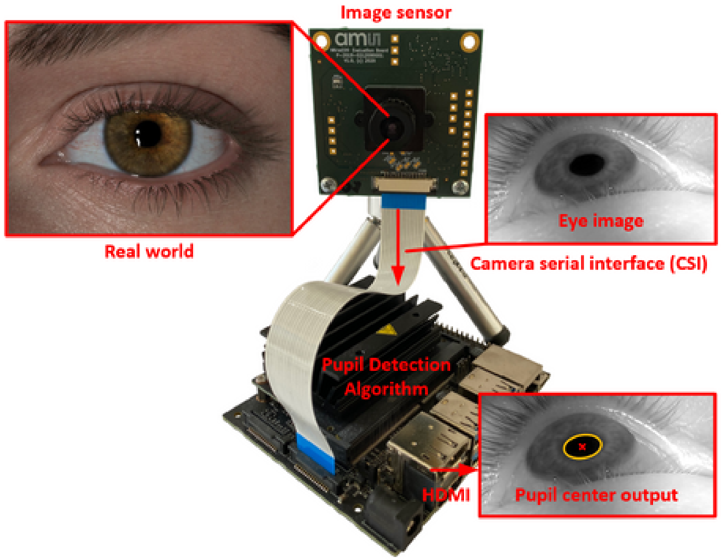


Ass. Prof. Christian Steger
Gernot Fiala

Project topics

- Accuracy analysis of a Neural Network for Pupil Detection with different input bit depth
- 3D Face/Eye Model for automatic training/test data generation
- Mira220 Evaluation Kit power measurement of a pupil detection algorithm





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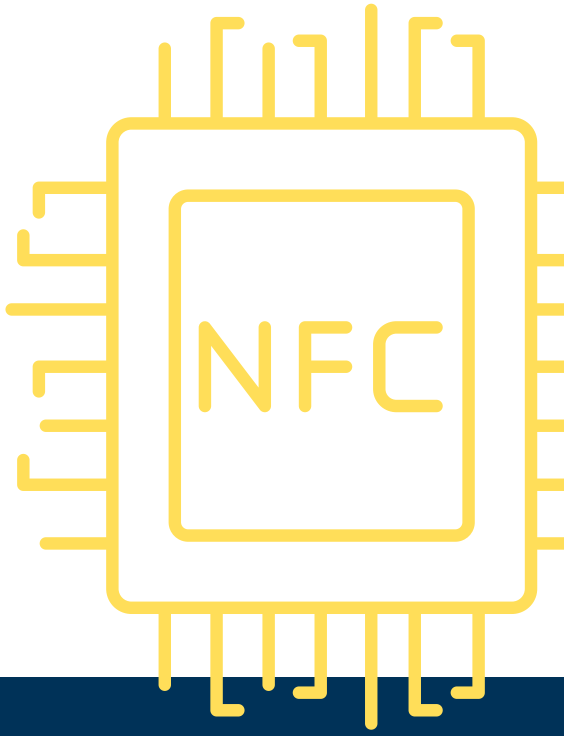
- Gernot Fiala (gernot.fiala@tugraz.at)

Near Field Communication (NFC) is a ubiquitous technology with many applications, ranging from identification to ticketing, from mobile payment to logistical solutions, and, just recently, wireless charging. A considerable amount of analog and digital signal processing is required on all NFC integrated circuits to achieve high performance and reliable communication, keeping costs of engineering and manufacturing still profitable.

One way to balance chip-resources with the growing need for flexibility is to consider the adoption of RTL microprocessors (softcores) able to perform DSP instructions. As opposed to more specialized signal processing made with custom digital logic, a DSP softcore provides the wanted flexibility at the cost of potentially higher resource usage, in particular program and data memory. Additionally, higher clock rates might be required to meet the end-application performance, which has an impact on the operative power consumption, as well as on the customer's adoptability of the offered solution.



Ass. Prof. Christian Steger
steger@tugraz.at

RISC-V

Adoption of DSP softcores for NFC Signal Processing

in cooperation with NXP Semiconductors

Research Topics

Of particular interest for this work will be the identification of any design requirement in terms of HW/SW partitioning, algorithms & architectures, DSP performance requirements in various operative modes, overall logic demand, clock rates, and power estimations. This exploration will be supported by the analysis of the (Matlab) models describing the existing solution. Supported by a mentor, the student will therefore have the opportunity to span over different disciplines, such as:

- Computer Architectures and Digital Signal Processing
- System Modeling & HW/SW Partitioning
- FW Development and Verification
- Digital Logic Design and Verification

We are looking for a student in the field of computer science, electrical engineering, software engineering, or similar and with:

- Academical background (if not also experience) in DSP theory and practice (e.g., in Matlab/Simulink)
- Understanding of computer architectures
- Microprocessor or DSP programming in C/C++
- An understanding of digital circuits design, HDL and verification techniques

Contacts

- Ass. Prof. Christian Steger (steger@tugraz.at)

Chip-Design

in cooperation with semify e.U. www.semify-eda.com

Topic 1: Automatic Error Pattern Detection for SoC Register Verification based on UVM Register Model

Nowadays, the Universal Verification Methodology (UVM) is the de facto standard for verification environments used to verify today's System on Chips (SoC). Each SoC contains hundreds of configuration and status registers which require special attention during the verification process. A set of dedicated classes, called UVM RAL (Register Abstraction Layer), targets the verification of these registers. Although UVM RAL is indented to model and verify the implementation of registers it lacks support for error pattern analysis and debugging.

Target of the Master Thesis is to develop data, address and time aware algorithms for detecting common error pattern leading to a significant debug time reduction. The reporting needs to be done in textual and graphical ways. The algorithms should address common error pattern like bitfield misalignments and addressing issues. Additionally, the potential of using machine learning (ML) algorithms should be explored. The developed algorithm will be integrating into the existing ErrorAnalyzer environment.

@ Ass. Prof. Christian Steger
steger@tugraz.at

Topic 2: Quadratic equation accelerator for RISC-V cores

For many of today's Mixed Signal applications it is required to compensate the non-linear behavior of analog components by using interpolation methods. A quadratic approximation is often used to compensate for these nonlinearities. If microcontroller-based systems are used for such applications, it makes sense to implement the calculation of the quadratic equation in hardware (HW).

Moreover, certain applications also have the need to perform this quadratic interpolation in fast real time calculations (eg. within regulation loops) making in necessary to implement these functionality in dedicated HW.

Target of this project is to develop a HW accelerator for calculating quadratic equations whereas the same accelerator can be used by
a) the microcontroller
b) the dedicated HW used for real-time calculations

The target microcontroller is a RISC-V microcontroller allowing an easy and straight forward way to add custom specific instructions for performing the quadratic interpolation with a single instruction.

Ass. Prof. Christian Steger
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INDUSTRIAL INFORMATICS

The Industrial Informatics working group closely cooperates with industry to tackle the needs and challenges in technology, process improvement, and new compulsory standards. While the complexity increases in products and solutions for the automotive, automation, and IT domains, development cycle times continuously shrink. System development by singular domain specialists is no longer sufficient. Systems have to be engineered in integrated design processes across distributed supply chains, keeping track of changes in an agile manner. The group focuses on general functional viewpoints and system-wide feature thinking.

- Dr. Georg Macher (georg.macher@tugraz.at) [Group leader]
- Jürgen Dobaj (juergen.dobaj@tugraz.at)
- Dr. Michael Krisper (michael.krisper@tugraz.at)
- Thomas Krug (t.krug@tugraz.at)
- Matthias Seidl (matthias.seidl@tugraz.at)

@

Dr. Georg Macher
georg.macher@tugraz.at

Area: Communication Technologies for Distributed Embedded Real-Time Systems

- Task: Create a reliable industrial IoT communication system by utilizing smart contracts, arbitration, and network management tools.
- Task: Explore the integration of AI in safety-critical (autonomous) applications (e.g., driving, robots, manufacturing, drones, ...)
- Task: Build a demonstrator platform to evaluate distributed industrial control algorithms based on ARM/X86 processor architectures running real-time Linux.
- Task: Analyze and compare the features of modern industrial & automotive real-time network technologies (e.g., EtherCAT, Time-Sensitive Networking, TTEthernet, Profinet, Sercos III, ...).

Contacts @

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- Matthias Seidl (matthias.seidl@tugraz.at)

Area: Service-Based Automation of Critical Distributed Embedded Real-Time Systems

- Task: Build a demonstrator for industrial IoT (IIoT) systems with a miniature industrial system.
- Task: Explore the integration feasibilities of AI in safety-critical real-time applications for attack mitigation.
- Task: Build a real-time demonstrator of an IIoT system with runtime adaptation.
- Task: Analyze and compare industrial service-based approaches for the feasibility of application in a dependable industrial system context.

Contacts

- Thomas Krug (t.krug@tugraz.at)
- Matthias Seidl (matthias.seidl@tugraz.at)

Area: Risk Assessment and Expert Judgement

- Task: Develop an online platform for assessing and combining expert judgments.
- Task: Create a tool for efficient construction and calculation of risk graphs.
- Task: Design a method for deriving quantitative values from existing qualitative assessments to get realistic and comparable risk assessments.

Contacts

- Dr. Michael Krisper (michael.krisper@tugraz.at)

Area: Methods, Tools & Industrial Informatics Applications

- Task: Check/test the cybersecurity measures of a series embedded automotive system.
- Task: Built up a demonstrator of an automotive battery management system.
- Task: Improve an existing vehicle simulation tool for calculating CO2 emissions for heavy-duty vehicles and busses (VECTO).
- Task: Support in designing a Cyber-Security educational program.
- Task: Mining and describing best practices and patterns for industrial Cyber-Security, Safety, and Risk Estimation.

Contacts

- Dr. Georg Macher (georg.macher@tugraz.at)

Area: MacGyver Projects
Invent something extraordinary!

These topics are not bound to a specific industry project but can be freely explored to do something highly innovative and creative.
Either you come up with your own crazy or unusual ideas, or be inspired by some of ours:

- Task: Automotive Cyber Security: Hack a motorcycle dashboard
- Task: Automotive Cyber Security: Hack a blue-tooth stack implementation
- Task: Automotive Cyber Security: Hack a car, Hack some IoT device, break encryptions
- Task: Machine Learning/AI for Self-Driving Cars: Build (an AI-driven) self-driving toy car
- Task: Machine Learning/AI in Dependable Systems: Use your knowledge of AI for increasing safety and security of dependable systems.
- Task: Home Automation: Create some crazy home automation with IoT
- Task: Home Automation: Develop an IoT-cat-sitter system (Food and water spender)
- Task: WAP ("Wild-and-Provocative") Digitalization Project: Build a hardware demonstrator of your interest that evaluates/improves/changes/enhances the current state of industry practice and science.

Contacts @

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THANK YOU