Open Thesis / Project:
FPGA supported Speech Processing

Motivation & Summary
With the increasing complexity of speech processing algorithms in various application domains (e.g., mobile communication, assistive hearing devices, etc.) the demand for dependable implementations in terms of efficient and deterministic execution times rises as well. Therefore, speech processing algorithms are often designed and implemented in high level tools (e.g., Matlab) and later integrated into ASICs. However, with the availability of reconfigurable hardware (FPGA) in future devices, a much more flexible realization as application specific on-chip peripherals for embedded MCU architectures becomes feasible. The goal of this thesis is to design and implement a framework for implementing speech processing units for an existing MCU architecture based upon Matlab code. The thesis will be jointly supervised by the Institute for Technical Informatics and the Signal Processing and Speech Communication Lab.

Student Target Groups
- EE-Toningenieur / ICE / EE

Thesis Type
- Master Thesis or Master Project + Master Thesis

Goals and Tasks
- Extend existing soft core platform by ADC/DAC capability
- Design of a framework for implementing speech processing algorithms in hardware.
- Proof of concept & Evaluation

Recommended Prior Knowledge
- Basic knowledge in FPGA / HDL
- Basic knowledge in Matlab
- Basic knowledge in Signal Processing

Used Tools & Equipment
- Xilinx FPGA
- Matlab

Contact & Information
Marcel Baunach  baunach@tugraz.at
Pejman Mowlaee  pejman.mowlaee@tugraz.at
http://www.tugraz.at/en/institute/iti/teaching/open-theses/

Institute for Technical Informatics - Embedded Automotive Systems Group
Signal Processing and Speech Communication Lab