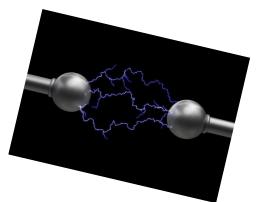


Graz University of Technology Institute of Electronics

IFE

# Master's thesis on Electrostatic Discharge



# **RF SEED (System Efficient ESD Design) modeling**

# **Motivation**

Cell phone RF front end and antenna circuit protection is the topic of this thesis. Systemlevel ESD robustness is a crucial design goal for any electronic system. To achieve the required level of robustness at the lowest cost a design concept is applied which assures matching between PCB protection components and IC IO behavior under system ESD discharge. It is now widely referred to as system efficient ESD design (SEED). A thorough characterization of the high current behavior of IO circuit and onboard protection elements provides the necessary data for a simulation based co-design of on-chip and on-board protection measures.

Predicting the system-level destruction threshold within an RF front-end of portable devices can increase the chance of achieving a "right first time" design which is of main importance for product manufacturers.

#### **Research topic**

Characterization of the high current behavior of RF front end components including antenna tuners, path section switches, LNAs, SAW filters and making their model and retrieving their damage threshold in order to provide the preliminary requirement of RF SEED simulation would be the scope of this project.

Basic experience of RF circuits is an advantage, basic knowledge in SPICE.

# Organizational matters

- Start: as soon as possible
- Workplace: at the institute of electronics

# Contact/Supervision



IFE: David Pommerenke (<u>david.pommerenke@tugraz.at</u>)