

Master Thesis

Implementation of a wafer-level soft switching setup for GaN power transistors

Background

This work is aiming for the development and implementation of a soft switching setup for GaN power devices fully based on wafer-level assessment.

Soft switching applications use typically a resonance in the circuit such that the power transistor is being discharged and its energy can be reused in the switching application. Thus, no energy is lost during switching and the power transistor does not see the harsh stress conditions that typically applies during hard switching. The work could explore two schemes of hard switching

- Soft switching by active components i.e. an active transistor turning on in parallel to the DUT
- (optional) resonant soft switching by passive components e.g. LC as energy storage as in typical resonant circuits

The setup should accommodate for in-situ characterization of the device including threshold voltage drifts i.e. measurement of the ID-VG, dynamic RDSon characterization, measurement of the gate and drain leakage currents, probing of potential at additional contact points e.g. Kelvin measurement points

The entire setup should be part of the existing hard switching wafer-level system at IFAT using a fully-automated wafer prober with existing test hardware, probe cards, test equipment, power supplies, oscilloscopes, HV pulser, and a self-written control software based on Python for operation.



Quick Info

Location: Villach, Infineon

Entry level: Master Thesis

Start: ~July 2021

Contract type: full time, temporary (9 to 12 months)

Job Description

During your thesis project, we expect you to become a growing expert for **electronic hardware (embedded software etc.) design**, with a strong focus on **soft-switching stress tests on wafer-level**. This means you will need to acquire some special knowledge and perform dedicated tasks:

- Learn about types and characteristics of **advanced power semiconductors**, especially GaN high-voltage devices
- Improve your skills in **power electronic hardware design, layout and circuit simulation**
- Further develop and implement the concept for an **automated wafer-level test system** together with your senior tutors (PhD students and senior engineers)
- Design, build and evaluate a working **hardware prototype**
- Document your results by writing and submitting your Master thesis

This position is subject to the collective agreement for workers and employees in the electrical and electronics industry. The **salary for this position is around €2200 gross p.m.** full-time

Your Profile

You are a **master student** covering the area of **(Power) Electronics (Informatics)** with a strong ambition for technology, **system (hardware/software) design** and making things work. You are also able to:

- Start right away, because you have completed most of your exams
- provide some knowledge and experience in **programming (Python) / HW design (μC)**
- work and communicate well with our international team in **English and/or German**
- provide relevant documents: CV, Bachelor certificate, transcript of records from your University

Contact

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please mail your application to: clemens.ostermaier@infineon.com