Institut für Elektronik

Master's Thesis

In cooperation with

Optimized I/O Pad Design for Smartphone Platforms

Current Status and Motivation:

Data communication between individual functional units on a smartphone is running via CMOS I/O pads. Performance parameters for the pads between vendor platforms vary. Not only the voltage level of the power supply is different but also the voltage levels for communication vary. Due to EMI requirements and different loading on the PCB, rise- and fall-times must be controlled. From IC manufactures point of view one pad design shall support the requirements of all customers. Fulfilling the varying needs by one analog design is very challenging.

Research Topic:

The proposed research topic is to design an I/O pad in a 130nm CMOS process which supports a maximum number of platforms. Voltage levels, transition time and propagation delay need to be configurable and stay within their given specifications. To find an optimal solution, different pad architectures shall be investigated, compared and enhanced up to highly innovative solutions.

Approach / Methodology:

- Literature and internet research on CMOS pad topologies
- Usage and further development of already existing pad designs
- Design and verification of an innovative CMOS pad
- Potentially bring the design on a test chip for characterization in the lab

Organisational Matters:

- Start of work: As of now
- Workplace: Infineon Technologies Austria AG Development Center Graz
- Paid thesis: 2.242,19 Euro gross p.m.
- Language: German or English

Contact Person / Supervisor:

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