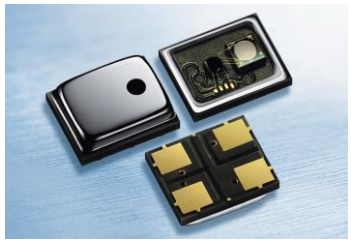
Institut für Elektronik

Master's Thesis

In cooperation with



Verification of an analog front-end for MEMS readout

Current Status and Motivation:

To read out a MEMS signal (voltage, charge, or current) it is typically converted into a digital representative value. The signal path extends from the input (input buffer) via signal shaping (filtering) to the digital output (Sigma-Delta-ADC). Performance parameters (e.g. gain, bandwidth, signal-to-noise ratio, total harmonic distortion, power-supply rejection …) need to be verified via simulation. A pure transient simulation is very inefficient due to its long-lasting simulation time.

Research Topic:

The proposed research topic is to investigate and develop appropriate verification methods to verify the performance parameters of the signal path. There is a mixture of different approaches which leads to the goal: Modeling of circuits in Verilog-A to gain simulation speed, mixed-signal verification, definition of figure-of-merits for the individual circuits which allow to estimate the overall performance, …. Target of the thesis is to explore potential approaches and identify the best solution.

Approach / Methodology:

- Literature- and internet research on state-of-the-art verification methods
- Usage and further development of already existing verification methods
- Simulation and analysis of leading-edge analog circuits for MEMS readout

Organisational Matters:

- Start of work: As of now
- Workplace: Infineon Technologies Austria AG Development Center Graz
- Paid thesis: 2.242,19 Euro gross p.m.
- Language: German or English

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