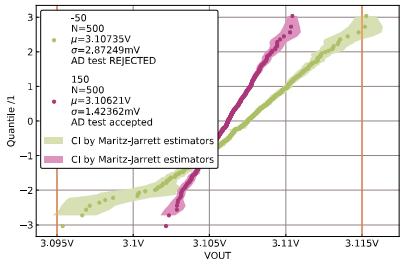
Institut für Elektronik

Master's thesis

In cooperation with



Statistical verification of analog circuits

Current Status and Motivation:

In analog chip design, performance parameters of circuits are randomly distributed due to variations in the CMOS production process. The production behavior is emulated already in simulation (e.g. by Monte Carlo simulation). Correctly interpreting the simulation result is key. The quantile-quantile plot is a common format to visualize such data. Additional statistical features (like confidence interval, statistical tests, …) increase the confidence for correct interpretation of the results.

Research Topic(s):

The proposed research topic is the analyzation of the statistical behavior of different analog circuits and their performance parameters and how to correctly interpret the result.

Approach / Methodology:

- Literature- and internet research on state-of-the-art verification methods in statistical domain
- Statistical simulation and analyzation of leading-edge analog circuits for MEMs readout
- Usage and further development of already existing data analyzation tools

Organisational Matters:

- Start of work: as of now
- Workplace: Infineon Technologies Austria AG Development Center Graz
- Paid thesis: 2.242,19 Euro gross p.m
- Language: German or English

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