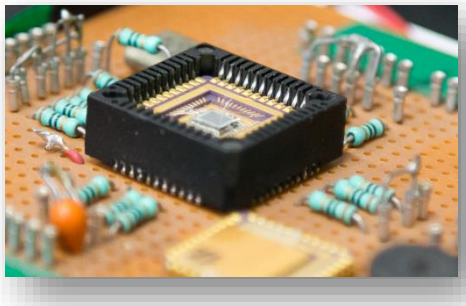
Institut für Elektronik

Master's thesis

In cooperation with XME - Xpert Microelectronic Engineering GmbH



Automatic High Level Modelling of Analog Circuit Blocks and Comparison with Spice Level Models

Current Status and Motivation:

Top level verification of mixed analog digital circuits is difficult and time consuming. A wide range of tools are available to support the modelling of analog circuit blocks but most of them use pre-defined schemes and templates that limit the flexibility in real life designs. The modelling is mostly done by hand and is slow as well as inaccurate and not suited to fast changing circuit designs.

XME has developed a design environment which allows detailed analysis of circuits from the lowest level. Using such an environment allows accurate analysis of analog circuits without a priori assumptions about the architecture or function. This knowledge can then be automatically coded in a high level model for top level verification – thus improving the cycle time and the accuracy enormously.

Research Topic(s):

The thesis develops analysis modules to interrogate the individual circuits, blocks and systems for typical typological structures that underlay the basic electrical functionality. The electrical functionality is then converted to models and these models are combined to make a block level description of the circuit. Comparison between such high level models and the spice simulation show the accuracy and useful range for these models. The use of a data base of circuit solutions allows these analysis modules to 'learn' the standard relationships between typology and function using Artificial Intelligence algorithms.

Approach / Methodology:

Literature- and internet research, state of the art techniques for mixed signal modelling.

The next phase is to extract good modelling techniques for low level blocks.

To develop analysis modules which can recognize the low level structures and map them to models.

To compare the models with the spice representation of the circuit and establish the useful range for such a model as well as the accuracy that we can expect from the model in practice.

Organisational Matters:

- Start of work: ASAP
- Workplace: IFE/TU Graz
- Paid thesis: € 2.800 brutto on ’Werkvertrag’ base
- Period: max. 6 months (subject to negotiations)
- The student should have a good understanding of analog electronic circuits and mathematics and experience in python, ruby and linux.
- The student should have an interest in analog design and in creating new and exciting circuit solutions.

Contact person / Supervisor:

IFE: ...must be defined before the start of the work (!)
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