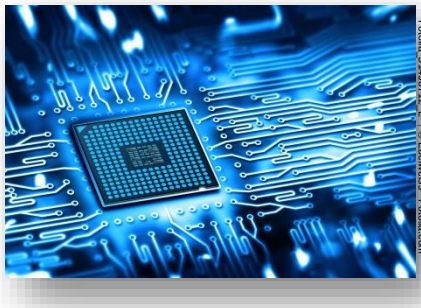
Institut für Elektronik

Master's thesis

In cooperation with XME - Xpert Microelectronic Engineering GmbH



Hardware Acceleration of Analog Circuit Blocks and Comparison with Spice Level Simulations

Current Status and Motivation:

Top level verification of mixed analog digital circuits is difficult and time consuming. A wide range of tools are available to support the modelling of analog circuit blocks but most of them use pre-defined schemas and templates that limit the flexibility in real life designs. The modelling is mostly done by hand and is slow as well as inaccurate and not suited to fast changing circuit designs.
XME has developed a design environment which allows detailed analysis of circuits from the lowest level. Using such an environment allows accurate analysis of analog circuits without a priori assumptions about the architecture or function. This knowledge can then be automatically coded in a high level model for top level verification – thus improving the cycle time and the accuracy enormously.

Research Topic(s):

The thesis develops analysis modules to interrogate the individual circuits, blocks and systems and create synthesizable verilog code for hardware acceleration. Comparison between such modules (synthesized on an FPGA) and the spice simulation show the accuracy and speed improvement of such an approach.

Approach / Methodology:

Literature- and internet research, state of the art techniques for verilog modelling.
The next phase is to extract good verilog modelling techniques for analog blocks.
To then optimize the synthesis of such models for a target FPGA platform.
To synthesize code and test the implementation.
And to compare the synthesized model with the spice simulation of the circuit and establish the accuracy and speed improvement of such an approach.

Organisational Matters:

- Start of work: ASAP
- Workplace: IFE/TU Graz (or name of cooperation partner)
- Paid thesis: € 2.800 brutto on ’Werkvertrag’ base
- Period: max. 6 months (subject to negotiations)
- The student should have a good understanding of electronic circuits and mathematics and experience (interest) in FPGAs, python, ruby and verilog.
- The student should have an interest in mixed signal design and in creating new and exciting verification solutions.

Contact person / Supervisor:

IFE: ...must be defined before the start of the work (!)
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