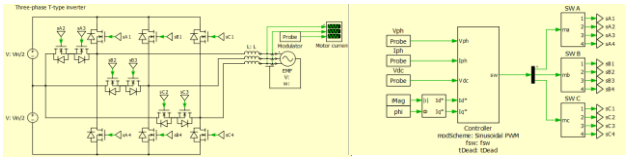
Graz University of Technology
Electric Drives and Machines Institute



Master's Thesis

Several Topics on Three-Level Inverter

Motivation

Multilevel topologies in inverters in combination with wide band gap (SiC, GaN) materials and sinusoidal output filters are a promising technology to reduce EMC and increase the efficiency of motor inverters. Three-level topologies yield to lower voltage levels and higher switching frequencies of the power stage in comparison with 2-level inverters can be implemented. This allows a significant improvement in efficiency, reduction of the filter components which could enable the integration of sine motor filter into the drive stage, however, some challenges need to be addressed to benefit from the advantages.

Topics on Three-Level Inverter

- Modulation and balancing of three-level inverters under different load conditions.
- Optimal paralleling of three-level inverter stages to increase power range.
- Design and optimization of three-level inverter with integrated sinus motor filter.
- Etc.

Tasks

- Literature study of possible solutions.
- Derivation of convenient PLECs simulation models for the corresponding topic.
- Development of new approaches, structures and detailed analysis on the developed approaches.
- Optimization of the approaches based on (semi-) analytical models.

Further Information

- Start: asap (according to agreement)
- Workplace: EAM Institute TU Graz (Workplace directly at B&R automation possible)

Contact

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