The Qubit is the Transistor: Si-based Transistor and Analog-Mixed-Signal Circuit Scaling and the Natural Progression of Moore's Law to Silicon Quantum Computing at the Atomic Scale

The short story

Quantum computing is a hot topic at very cool temperatures. Cool as in 10-100 mK.

Recently, a cold-atom physicist nonchalantly asked me the question: Why are you interested in high temperature quantum computers? High as in 4-12 K. He was serious! Need I talk about Global Warming in such cool environments? Pluto is another option.

Today, quantum computers consist of racks of microwave and analog-mixed-signal test equipment, FPGAs and feedback loops for error correction, long 50-Ohm coaxial cables, and a few qubits formed with non-linear Josephson-junction resonators, entangled through niobium superconducting $\lambda/4$ resonators at 8-20 GHz, biased by a DC magnetic field of up to 1 Tesla, and whose spin is controlled by an AC magnetic field rotating in the "lab frame". Are you still spinning?

There's talk of electrons as "microwave photons", Larmor and Rabi frequencies, photon-to-spin entanglement, RAP (as in rapid adiabatic passage), Bloch sphere, tensors in n-dimensional Hilbert spaces, but also of OFDM, phase noise, I-Q up- and down-conversion, Gaussian pulse modulation, coherent $\pi/2$, $\pi/4$ spin phase rotations in azimuth and elevation. Qubits are logic gates and memory cells at the same time. Logic gate operations consist of synchronized microwave pulses applied sequentially to the same qubits. The only probabilistic part (need I mention Schrodinger's cats Flip and Flop?) is readout, when the spin state is projected on the Z (DC magnetic field) axis.

In other words, quantum computing is about everything you learned and thought you'd never use again, should have learned, or you were never taught in undergrad and grad school in math, quantum and atomic physics, electronics, electromagnetics, and computer science...

This talk will first attempt to demystify and translate the physics of quantum computing to an electronics engineer jargon. Next, I will discuss the feasibility of high-temperature (2-4 K) Si and SiGe electron/hole-spin qubits and qubit integrated circuits (ICs) in commercial 22nm FDSOI CMOS technology, and explore their scalability through simulation to 2nm dimensions, when the coupling energy, ΔE, becomes comparable to thermal noise at 77-300 K.

The longer story

Silicon electron-spin and hole-spin coupled quantum-dot (QD) qubits have attracted a lot of interest recently due to their potential for integration in commercial CMOS technology. However, like their more established superconducting cousins, to date, because of the low confinement and coupling energies (e.g. ΔE, in the tens of μeV range, comparable to the thermal noise level, $k_B T$, at 100 mK) their operation has been restricted to temperatures below 100 mK. Moreover, since cryogenic systems cannot remove more than a few μW of thermal power at 100 mK, and the experimental laboratory (think university lab versus 7nm FinFET fab) technologies in which these qubits have been realized do not allow for fabrication of spin manipulation and readout circuitry, the latter reside on a separate chip, at 4 K or higher temperature. The lack of monolithic integration further degrades readout fidelity and computing speed because the atto-Farad capacitance, high-impedance qubit needs to drive 50Ω and 100x larger capacitance interconnect off-chip. A qubit with higher confinement and coupling energies, with spin resonance in the upper mm-wave region, will allow for higher temperature operation, alleviating these problems and enabling large-scale monolithic quantum computing processors. For

example, a qubit operating at 4 K would require mode splitting energies of 0.25 meV which corresponds to a spin resonance frequency of 60 GHz and require a DC magnetic field of 2.5 T. Simplifying a bit, 240GHz spin-resonance frequencies and 9T magnetic fields should be adequate for 12K operation and 1.4 THz and a humongous magnetic field are needed for 77 K. You get the idea.

Finally, I will briefly review hot-off-the-press results obtained at the University of Toronto. For the first time we report (i) integration of qubits and electronics on the same die, (ii) strained SiGe hole-spin and strained Si electron-spin FDSOI qubits on the same die, and (iii) propose a monolithic processor architecture which allows for short, 10-20ps spin control pulses and high Rabi frequencies, f_{Rabi}, to compensate for short spin phase coherence lifetime. We also demonstrate that, at 2 K, MOSFETs and cascodes can be operated as QDs in the subthreshold region while behaving as classical MOSFETs and cascodes in the saturation region, suitable for qubits and mm-wave mixed-signal processing circuits, respectively.

Time permitting, I will go through a tutorial example of how we can derive the specification for the mm-wave spin manipulation and readout circuits starting from the Hamiltonian and the measured I-V characteristics of our SiGe hole-spin qubits. I may touch on the impact of minimum-size (18nmx6nmx80nm) MOSFET threshold voltage and process variation on qubit characteristics, on spin manipulation and readout architectural options (low phase-noise radar, OFDM radio, low-noise, broadband, ultra-high-gain TIAs), mm-wave switch impact, and OFDM sub-carrier spacing on qubit crosstalk and isolation.