

DESIGN CONSIDERATIONS TO IMPROVE THE EFFICIENCY OF AN AC-AC CONVERTER AT LOW PARTIAL LOAD

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Introduction

Often home appliances are mainly operated at low partial load, what has increased interest in increasing their energy conversion efficiencies in this area of operation. We review different design considerations to improve an AC-AC converter designed to operate at a low partial load of 7 W, which is 10 % of its maximum thermal capability.

AC-DC Converter – the Power Factor Correction Unit

A new single-phase hybrid bridge-less step-down PFC converter topology, (Fig. 1) allows removing the dead times of the AC line current in the conventional buck PFC (Fig. 2), thereby improving the power factor (Fig. 3). This may be enhanced by an improved control, operating in Critical Conduction Mode (CRM) and utilising Constant On Time, thus significantly reducing the losses in the PFC because of turning on and off the operating switch at zero voltage (Fig. 4). [1]

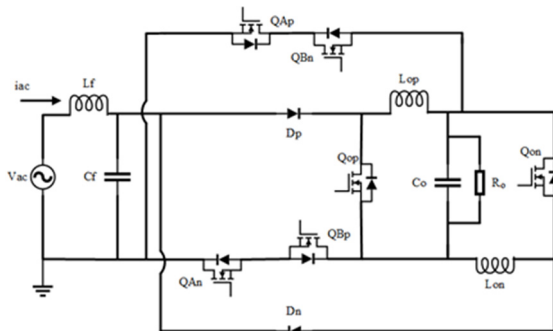


Figure 1: Proposed hybrid bridge-less step down PFC converter

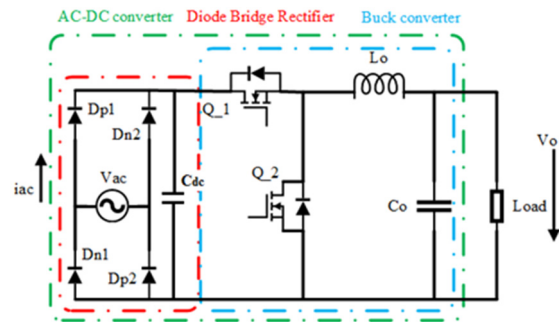


Figure 2: Conventional buck PFC topology

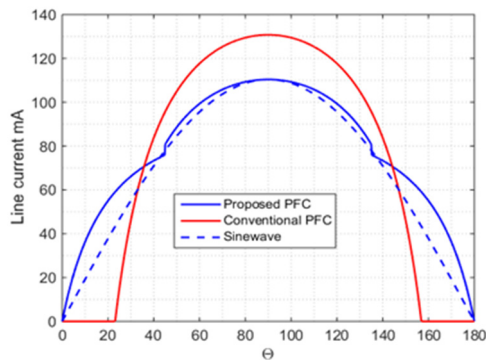


Figure 3: AC line currents of both PFCs topologies. The line current of the proposed PFC is much closer to a sinewave.

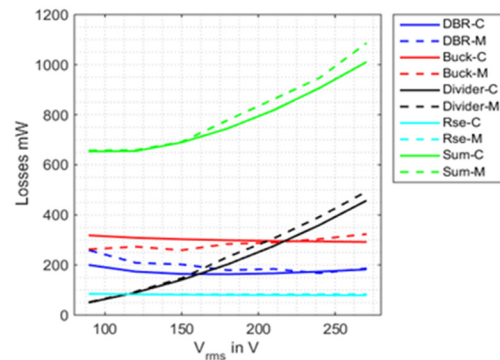


Figure 4: Measured (-M) and computed (-C) losses of a conventional buck PFC (Fig. 2), with applying an improved CRM with COT; DBR = Diode Bridge Rectifier; Buck = Q₁ and Q₂, Divider = voltage divider to sense the input voltage, Rse = inductor current sensing resistance.

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DC-AC Converter – Inverter

Hard Switching Inverter (HSI) [2]

The switching losses of this well-known inverter can be reduced by optimizing the turn on dead time of both switches (Fig. 5).

However, the use of a RGD (as proposed in [3]) does not reduce the gate drive losses of the MOSFETs selected here, because of their relatively high internal gate resistance.

Soft Switching Inverter [4]

The losses of an Auxiliary Resonant Commutated Pole Inverter (ARCPI, Fig. 6, originally proposed in [5]) can be further reduced by, again, introducing a new switching sequence and, in addition, adjusting, the boost current according to the instantaneous value of the sinusoidal load current as well as skipping one of the two auxiliary pulses in each switching cycle.

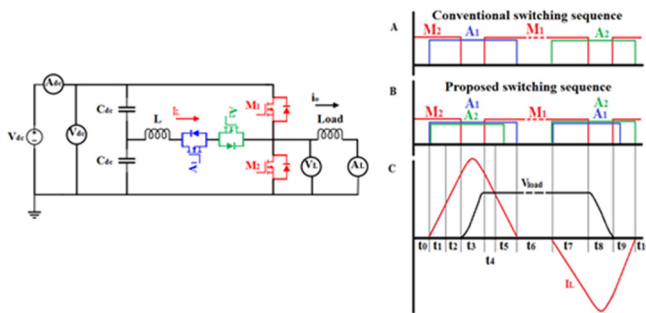


Figure 6: ARCP as proposed in [5]; A. conventional switching sequence, B. proposed switching sequence, C. load voltage and resonant current.

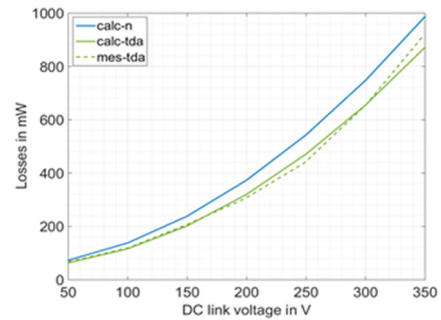


Figure 5: Measured (dashed green) and calculated (solid green) losses of the hard switching inverter when optimizing the turn on dead time. The solid blue curve shows the losses of the conventional approach.

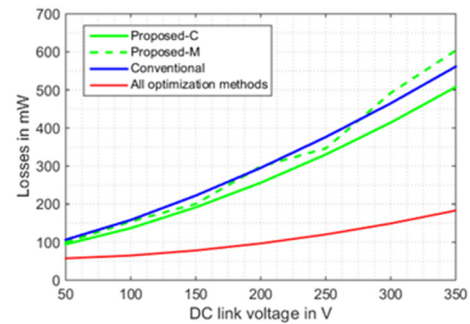


Figure 7: Measured and calculated losses of the ARCP: conventional (blue), proposed switching sequence (green), all proposed optimization methods applied (red).

Numerical models, based on analytic formulas, have been established for all the investigated stages (PFC, HSI, ARCPI, RGD), allowing to compute the losses and the efficiencies respectively using component data sheet information only. These models can be used for component selection and for determining optimum operating regions enabling further reduction of system losses and thus overall system optimisation.

References

- [1] K. A. Mahafzah, Design Considerations to Improve the Efficiency of an AC-AC Converter at Low Partial Load, Doctoral Thesis, Graz University of Technology, Jan. 2018.
- [2] K. A. Mahafzah, K. Krischan, and A. Muetze, "Efficiency enhancement of a three phase hard switching inverter under light load conditions", Proc. IECON 2016, pp. 3372-3377.
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