Power Hardware-in-the-Loop testing for the Inverter-based Distributed Power Source

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Abstract: This paper presents a Power Hardware-in-the-Loop (PHIL) test platform for the inverter-based distributed power source. A quantitative study of the precision and stability of this PHIL test platform is given. A detailed basic study of the relationship between delay and accuracy of HIL test platform is carried out by means of the system stability criterion. Finally, the PHIL test platform has been built in the laboratory. The function of the HIL test platform is verified by a set of PHIL tests for PV inverter.

Keywords: Hardware-in-the-Loop test, grid-connected inverter, grid model, LVRT

1. Introduction

In the process of R&D of inverters of distributed power source, testing and validation of a new circuit topologies or control algorithms can at the present stage only be carried out after the completed construction and erection of the prototype. This implies very high costs and time risks.

The new suggested R&D approach, which based on the HIL test concept, allows testing of every phase of development (**Figure 1**). After the control algorithms and hardware topology design is finished, an offline simulation test for verification of the correctness of the design have been carried out [**1**].

When the controller design (such as the peripheral circuits of processors, the sensor signal processing circuits, the driving circuits, etc.) and programming is completed, a test and validation will be done by means of Controller Hardware-in-the-Loop (CHIL) (**Figure 2, left**), while the controller is connected to the inverter model in a real-time simulation system, to verify the functions of the controller and programs [**2**]. CHIL can test the influences of the signal delay, sampling error. The black box testing of the control program can be executed, to improve the efficiency of the debugging.

When the construction of the prototype of an inverter-based distributed power source has been carried out, the power grid model and some parts of mechanical modules in the real-time simulation system will be connected with the prototype, namely Power Hardware-in-the-Loop (PHIL) (**Figure 2, right**), to verify the fully functions and the matching between hardware and controller.

This R&D approach can find design defects in the earlier phases, instead of detecting an irreparable error in the final stage, which can make the entire R&D project to re-invent the wheel. Using this approach can improve the efficiency and thereby reduce development costs and time.

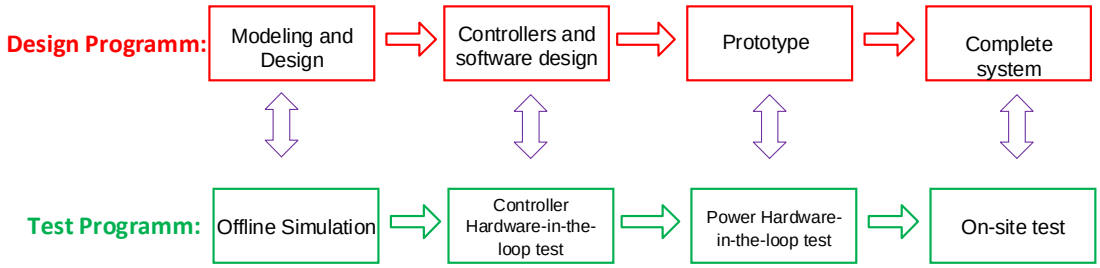

Figure.1: R&D approach of an inverter-based distributed power source based on Hardware-in-the-Loop (HIL) test platform

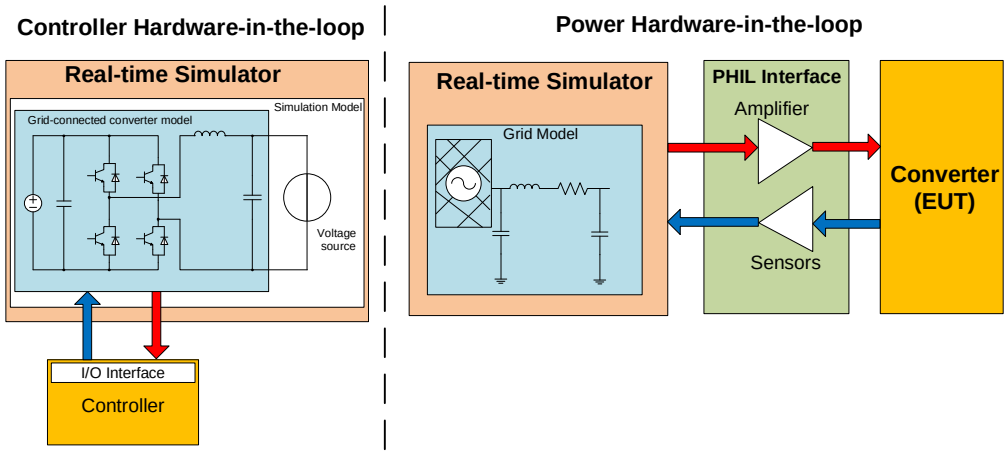

Figure.2: Left: Controller Hardware-in-the-Loop (CHIL); Right: Power Hardware-in-the-Loop (PHIL)

2 Power Hardware-in-the-Loop

The equipment under test (EUT) of PHIL is the inverter-based distributed power source. Since the signal exchange between the EUT and an RTS is through high-power signals, the PHIL Interface (PI) is required (**Figure 2, right**). The PI is responsible for converting the power signal from EUT to small signal for RTS through the sensors, simultaneously converting the small signal from RTS through the power amplifier to fulfill large power signal for EUT. The power amplifiers and sensors will inevitably lead to a system delay problem. These problems will affect the accuracy and stability of the real-time simulation.

The commonly used topologies of PHIL interface in the literature [**3**,**4**,**5**] is the ideal transfer method (ITM) (**Figure 3**).

The principle of ITM-PHIL is shown in **Figure 3**. In pink box is the software part of the system. U_q in this case is the voltage source of the grid model, Z_{Sim} is the grid impedance of the grid model, I_{Sim} is represents the influence of the EUT current upon the grid in the form of a current source. In the blue box is the real world. U_{EUT} is the output voltage of the power amplifier. Z_{EUT} is the impedance of the real world. The interaction of the grid model and the real world is realized by the PHIL interface (green box in **Figure 3**). The output voltage signal of the grid model is fed to the EUT, and the current signal of EUT will be feedback to the grid model by the simulating current source.

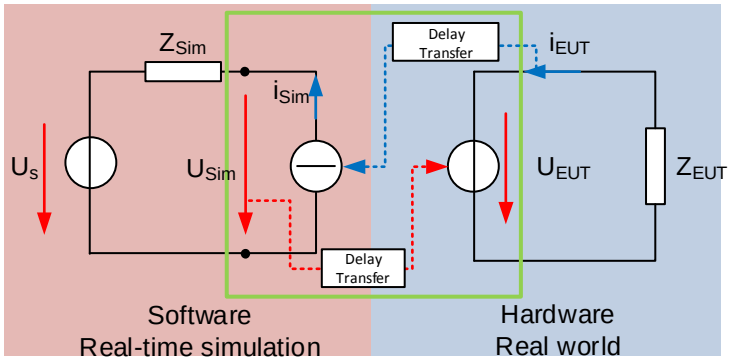

Figure.3 Simplified circuit of PHIL interface the ideal transfer method

2.1 Study of stability

Due to the delay properties, the relationship between two voltage signals and two current signals can be expressed by the following equation:

$$U_{EUT}(s) = e^{-st_{da}} G_A(s) U_{Sim}(s) \tag{2.1}$$

$$i_{Sim}(s) = e^{-st_{ds}} G_S(s) i_{EUT}(s) \tag{2.2}$$

t_{da} and t_{ds} are the time delays for of the two respective signals. $G_A(s)$ and $G_S(s)$ are the transfer function of the amplifier and sensor systems.

Since the real-time simulator is discrete operation, the results of the simulation are delay from the input signal. The time delay t_{dc} is its simulation step. The results of the simulation can be expressed by the following equation:

$$U_{Sim}(s) = e^{-st_{dc}} (U_S(s) - i_{Sim}(s) Z_{Sim}(s)) \tag{2.3}$$

The block diagram of PHIL testing system (**Figure 4**):

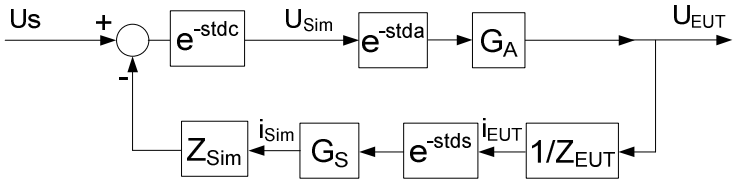

Figure.4 the block diagram of the ideal transfer method PHIL system

The close loop transfer function of the U_{EUT} to U_s is given by G_{ITM_CL} (s):

$$G_{ITM\_CL}(s) = \frac{U_{EUT}(s)}{U_S(s)} = \frac{e^{-st_{dc}} e^{-st_{da}} G_A(s) Z_{EUT}(s)}{e^{-st_{ds}} e^{-st_{dc}} e^{-st_{da}} G_S(s) Z_{Sim}(s) + Z_{EUT}(s)} \tag{2.4}$$

And the open loop transfer function:

$$G_{ITM\_OL}(s) = -e^{-st_{ds}} e^{-st_{da}} e^{-st_{dc}} G_A(s) G_S(s) \frac{Z_{Sim}(s)}{Z_{EUT}(s)} \tag{2.5}$$

In order to facilitate the analysis, assume the signal through the sensors and the amplifier without distortion, only delay. That means:

$$G_A(s) = G_S(s) = 1 \tag{2.6}$$

The total delay of PHIL testing system is t_d, which

$$t_d = t_{da} + t_{ds} + t_{dc} \tag{2.7}$$

Let the equation 2.6 and 2.7 into 2.5, the simplified the open loop transfer function:

$$G_{ITM\_OL}(s) = -e^{t_d} \frac{Z_{Sim}(s)}{Z_{EUT}(s)} \tag{2.8}$$

According to the nyquist stability criterion [6], we can discuss the stability of the system with the open loop transfer function (**Figure.5**). Take this for example: Z_{Sim} and Z_{EUT} are two RL series circuits, the time delay of system is 100µs, and the arbitrarily chosen impedance parameters are as follows:

Table.1: Impedance parameters of Z_{Sim} and Z_{EUT}

	Case 1		**Case 2**	
	Z_{Sim}	Z_{EUT}	Z_{Sim}	Z_{EUT}
R	2 Ω	1Ω	1Ω	2Ω
L	2 mH	1 mH	1 mH	2 mH

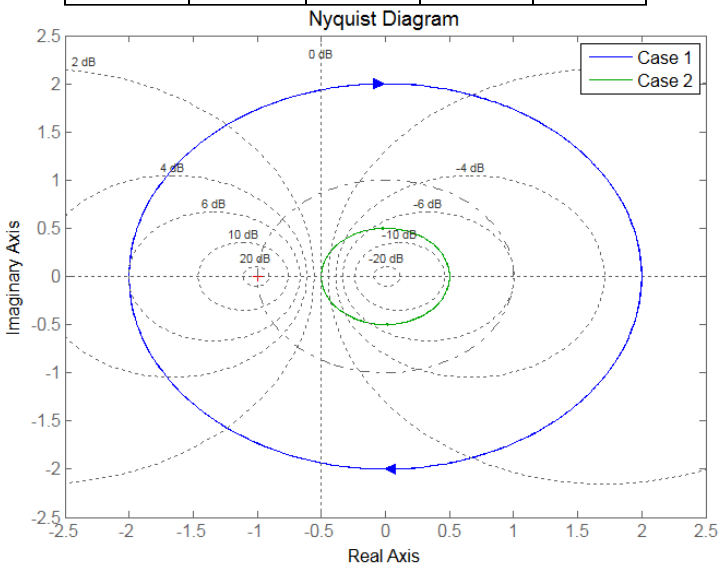

Figure.5 the nyquist curve of the open loop transfer function

Which in Case 1, the absolute impedance ratio $|Z_{Sim}/Z_{EUT}|>1$, and in Case 2, $|Z_{Sim}/Z_{EUT}|<1$.

From the **Figure 5**, in Case 1, the nyquist curve (blue) enclosed the point [-1, j0], so the system is not stable. In Case 2, the nyquist curve (green) is not enclosed the point [-1, j0], so the system is stable. As a result, when the impedance of the power network model is greater than the impedance of the EUT, the ITM-PHIL system will lose its stability.

2.2 Study of accuracy

With the close loop transfer function (**Equation 2.4**), we can discuss the accuracy of the system.

Due to the delay caused by the sensors t_{ds} is very small, so here is the assumption that the following approximation:

$$t_d = t_{da} + t_{ds} + t_{dc} \approx t_{da} + t_{dc} \tag{2.9}$$

Let the equation 2.6 and 2.9 in 2.4:

$$G_{ITM\_CL}(s) = \frac{U_{EUT}(s)}{U_S(s)} = \frac{e^{-st_d} Z_{EUT}(s)}{e^{-st_d} Z_{Sim}(s) + Z_{EUT}(s)} \tag{2.10}$$

In the ideal case which is without system delay, $G_{ITM\_Ideal}(s)$ of the PHIL system is given by (Eq. 2.11):

$$G_{ITM\_Ideal}(s) = \frac{U_{EUT}(s)}{U_S(s)} = \frac{Z_{EUT}(s)}{Z_{Sim}(s) + Z_{EUT}(s)} \tag{2.11}$$

The accuracy of PHIL can be quantitatively analyzed and the relative error Error(s) of the delay is stated as follows:

$$Error_{ITM}(s) = 20\log\left(\frac{G_{ITM\_CL}(s) - G_{ITM\_Ideal}(s)}{G_{ITM\_Ideal}(s)}\right) \tag{2.12}$$

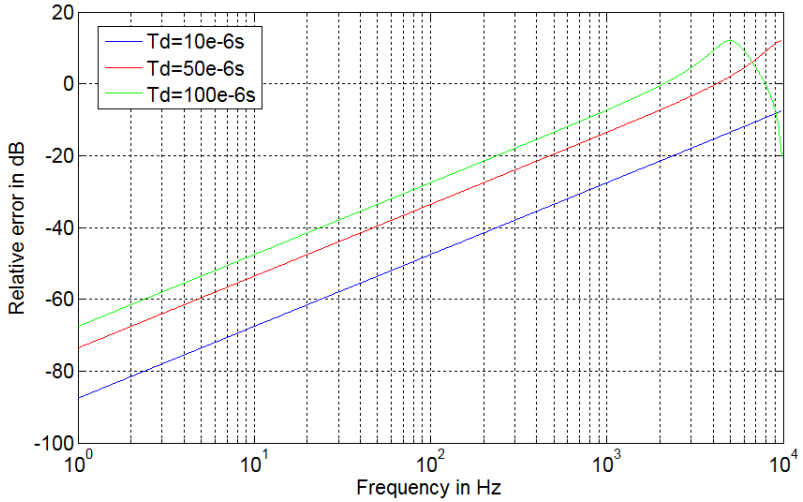

Figure.6 Frequency response of the relative error with difference delays

Here the impedance parameters of Z_{Sim} and Z_{EUT} from **case 2** in **Chapter 2.1** are used as an example again, and the time delays are 10µs, 50µs and 100µs.

In **Figure 6,** the error increases with the frequency of the same delay. At the same frequency, the error increases with the delay. This is reflects the limited working bandwidth of the PHIL testing system. In this example case, at the 50Hz, all the relative errors are small than -20dB. But at the 2000 Hz, only the relative errors from t_d = 10µs is small than -20dB.

When using different impedance combinations and same time delays t_d = 10µs:

Table.2: Impedance parameters of Z_{Sim} and Z_{EUT}

	Case 3		**Case 4**		**Case 5**	
	Z_{Sim}	Z_{EUT}	Z_{Sim}	Z_{EUT}	Z_{Sim}	Z_{EUT}
R	1 Ω	2Ω	1Ω	10Ω	1Ω	100Ω
L	1 mH	2 mH	1 mH	10 mH	1 mH	100 mH

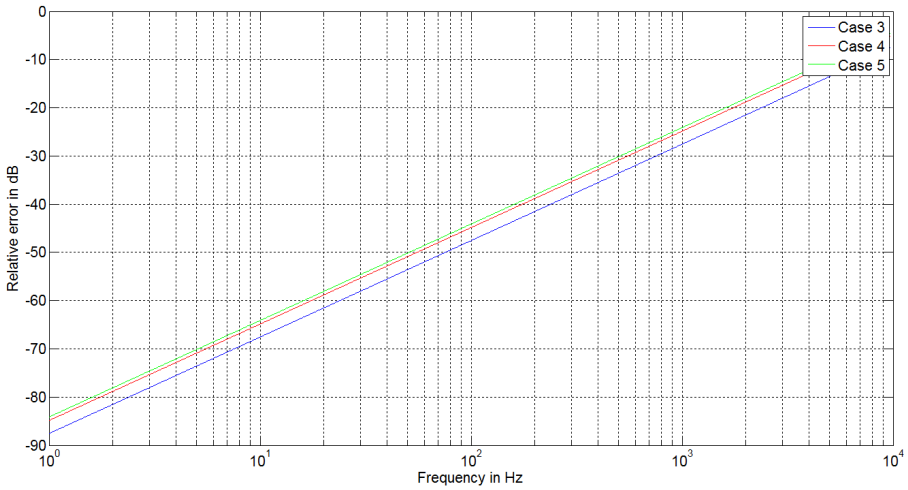

Figure.7 Frequency response of the relative error with difference impedance combinations

Figure 7 shows, in all frequency range, the relative error of **Case 3** is the minimum, and the relative error of **Case 5** is the maximum. Since absolute impedance ratio $|Z_{Sim}/Z_{EUT}|$ of **Case 3** is the smallest, and the absolute impedance ratio of **Case 5** are biggest, the following conclusions can be obtained. In ITM mode, under the premise of stable ($|Z_{Sim}/Z_{EUT}|<1$), the smaller the difference between Z_{Sim} and Z_{EUT}, cause the smaller the system relative error.

3 Laboratory realization

Through the research of the above chapters, a PHIL testing system for PV inverter as EUT in the laboratory is established (See **Figure 8** and **Figure 9)**.The real-time simulator is the product from dSpace®. The output voltage of the PV cell is simulated by DC source (PV Simulator), and is supplied to the EUT (PV inverter). Output voltage of the power amplifier used to simulate the grid voltage. Here the power amplifier is an IGBT based four-quadrant voltage source, the capacity of the amplifier is 120kVA.

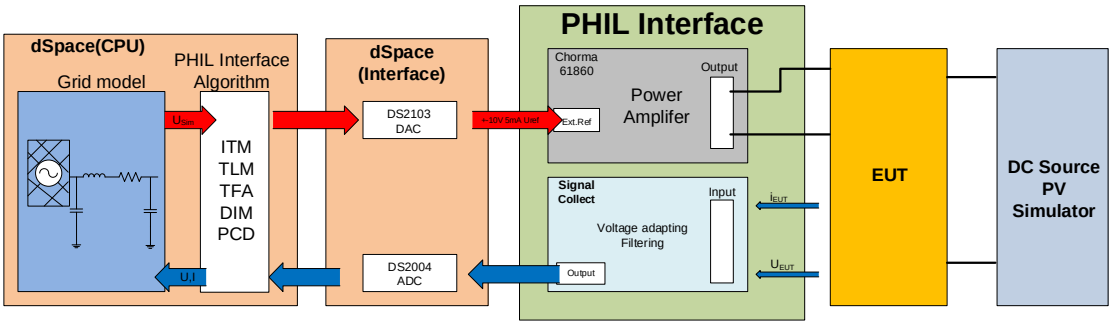

Figure.8 Topology of the PHIL testing system

The AC voltage and current signals from EUT through the voltage adaptation and filter circuit transfer into the ADC Unit of dSpace system. Then the current signal from EUT is through the PI algorithm input to the grid model. The calculation results of the grid model output to EUT through the power amplifier.

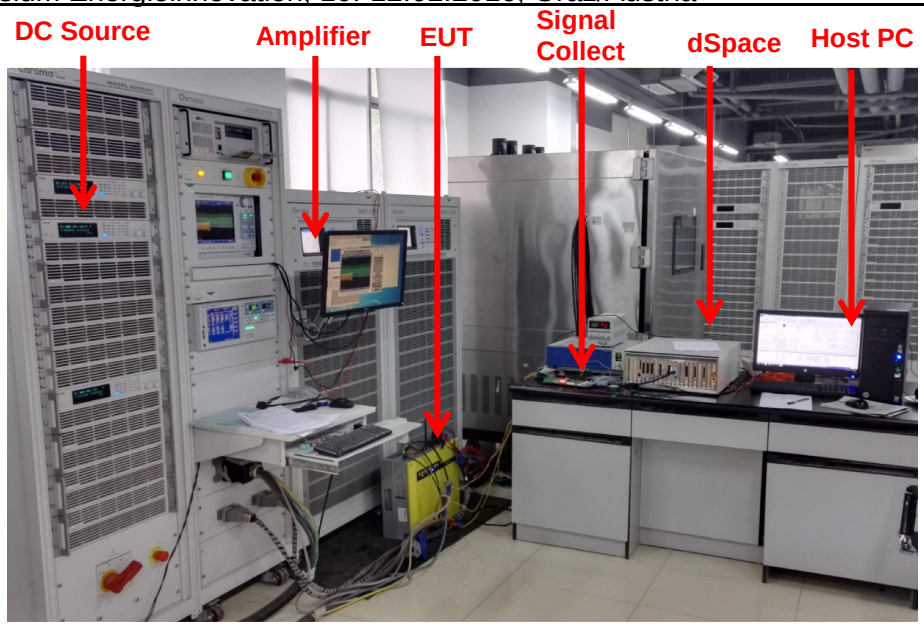

Figure.9 PHIL testing system in Laboratory

Taking a typical single phase low voltage grid as an example (**Figure.10**). The EUT is a single phase PV inverter, with rated AC power 4600W.The rated output voltage form the EUT is 230V, then power transport to the point of common coupling (PCC) by a 100m long cable. There are other loads in the same low voltage grid. The transmission cable of Load 1 will occur the ground fault. There are also 10 sets of load groups and cables in this grid. The load 3 is cut-in or cut-off by a circuit breaker S1.

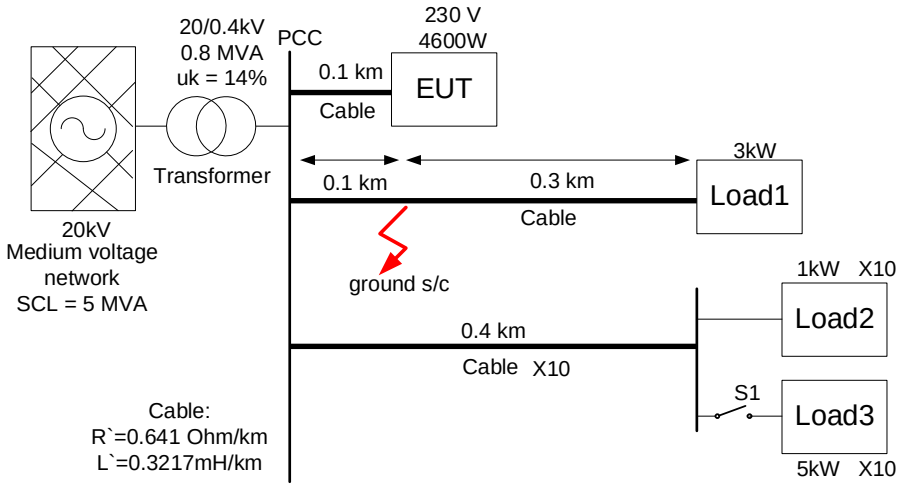

Figure.10 test grid model

Use the method of system identification, we get the transfer function of the power amplifier:

$$G_{Amp}(s) = e^{-90\cdot10^{-6}\cdot s}\frac{7.125\cdot10^{9}}{s^{2}+3.73\cdot10^{4}s+1.679\cdot10^{8}} \tag{3.1}$$

Its time delay is 90 μs and the phase shift at 50Hz is -4 degree. The cutoff frequency is 900Hz. The output impedance of EUT Z_{EUT} from rated power can be getting from followed equation:

$$Z_{EUT} = R_{EUT} = \frac{U_{rated}^{2}}{P_{rated}} = \frac{230V^{2}}{4600VA} = 11.5\Omega \tag{3.2}$$

This is the minimum impedance of EUT, because the EUT will limit its output power. When the output power is small, for example, when the DC input power is small, according to the **equation 3.2**, the output impedance of EUT will be bigger. At the same time, the grid impedance Z_{Sim} is much less than 11.5 ohm. According to the discussion in the **chapter 2.1**, this PHIL system is stable.

When meeting the starting conditions, this EUT will increase the output current from 0A to the rated current (22A) in 15 seconds. When we set the output voltage of the AC source fixed at 230V, which is the common test settings (i.e. non-PHIL test), the output voltage will not change with the increase of EUT current (**Figure.11 left**). In PHIL test with the above grid model (**Figure.10**), the output voltage will change with the increase of EUT current (**Figure.11 right**). This is realized the grid retroactive effects in the test, making the test more realistic.

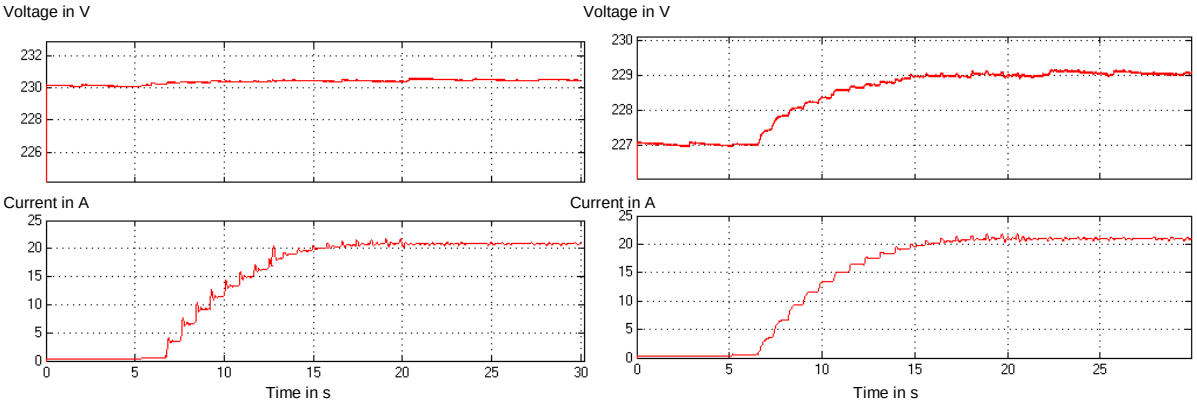

Figure.11 without PHIL (left) vs with PHIL (right); upper: V_{RMS} curve, down: i_{RMS} curve

The test of the Low Voltage Ride Through (LVRT) capability of EUT is also based on PHIL with the above grid model (**Figure.10**). The voltage dip will be realized by a short circuit fault, its duration is 650ms. The fault point is 100m from the PCC and circuit breaker S1 is close. The voltage and current curves are shown in **Figure 12**.

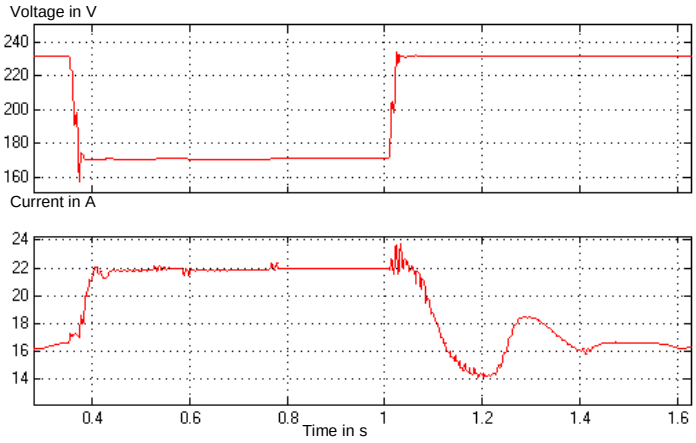

Figure.12 V_{RMS} (upper) and i_{RMS} (down) curve during the short circuit fault

The voltage drops from 231.9V to 170.8V, the residual voltage rate is 73.6%. At the same time, the current rises from 16A to 22A, which is the maximum rated current of EUT. The rising of current is due to the balance of input and output power of EUT.

$$P_{in} = P_{out} = UI \tag{3.3}$$

According to the **equation 3.3**, when the input power $\mathbf{P_{in}}$ kept constant, the grid voltage **U** drops, in order to meet the power balance, the EUT output current **I** must increase. When the voltage drop is much bigger, the output current reaches its set limit, and the input and output power of EUT cannot be balanced, the excess power will enter the DC capacitor, increase the DC bus voltage. If there is no protection, this will lead to damage to components. In this case, the power balance is just meet during voltage dip, so EUT can operate continuously for 650ms or even longer at low voltage situation.

The voltage and current waveforms at the moment when the voltage dip occur are shown in **Figure 13**. Can be seen from the figure, at the moment of voltage drop, the current (blue) appeared a spike, and then the current becomes unstable, there have been several oscillations. The current spike is caused by the transient response of EUT. The reason for the current oscillation is: in order to balance the input and output power of EUT, the DC bus voltage becomes transient instability, which result current amplitude control loop oscillation. Because the output current amplitude is controlled by the DC bus voltage.

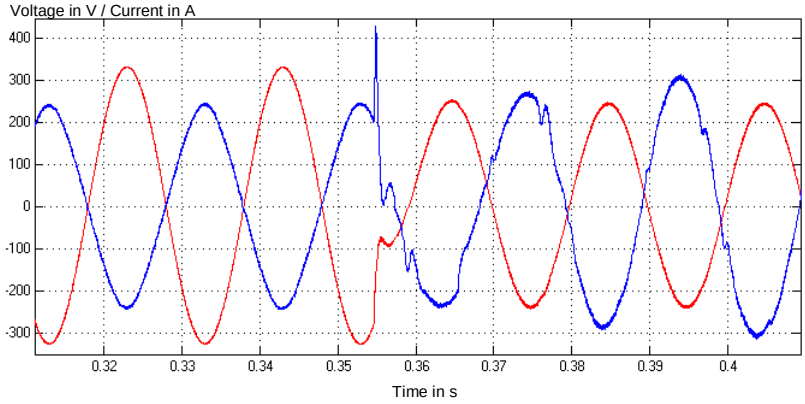

Figure.13 voltage (red) and current (blue, ten-times magnification) waveforms at the moment when the voltage dip occurs

When using the same configuration for another test, a different result is obtained, shown in the **Figure.14**. After the voltage drop, the current output of the EUT is stopped.

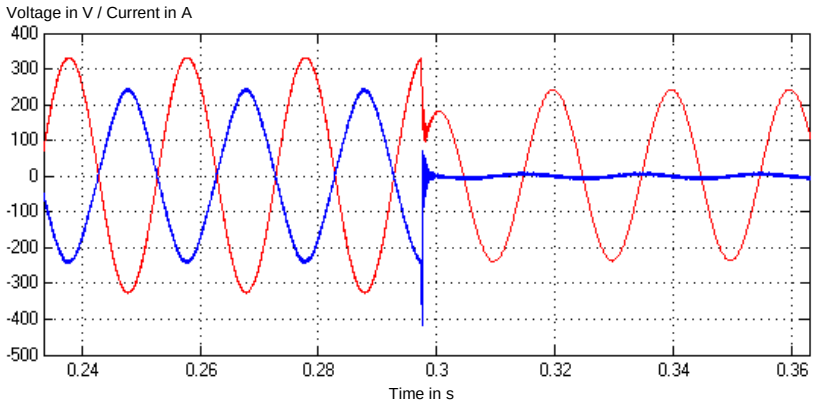

Figure.14 voltage (red) and current (blue, ten-times magnification) waveforms at the moment when the voltage dip occurs

In 5ms after voltage drop, the current has a high frequency oscillation. This is different from the low frequency oscillations in **Figure.13**. In **Figure.14**, the voltage drop occurs at the highest point of voltage. This caused a drastic imbalance process of power, and then leads to the integral saturation of the current amplitude control loop of EUT, triggering the

shutdown protection. In **Figure.13**, the voltage drop occurs at a lower voltage point, so the oscillation is smaller.

The common testing process (non-PHIL test) let the voltage drop occurs at the zero crossing point of the voltage. So it will not produce current oscillations, makes LVRT ability test much easier. But this also lost the realistic of the test.

5 Conclusions

In this paper, a PHIL based testing method is presented. This paper presents a quantitative study of the accuracy and stability of the PHIL testing system. A detailed basic study of the relationship between delay and accuracy of PHIL system, and gives the system stability criterion. Finally, the PHIL testing system has been built in the laboratory. The function of the PHIL testing system is verified. This paper takes a typical low voltage grid as an example, a set of PV inverter PHIL tests are carried out. The experimental results are analyzed in detail, the necessity and realistic of PHIL test is proved.

6 References

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